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# HD74AC194

## 4-bit Bidirectional Universal Shift Register

# HITACHI

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### Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation: parallel (broadside) load, shift right (in the direction  $Q_0$  toward  $Q_3$ ); shift left; inhibit clock (do nothing).

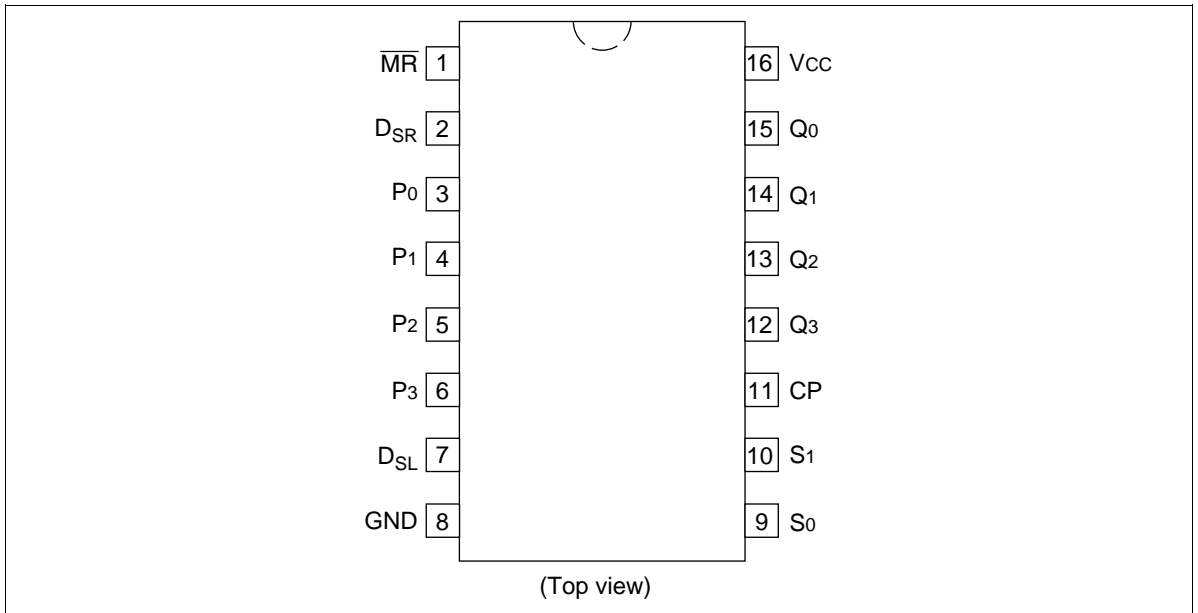
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs,  $S_0$  and  $S_1$ , high. The data are loaded into their respective flip-flops and appear at the output after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when  $S_0$  is high and  $S_1$  is low. Serial data for this mode is entered at the shift right data input. When  $S_0$  is low and  $S_1$  is high, data shifts left synchronously and new data is entered at the shifts left serial input. Clocking of the flip-flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the clock input is high.

### Features

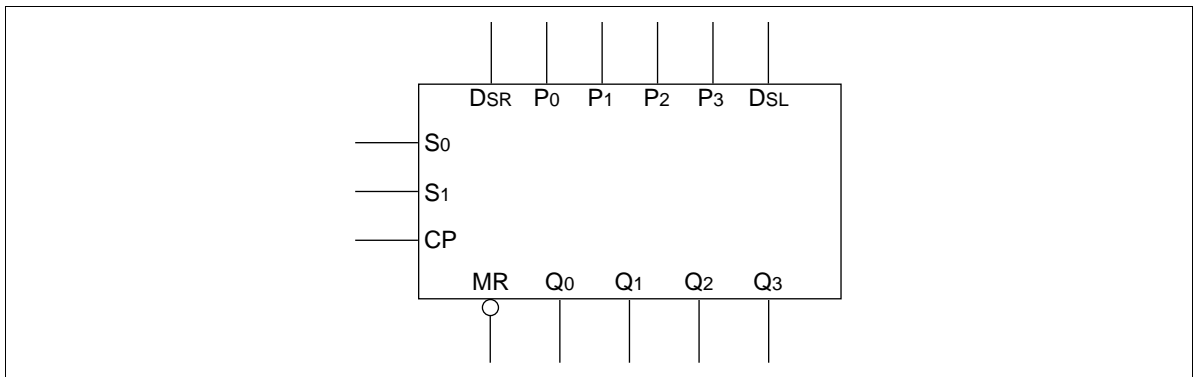
- Asynchronous Master Reset
- Hold (Do Nothing) Mode
- Outputs Source/Sink 24 mA

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## Pin Arrangement



## Logic Symbol

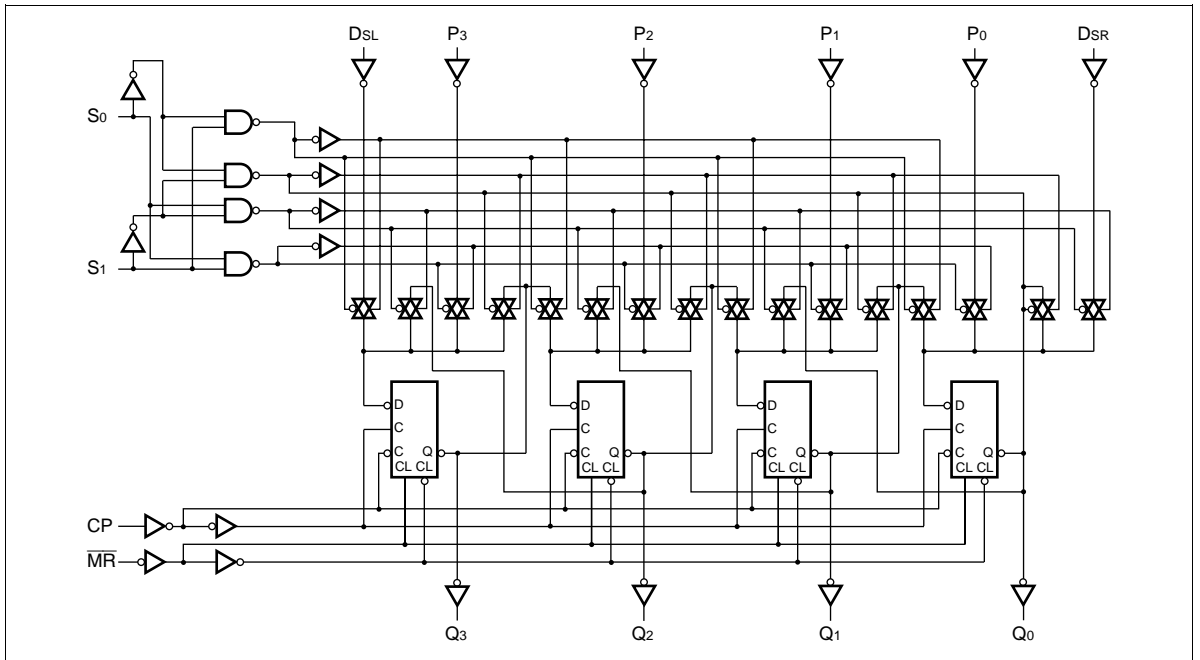


## Pin Names

- S<sub>0</sub>, S<sub>1</sub> Mode Control Inputs
- P<sub>0</sub> to P<sub>3</sub> Parallel Data Inputs
- D<sub>SR</sub> Serial Data Input (Shift Right)
- D<sub>SL</sub> Serial Data Input (Shift Left)
- CP Clock Pulse Input (Active Rising Edge)
- $\overline{\text{MR}}$  Asynchronous Master Reset Input (Active LOW)
- Q<sub>0</sub> to Q<sub>3</sub> Parallel Outputs

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Logic Diagram



Mode Select Table

Operating Mode	Inputs						Output			
	$\overline{MR}$	$S_1$	$S_0$	$D_{SR}$	$D_{SL}$	$P_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	L	L	X	X	X	$q_0$	$q_1$	$q_2$	$q_3$
Shift Left	H	H	L	X	L	X	$q_1$	$q_2$	$q_3$	L
	H	H	L	X	H	X	$q_1$	$q_2$	$q_3$	H
Shift Right	H	L	H	L	X	X	L	$q_0$	$q_1$	$q_2$
	H	L	H	H	X	X	H	$q_0$	$q_1$	$q_2$
Parallel Load	H	H	H	X	X	$p_n$	$p_0$	$p_1$	$p_2$	$p_3$

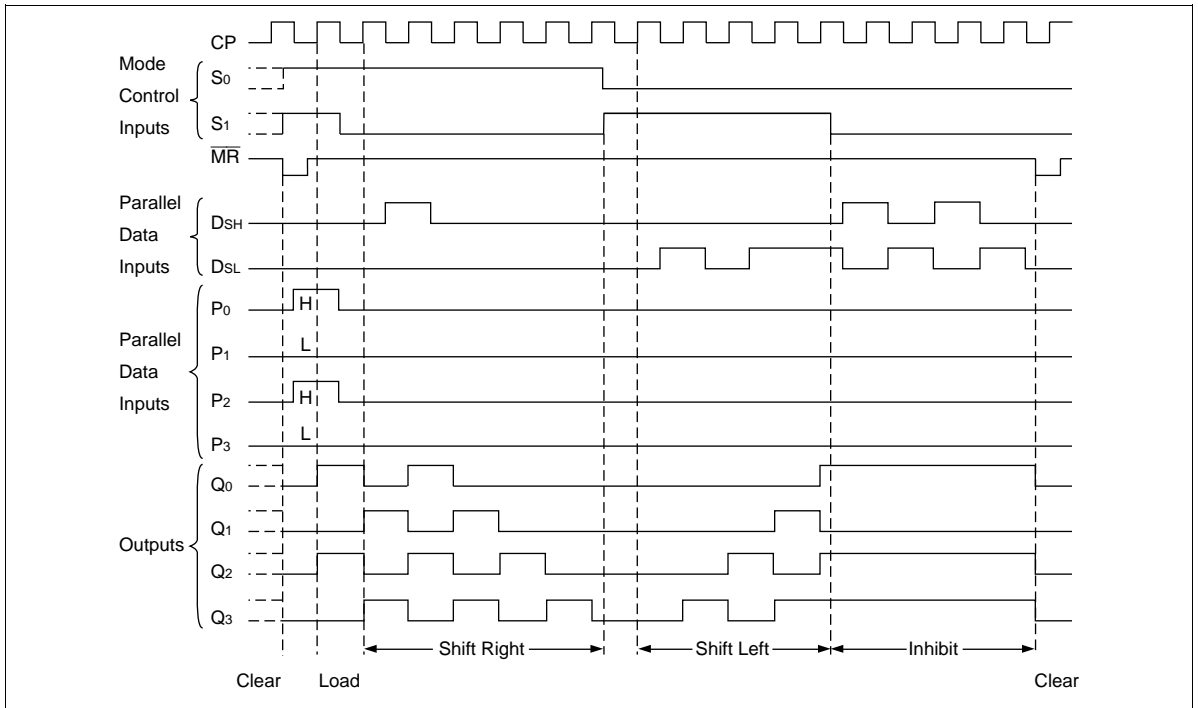
H : HIGH Voltage Level

L : LOW Voltage Level

$p_n$  ( $q_n$ ) : Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition

X : Immaterial

## Timing Diagram



## DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	$I_{CC}$	80	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = \text{Worst case}$
Maximum quiescent supply current	$I_{CC}$	8.0	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = 25^\circ C$

**AC Characteristics: HD74AC194**

Item	Symbol	V <sub>CC</sub> (V)*1	Ta = +25°C C <sub>L</sub> = 50 pF			Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f <sub>max</sub>	3.3	7.5	—	—	65	MHz	
		5.0	100	—	—	85		
Propagation delay CP to Q <sub>n</sub>	t <sub>PLH</sub>	3.3	1.0	—	13.0	1.0	15.0	ns
		5.0	1.0	—	10.0	1.0	11.5	
Propagation delay CP to Q <sub>n</sub>	t <sub>PHL</sub>	3.3	1.0	—	13.0	1.0	15.0	ns
		5.0	1.0	—	10.0	1.0	11.5	
Propagation delay MR to Q <sub>n</sub>	t <sub>PHL</sub>	3.3	1.0	—	10.5	1.0	12.5	ns
		5.0	1.0	—	8.0	1.0	9.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

**AC Operating Requirements: HD74AC194**

Item	Symbol	V <sub>CC</sub> (V)*1	Typ	Guaranteed Minimum		Unit
			Ta = +25°C C <sub>L</sub> = 50 pF			
Setup time, HIGH or LOW Pn or D <sub>SR</sub> or D <sub>SL</sub> to CP	t <sub>su</sub>	3.3	—	5.5	7.0	ns
		5.0	—	4.0	5.0	
Hold time, HIGH or LOW Pn or D <sub>SR</sub> or D <sub>SL</sub> to CP	t <sub>h</sub>	3.3	—	2.0	3.0	ns
		5.0	—	1.5	2.0	
Setup time, HIGH or LOW S <sub>n</sub> to CP	t <sub>su</sub>	3.3	—	6.0	7.5	ns
		5.0	—	4.5	5.5	
Hold time, HIGH or LOW S <sub>n</sub> to CP	t <sub>h</sub>	3.3	—	0.0	0.0	ns
		5.0	—	0.0	0.0	
Recovery time MR to CP	t <sub>rec</sub>	3.3	—	0.5	0.5	ns
		5.0	—	0.5	0.5	
Pulse width	t <sub>w</sub>	3.3	—	5.5	7.0	ns
		5.0	—	4.5	5.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

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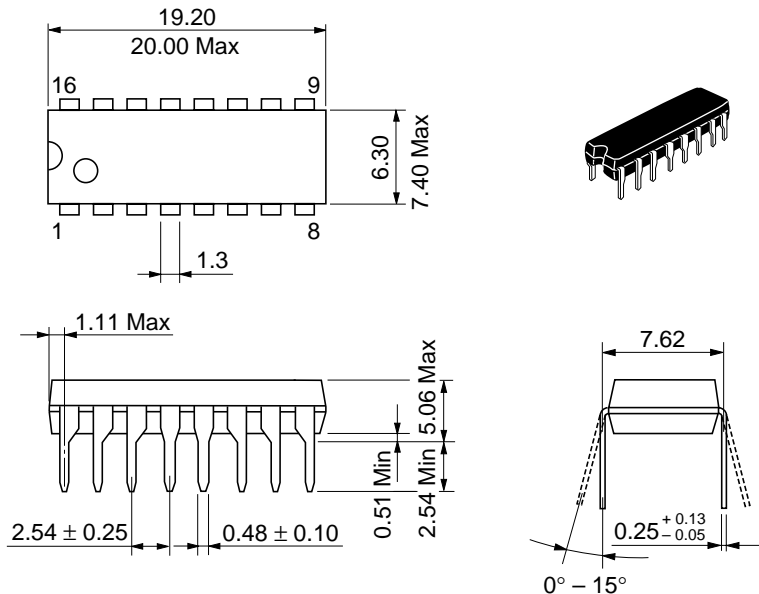
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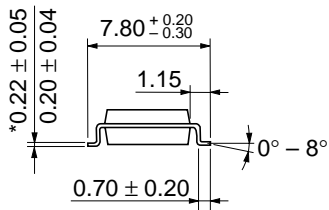
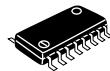
## Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	$C_{IN}$	4.5	pF	$V_{CC} = 5.5 \text{ V}$
Power dissipation capacitance	$C_{PD}$	100	pF	$V_{CC} = 5.0 \text{ V}$

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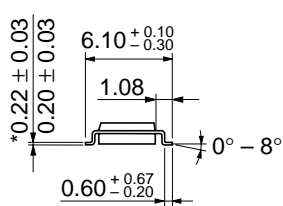
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
 Base material dimension

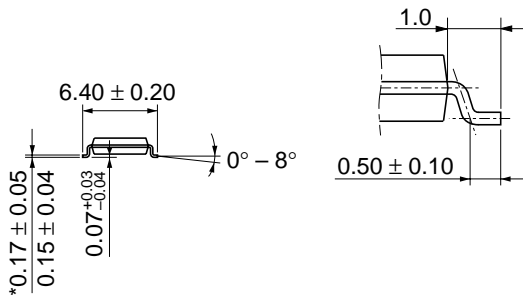
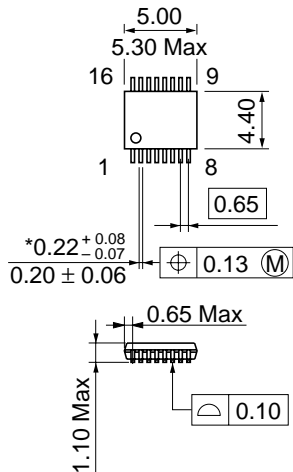
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g





\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



\*Dimension including the plating thickness  
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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