

# HD6305U0, HD63A05U0, HD63B05U0 CMOS MCU (Microcomputer Unit)

The HD6305U0 is a CMOS 8-bit single-chip MCU which is similar to the HD6305X MCU family. This version is upward compatible with the HD6805 family in respect to instructions. A CPU, a clock generator, a 2k-byte ROM, a 128-byte RAM, 31 I/O terminals, two timers, and a serial communication interface (SCI) are incorporated in the HD6305U0. As a result of CMOS technology, the HD6305U0 consumes much less power than NMOS counterparts. In addition, three low power dissipation modes (stop, wait and standby) which further decreases power consumption, are included in the HD6305U0.

Other notable features include enhanced instruction cycle of the main instructions and the use of three additional instructions to improve system throughput.

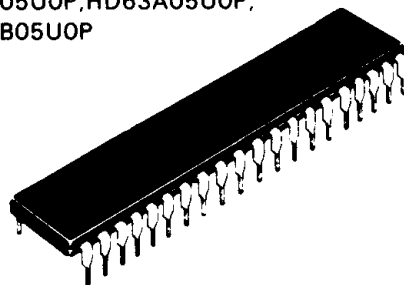
## ■ HARDWARE FEATURES

- CMOS 8-bit single-chip MCU
- 2048 bytes of ROM
- 128 bytes of RAM
- 31 bidirectional I/O terminals
- Two timers
  - 8-bit timer with a 7-bit prescaler (programmable prescaler; event counter)
  - 15-bit timer (commonly used with the SCI clock divider)
- On-chip serial interface circuit (synchronized with clock)
- Six interrupts (two external, two timer, one serial and one software)
- Low power dissipation modes
  - Wait. . . . . In this mode, the clock oscillator is on and the CPU halts but the timer/serial/interrupt function is operable. Also, all registers are held, except the I bit in the condition code register is cleared.
  - Stop. . . . . In this mode, the clock stops but the RAM data, I/O status and registers are held. Except the timer control register (bits 6 and 7) and the I bit of the condition code register.
  - Standby. . . . . In this mode, the clock stops, the RAM data is held, and the other internal condition is reset.
- Minimum instruction cycle time
  - HD6305U0 . . . . . 1  $\mu$ s (f = 1 MHz)
  - HD63A05U0 . . . . . 0.67  $\mu$ s (f = 1.5 MHz)
  - HD63B05U0 . . . . . 0.5  $\mu$ s (f = 2 MHz)
- Wide operating range
  - $V_{CC} = 3$  to 6V (f = 0.1 to 0.5 MHz)
  - HD6305U0 . . . . . f = 0.1 to 1 MHz  
( $V_{CC} = 5V \pm 10\%$ )
  - HD63A05U0 . . . . . f = 0.1 to 1.5 MHz  
( $V_{CC} = 5V \pm 10\%$ )
  - HD63B05U0 . . . . . f = 0.1 to 2 MHz  
( $V_{CC} = 5V \pm 10\%$ )
- System development fully supported by an emulator

## ■ SOFTWARE FEATURES

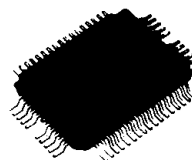
- Similar to HD6800
- Byte efficient instruction set
- Powerful bit manipulation instructions (Bit Set, Bit Clear, and Bit Test and Branch usable for all RAM bits and all I/O terminals)

HD6305U0P, HD63A05U0P,  
HD63B05U0P



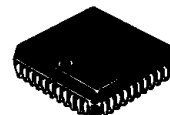
(DP-40)

HD6305U0F, HD63A05U0F,  
HD63B05U0F



(FP-54)

HD6305U0CP,  
HD63A05U0CP,  
HD63B05U0CP



(CP-44)

## ■ PROGRAM DEVELOPMENT SUPPORT TOOLS

- Cross assembler software for IBM PCs and compatibles
- In circuit emulator for use with IBM PCs and compatibles





# HD6305U0, HD63A05U0, HD63B05U0

## ■ ABSOLUTE MAXIMUM RATINGS

| Item                  | Symbol    | Value                 | Unit |
|-----------------------|-----------|-----------------------|------|
| Supply voltage        | $V_{CC}$  | -0.3 ~ +7.0           | V    |
| Input voltage         | $V_{in}$  | -0.3 ~ $V_{CC} + 0.3$ | V    |
| Operating temperature | $T_{opr}$ | 0 ~ +70               | °C   |
| Storage temperature   | $T_{stg}$ | -55 ~ +150            | °C   |

[NOTE] These products have a protection circuit in their input terminals against high electrostatic voltage or high electric fields. Notwithstanding, be careful not to apply any voltage higher than the absolute maximum rating to these high input impedance circuits. To assure normal operation, we recommended  $V_{in}, V_{out}: V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

## ■ ELECTRICAL CHARACTERISTICS

• DC Characteristics ( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = GND$  and  $T_a = 0 \sim +70^\circ C$  unless otherwise specified)

| Item                  | Symbol   | Test condition | min                               | typ | max            | Unit    |         |
|-----------------------|--|----------------|-----------------------------------|-----|----------------|---------|---------|
| Input voltage "High"  | RES, STBY  | $V_{IH}$       | $V_{CC} - 0.5$                    | -   | $V_{CC} + 0.3$ | V       |         |
|                       | EXTAL  |                | $V_{CC} \times 0.7$               | -   | $V_{CC} + 0.3$ | V       |         |
|                       | Others   |                | 2.0                               | -   | $V_{CC} + 0.3$ | V       |         |
| Input voltage "Low"   | All Inputs   | $V_{IL}$       | -0.3                              | -   | 0.8            | V       |         |
| Current * dissipation | Operating  | $I_{CC}$       | $f = 1MHz^{**}$                   | -   | 5              | 10      | mA      |
|                       | Wait   |                |                                   | -   | 2              | 5       | mA      |
|                       | Stop   |                |                                   | -   | 2              | 10      | $\mu A$ |
|                       | Standby  |                |                                   | -   | 2              | 10      | $\mu A$ |
| Input leakage current | TIMER, INT, STBY   | $ I_{IL} $     | -                                 | -   | 1              | $\mu A$ |         |
| Three-state current   | $A_0 \sim A_7, B_0 \sim B_7, C_0 \sim C_7, D_0 \sim D_6$ | $ I_{TSI} $    | $V_{in} = 0.5 \sim V_{CC} - 0.5V$ | -   | -              | 1       | $\mu A$ |
| Input capacity        | All terminals  | $C_{in}$       | $f = 1MHz, V_{in} = 0V$           | -   | -              | 12      | pF      |

\*  $V_{IHmin} = V_{CC} - 1.0V, V_{ILmax} = 0.8V$

\*\* The value at  $f = xMHz$  can be calculated by the following equation:  $I_{CC}(f = xMHz) = I_{CC}(f = 1MHz)$  multiplied by  $x$



# HD6305U0, HD63A05U0, HD63B05U0

● AC Characteristics ( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = GND$  and  $T_a = 0 \sim +70^\circ C$  unless otherwise specified)

| Item                             | Symbol     | Test condition                                | HD6305U0        |     |     | HD63A05U0       |     |     | HD63B05U0       |     |     | Unit      |
|----------------------------------|------------|---|-----------------|-----|-----|-----------------|-----|-----|-----------------|-----|-----|-----------|
|                                  |            |   | min             | typ | max | min             | typ | max | min             | typ | max |           |
| Clock frequency                  | $f_{cl}$   |   | 0.4             | —   | 4   | 0.4             | —   | 6   | 0.4             | —   | 8   | MHz       |
| Cycle time                       | $t_{cyc}$  |   | 1.0             | —   | 10  | 0.666           | —   | 10  | 0.5             | —   | 10  | $\mu s$   |
| $\overline{INT}$ pulse width     | $t_{1WL}$  |   | $t_{cyc} + 250$ | —   | —   | $t_{cyc} + 200$ | —   | —   | $t_{cyc} + 200$ | —   | —   | ns        |
| $\overline{INT2}$ pulse width    | $t_{1WL2}$ |   | $t_{cyc} + 250$ | —   | —   | $t_{cyc} + 200$ | —   | —   | $t_{cyc} + 200$ | —   | —   | ns        |
| $\overline{RES}$ pulse width     | $t_{RWL}$  |   | 5               | —   | —   | 5               | —   | —   | 5               | —   | —   | $t_{cyc}$ |
| TIMER pulse width                | $t_{TWL}$  |   | $t_{cyc} + 250$ | —   | —   | $t_{cyc} + 200$ | —   | —   | $t_{cyc} + 200$ | —   | —   | ns        |
| Oscillation start time (crystal) | $t_{OSC}$  | $C_L = 22pF \pm 20\%$<br>$R_s = 60\Omega$ max | —               | —   | 20  | —               | —   | 20  | —               | —   | 20  | ms        |
| Reset delay time                 | $t_{RHL}$  | External cap. $2.2\mu F$                      | 80              | —   | —   | 80              | —   | —   | 80              | —   | —   | ms        |

● Port Electrical Characteristics ( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = GND$  and  $T_a = 0 \sim +70^\circ C$  unless otherwise specified)

| Item                  | Symbol     | Test condition                    | min            | typ | max            | Unit    |
|-----------------------|------------|-----------------------------------|----------------|-----|----------------|---------|
| Output voltage "High" | $V_{OH}$   | $I_{OH} = -200\mu A$              | 2.4            | —   | —              | V       |
|                       |            | $I_{OH} = -10\mu A$               | $V_{CC} - 0.7$ | —   | —              | V       |
| Output voltage "Low"  | $V_{OL}$   | $I_{OL} = 1.6mA$                  | —              | —   | 0.55           | V       |
| Input voltage "High"  | $V_{IH}$   |                                   | 2.0            | —   | $V_{CC} + 0.3$ | V       |
| Input voltage "Low"   | $V_{IL}$   |                                   | -0.3           | —   | 0.8            | V       |
| Input leakage current | $ I_{IL} $ | $V_{in} = 0.5 \sim V_{CC} - 0.5V$ | —              | —   | 1              | $\mu A$ |

● SCI Timing ( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = GND$  and  $T_a = 0 \sim +70^\circ C$  unless otherwise specified)

| Item                   | Symbol     | Test Condition   | HD6305U0 |     |       | HD63A05U0 |     |       | HD63B05U0 |     |       | Unit    |
|------------------------|------------|------------------|----------|-----|-------|-----------|-----|-------|-----------|-----|-------|---------|
|                        |            |                  | min      | typ | max   | min       | typ | max   | min       | typ | max   |         |
| Clock Cycle            | $t_{Scyc}$ | Fig. 1<br>Fig. 2 | 1        | —   | 32768 | 0.67      | —   | 21845 | 0.5       | —   | 16384 | $\mu s$ |
| Data Output Delay Time | $t_{TXD}$  |                  | —        | —   | 250   | —         | —   | 250   | —         | —   | 250   | ns      |
| Data Set-up Time       | $t_{SRX}$  |                  | 200      | —   | —     | 200       | —   | —     | 200       | —   | —     | ns      |
| Data Hold Time         | $t_{HRX}$  |                  | 100      | —   | —     | 100       | —   | —     | 100       | —   | —     | ns      |



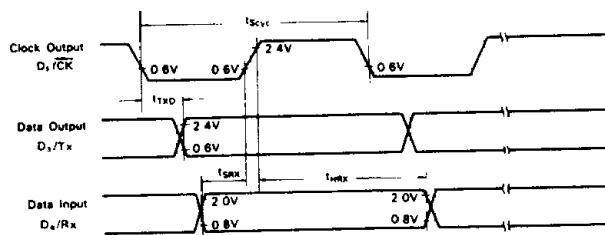


Figure 1 SCI Timing (Internal Clock)

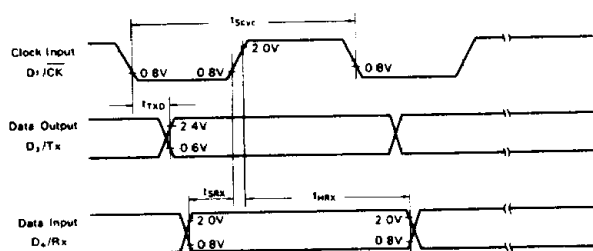
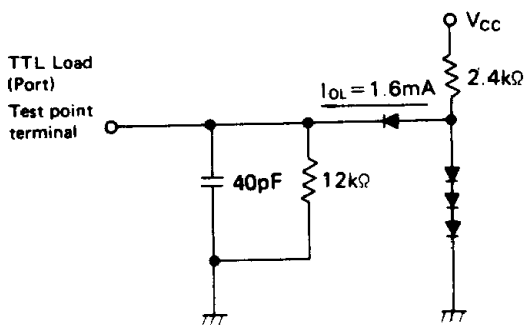


Figure 2 SCI Timing (External Clock)



- [NOTES] 1. The load capacitance includes stray capacitance caused by the probe, etc.  
 2. All diodes are 1S2074 (H).

Figure 3 Test Load

## DESCRIPTION OF TERMINAL FUNCTIONS

The input and output signals of the HD6305U0 are described here.

### V<sub>CC</sub>, V<sub>SS</sub>

Voltage is applied to the HD6305U0 through these two terminals. V<sub>CC</sub> is 5.0V ± 10%, while V<sub>SS</sub> is grounded.

### INT, INT<sub>2</sub>

External interrupt request inputs to the HD6305U0. For details, refer to "INTERRUPTS". The INT<sub>2</sub> terminal is also used as the port D<sub>6</sub> terminal.

### XTAL, EXTAL

These terminals provide input to the on-chip clock circuit. A crystal oscillator (AT cut, 2.0 to 8.0 MHz) or ceramic filter is connected to the terminal. Refer to "INTERNAL OSCILLATOR" for using these input terminals.

### TIMER

This is an input terminal for event counter. Refer to "TIMER" for details.

### RES

Used to reset the MCU. Refer to "RESET" for details.

### NUM

This terminal is not intended for user applications. It must be grounded to V<sub>SS</sub>.

### Input/Output Terminals (A<sub>0</sub> ~ A<sub>7</sub>, B<sub>0</sub> ~ B<sub>7</sub>, C<sub>0</sub> ~ C<sub>7</sub>, D<sub>0</sub> ~ D<sub>6</sub>)

These 31 terminals consist of three 8-bit I/O ports (A, B and C) and a 7-bit I/O port D. Each of these can be used as an input or output terminal on a bit basis through program control of the data direction register (DDR). For details, refer to "I/O PORTS."

Since port D<sub>6</sub> is also used for the INT<sub>2</sub> input, in order to use port D<sub>6</sub> as an I/O port, the INT<sub>2</sub> interrupt mask bit in the miscellaneous register should be set to "1" to disable the INT<sub>2</sub> input.

### STBY

This terminal is used to place the MCU into the standby mode. With STBY at "Low" level, the oscillation stops and the internal condition is reset. For details, refer to "STANDBY MODE."

The terminals described in the following are I/O pins for serial communication interface (SCI). They are also used as ports D<sub>3</sub>, D<sub>4</sub> and D<sub>5</sub>. For details, refer to "SERIAL COMMUNICATION INTERFACE."

### CK (D<sub>3</sub>)

Used to input or output clocks for serial operation.

### Rx (D<sub>4</sub>)

Used to receive serial data.

### Tx (D<sub>5</sub>)

Used to transmit serial data.

### MEMORY MAP

The memory map of the HD6305U0 MCU is shown in Fig. 4. During interrupt processing, the contents of the MCU registers are saved into the stack in the sequence shown in Fig. 5. This saving begins with the lower byte (PCL) of the program counter. Then the value of the stack pointer is decremented and the higher byte (PCH) of the program counter, index register (X), accumulator (A) and condition code register (CCR) are stacked in that order. In a subroutine call, only the contents of the program counter (PCH and PCL) are stacked.

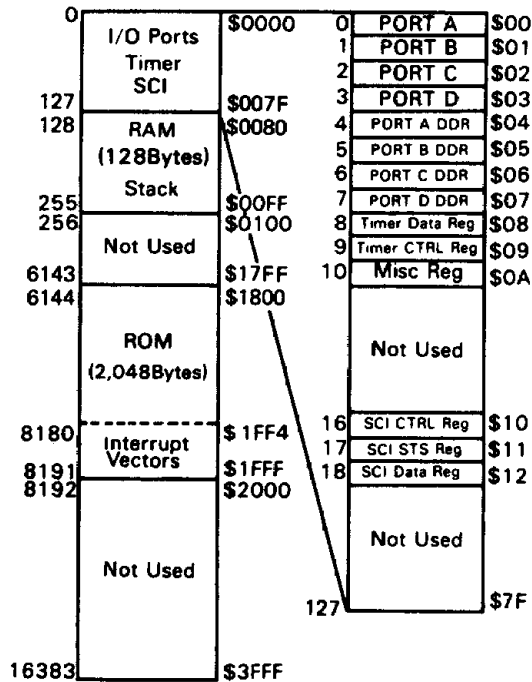
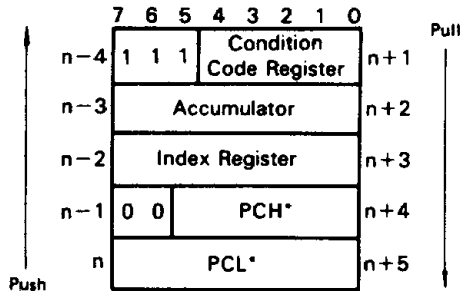


Figure 4 Memory Map of HD6305U0 MCU



\* In a subroutine call, only PCL and PCH are stacked.

Figure 5 Sequence of Interrupt Stacking

REGISTERS

There are five registers which the programmer can operate.

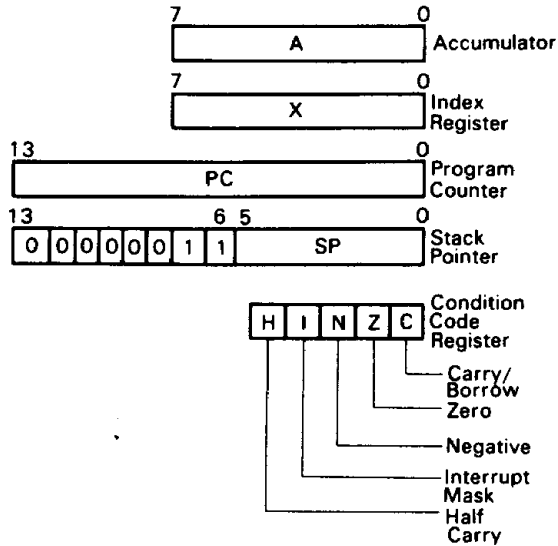


Figure 6 Programming Model

Accumulator (A)

This accumulator is a general purpose 8-bit register which holds operands or the result of arithmetic operation or data processing.

Index Register (X)

The index register is an 8-bit register, and is used for index addressing mode. Each of the addresses contained in the register consists of 8 bits which, combined with an offset value, provides an effective address.

In the case of a read/modify/write instruction, the index register can be used like an accumulator to hold operation data or the result of operation.

If not used in the index addressing mode, the register can be used to store data temporarily.

Program Counter (PC)

The program counter is a 14-bit register that contains the address of the next instruction to be executed.

Stack Pointer (SP)

The stack pointer is a 14-bit register that indicates the address of the next stacking space. Just after reset, the stack pointer is set at address \$00FF. It is decremented when data is pushed, and incremented when pulled. The upper 8 bits of the stack pointer are fixed to 00000011. During the MCU being reset or during a reset stack pointer (RSP) instruction, the pointer is set to address \$00FF. Since a subroutine or interrupt can use space up to address \$00C1 for stacking, the subroutine can be used up to 31 levels and the interrupt up to 12 levels.

Condition Code Register (CCR)

The condition code register is a 5-bit register, each bit indicating the result of the instruction just executed. The bits can be individually tested by conditional branch instructions. The CCR bits are as follows:

Half Carry (H): Used to indicate that a carry occurred between bits 3 and 4 during an arithmetic operation (ADD, ADC).

Interrupt (I): Setting this bit causes all interrupts, except a software interrupt, to be masked. If an interrupt occurs with the bit I set, it is latched. It will be processed the instant the interrupt mask bit is reset. (More specifically, it will enter the interrupt processing routine after the instruction following the CLI has been executed.)

- Negative (N): Used to indicate that the result of the most recent arithmetic operation, logical operation or data processing is negative (bit 7 is logic "1").
- Zero (Z): Used to indicate that the result of the most recent arithmetic operation, logical operation or data processing is zero.
- Carry/  
Borrow (C): Represents a carry or borrow that occurred in the most recent arithmetic operation. This bit is also affected by the Bit Test and Branch instruction, a shift instruction and a Rotate instruction.

■ INTERRUPT

There are six different types of interrupt: external interrupts ( $\overline{INT}$ ,  $\overline{INT}_2$ ), internal timer interrupts (TIMER,  $TIMER_2$ ), serial interrupt (SCI) and interrupt by an instruction (SWI).

Of these six interrupts, the  $\overline{INT}_2$  and TIMER or the SCI and  $TIMER_2$  generate the same vector address, respectively. Although, a different vector address is generated for a timer interrupt during the wait mode, as shown in Table 1.

When an interrupt occurs, the program in progress stops and then the CPU status is saved onto the stack. And then, the interrupt mask bit (I) of the condition code register is set and the start address of the interrupt processing routine is obtained from a particular interrupt vector address. Then the interrupt routine starts from the start address. System can exit from the interrupt routine by a RTI instruction. When this instruction is executed, the CPU status before the interrupt (saved onto the stack) is pulled and the CPU restarts the sequence with the instruction next to the one at which the interrupt occurred. Table 1 lists the priority of interrupts and their vector addresses.

Table 1 Priority of Interrupts

| Priority | Interrupt                 | Vector Address |
|----------|---------------------------|----------------|
| 1        | $\overline{RES}$          | \$1FFE, \$1FFF |
| 2        | SWI                       | \$1FFC, \$1FFD |
| 3        | $\overline{INT}$          | \$1FFA, \$1FFB |
| 4        | TIMER/ $\overline{INT}_2$ | \$1FF8, \$1FF9 |
| 5        | TIMER (WAIT)              | \$1FF6, \$1FF7 |
| 6        | SCI/ $TIMER_2$            | \$1FF4, \$1FF5 |

A flowchart of the interrupt sequence is shown in Fig. 7. A block diagram of the interrupt request source is shown in Fig. 8.

In the block diagram of Fig. 8, the external interrupt  $\overline{INT}_2$  is a falling edge trigger input, whereas, the external interrupt  $\overline{INT}$  can be configured as a falling edge trigger input or a combination of falling edge and low level trigger input, depending on the status of bit 5 in the miscellaneous register (MR). When an interrupt request is detected at the  $\overline{INT}_2$  or  $\overline{INT}$  inputs, an interrupt re-

quest is generated and latched. The  $\overline{INT}$  interrupt request is automatically cleared if jumping is made to the  $\overline{INT}$  processing routine. Meanwhile, the  $\overline{INT}_2$  request is cleared if "0" is written in bit 7 of the miscellaneous register.

For the external interrupts ( $\overline{INT}$ ,  $\overline{INT}_2$ ), internal timer interrupts (TIMER,  $TIMER_2$ ) and serial interrupt (SCI), each interrupt request is held, but not processed, if the I bit of the condition code register is set. Immediately after the I bit is cleared, the corresponding interrupt processing starts according to the priority.

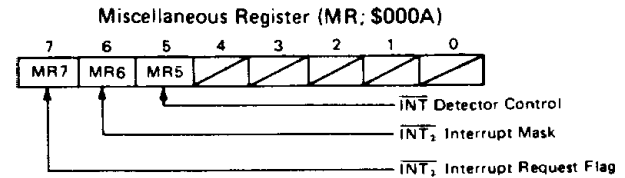
The  $\overline{INT}_2$  interrupt can be masked by setting bit 6 of the miscellaneous register; the TIMER interrupt by setting bit 6 of the timer control register; the SCI interrupt by setting bit 5 of the serial status register; and the  $TIMER_2$  interrupt by setting bit 4 of the serial status register.

The status of the  $\overline{INT}$  terminal can be tested by a BIL or BIH instruction. The  $\overline{INT}$  falling edge and falling edge/low level detector circuit and its latching circuit are independent of testing by these instructions. This is also true with the status of the  $\overline{INT}_2$  terminal.

● Miscellaneous Register (MR; \$000A)

The external interrupt  $\overline{INT}_2$  and the TIMER interrupt have identical interrupt vector addresses, as shown in Table 1. For this reason, bits 6 and 7 of a special register called the miscellaneous register (MR; \$000A) are available to control the  $\overline{INT}_2$  interrupt. Moreover, bit 5 of the MR controls the sensing mode for the  $\overline{INT}$  interrupt detector (falling edge detector or falling edge/low level detector).

Bit 7 of the MR is the  $\overline{INT}_2$  interrupt request flag. When a falling edge is detected at the  $\overline{INT}_2$  terminal, bit 7 is set to "1". Then the interrupt routine software (vector addresses: \$1FF8, \$1FF9) checks bit 7 to see if an  $\overline{INT}_2$  interrupt occurred. Bit 7 can be reset by software.



Bit 6 is the  $\overline{INT}_2$  interrupt mask bit. If this bit is set to "1", then the  $\overline{INT}_2$  interrupt is disabled. Both read and write are possible with bit 7, but "1" cannot be written in this bit by software. In other words, an  $\overline{INT}_2$  interrupt request by software is not possible.

Bit 5 is the control bit for  $\overline{INT}$  interrupt detection. If this bit is reset to "0", the detection logic will detect a falling edge. When this bit is set to "1", the detection logic will detect a falling edge or a low level.

When reset, bit 7 is cleared to "0", bit 6 is set to "1" and bit 5 is cleared to "0".

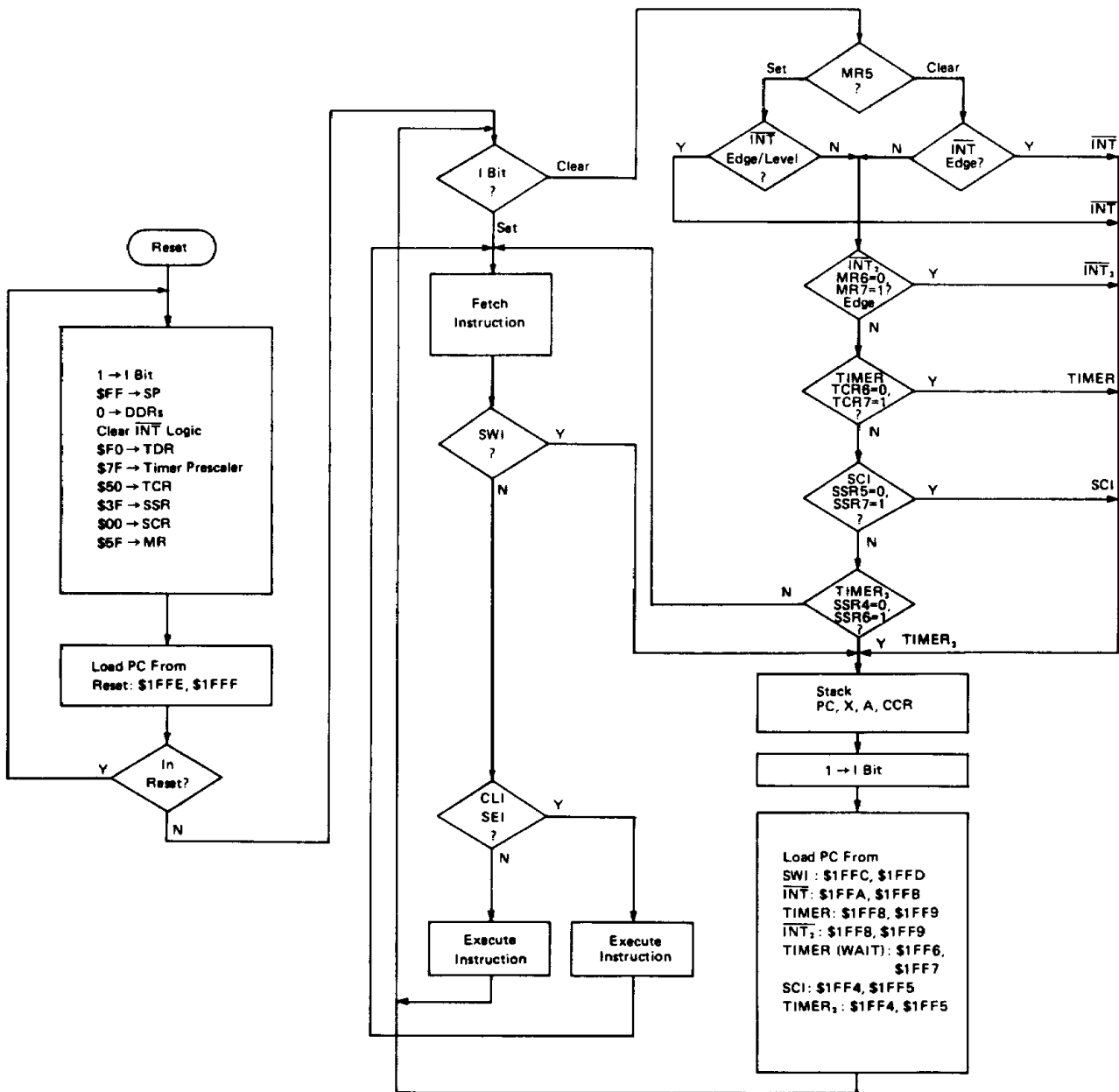


Figure 7 Interrupt Flowchart



■ **TIMER**

Figure 9 shows an MCU timer block diagram. The timer data register is loaded by software and, upon receipt of a clock input, begins to count down. When the timer data register (TDR) becomes "0", the timer interrupt request bit (bit 7) in the timer control register is set. In response to the interrupt request, the MCU saves its status into the stack and fetches the timer interrupt routine addresses \$1FF8 and \$1FF9 (or \$1FF6 and \$1FF7 when the timer interrupt occurs during the wait mode) and executes the interrupt routine. The timer interrupt can be masked by setting the timer interrupt mask bit (bit 6) in the timer control register. The mask bit (I) in the condition code register can also mask the timer interrupt.

The source clock to the timer can be either an external signal from the timer input terminal or the internal E signal (the oscil-

lator clock divided by 4). If the E signal is used as the source, the clock input can be gated by the input to the timer input terminal.

Once the timer count has reached 0, it starts counting down with "FF". The count can be monitored whenever desired by reading the timer data register. This permits the program to know the length of time having passed after the occurrence of a timer interrupt, without disturbing the contents of the counter.

When the MCU is reset or placed in the stop mode, the timer data register (TDR) is initialized to \$F0. The timer interrupt request bit (bit 7) then is cleared and the timer interrupt mask bit (bit 6) is set.

To clear the timer interrupt request bit (bit 7), it is necessary to write "0" in that bit.

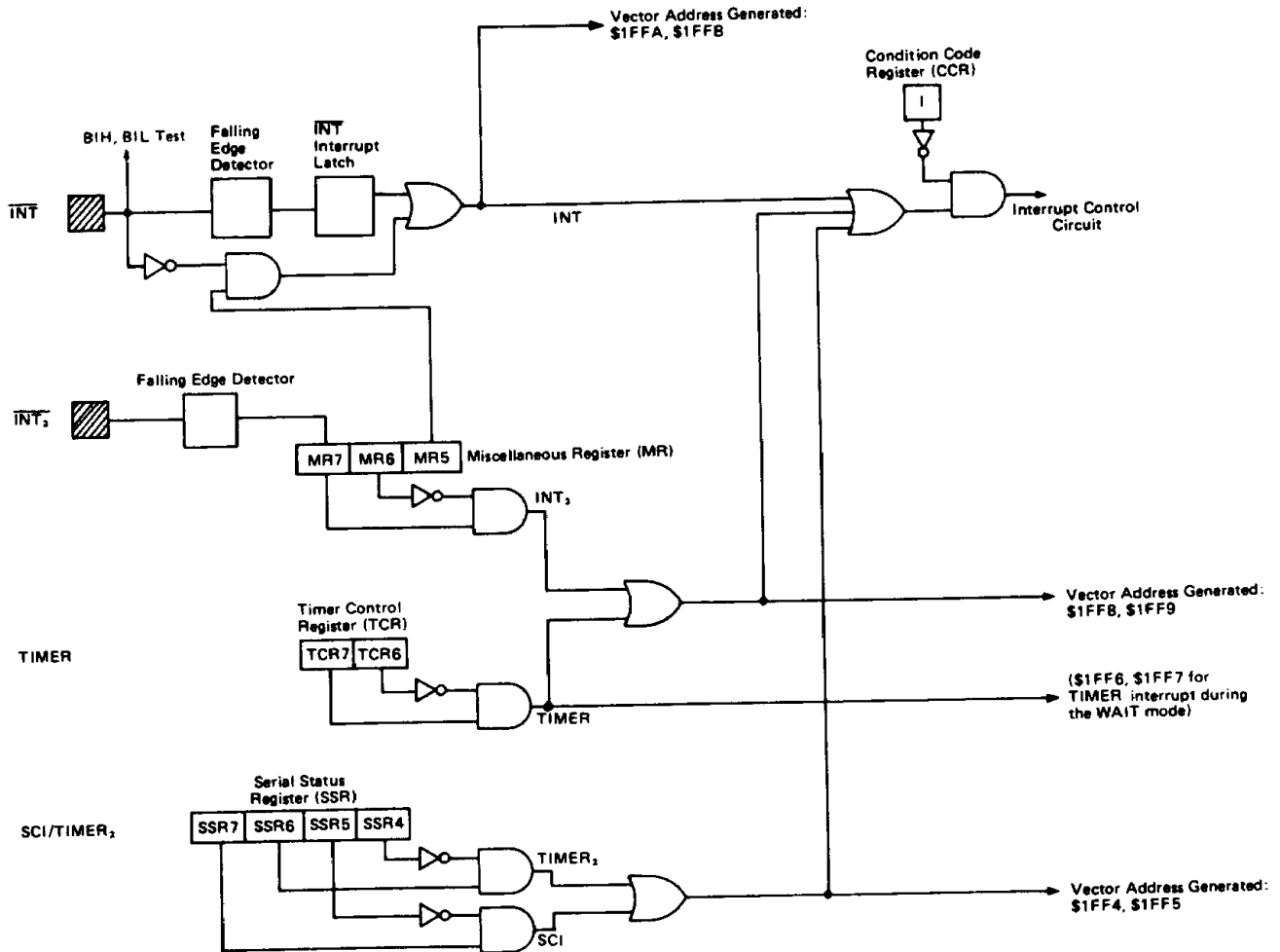


Figure 8 Interrupt Request Generation Circuitry

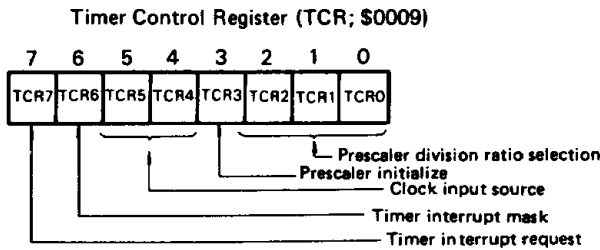
# HD6305U0, HD63A05U0, HD63B05U0

|      |                         |
|------|-------------------------|
| TCR7 | Timer interrupt request |
| 0    | Absent                  |
| 1    | Present                 |
| TCR6 | Timer interrupt mask    |
| 0    | Enabled                 |
| 1    | Disabled                |

● **Timer Control Register (TCR; \$0009)**

Selection of a clock source, selection of a prescaler frequency division ratio, and a timer interrupt can be controlled by the timer control register (TCR; \$0009).

For the selection of a clock source, any one of the four modes (see Table 2) can be selected by bits 5 and 4 of the timer control register (TCR).



After reset, the TCR is initialized to "E under timer terminal control" (bit 5 = 0, bit 4 = 1). If the timer terminal is "1", the counter starts counting down with "\$F0" immediately after reset.

When "1" is written in bit 3, the prescaler is initialized to "\$7F". This bit always shows "0" when read.

Table 2 Clock Source Selection

| TCR   |       | Clock input source                |
|-------|-------|-----------------------------------|
| Bit 5 | Bit 4 |                                   |
| 0     | 0     | Internal clock E                  |
| 0     | 1     | E under TIMER terminal control    |
| 1     | 0     | No clock input (counting stopped) |
| 1     | 1     | Event input from TIMER terminal   |

A prescaler division ratio is selected by the combination of three bits (bits 0, 1 and 2) of the timer control register (see Table 3). There are eight different division ratios: +1, +2, +4, +8, +16, +32, +64 and +128. After reset, the TCR is set to the +1 mode.

Table 3 Prescaler Division Ratio Selection

| TCR   |       |       | Prescaler division ratio |
|-------|-------|-------|--------------------------|
| Bit 2 | Bit 1 | Bit 0 |                          |
| 0     | 0     | 0     | ÷1                       |
| 0     | 0     | 1     | ÷2                       |
| 0     | 1     | 0     | ÷4                       |
| 0     | 1     | 1     | ÷8                       |
| 1     | 0     | 0     | ÷16                      |
| 1     | 0     | 1     | ÷32                      |
| 1     | 1     | 0     | ÷64                      |
| 1     | 1     | 1     | ÷128                     |

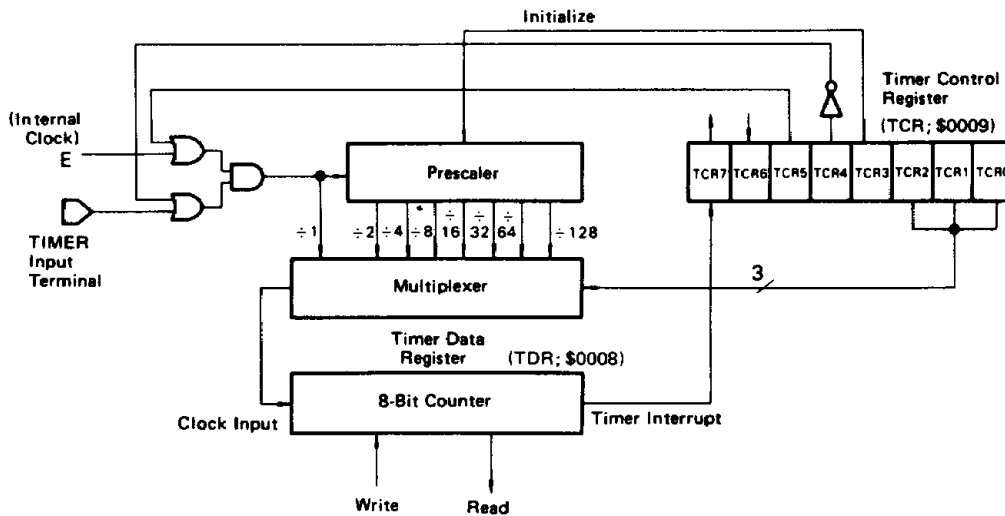


Figure 9 Timer Block Diagram

A timer interrupt is enabled when the timer interrupt mask bit is "0", and disabled when the bit is "1". When a timer inter-

rupt occurs, "1" is set in the timer interrupt request bit. This bit can be cleared by writing "0" in that bit.



## ■ SERIAL COMMUNICATION INTERFACE (SCI)

This interface is used for serial transmission or reception of 8-bit data. Sixteen transfer rates are available in the range from 1  $\mu$ s to approx. 32 ms (for oscillation at 4 MHz).

The SCI consists of three registers, one octal counter and one prescaler. (See Fig. 10.) SCI communicates with the CPU via the data bus, and with the outside world through bits 3, 4 and 5 of port D. Described below are the operations of each reg-

ister and data transfer.

### ● SCI Control Register (SCR; \$0010)

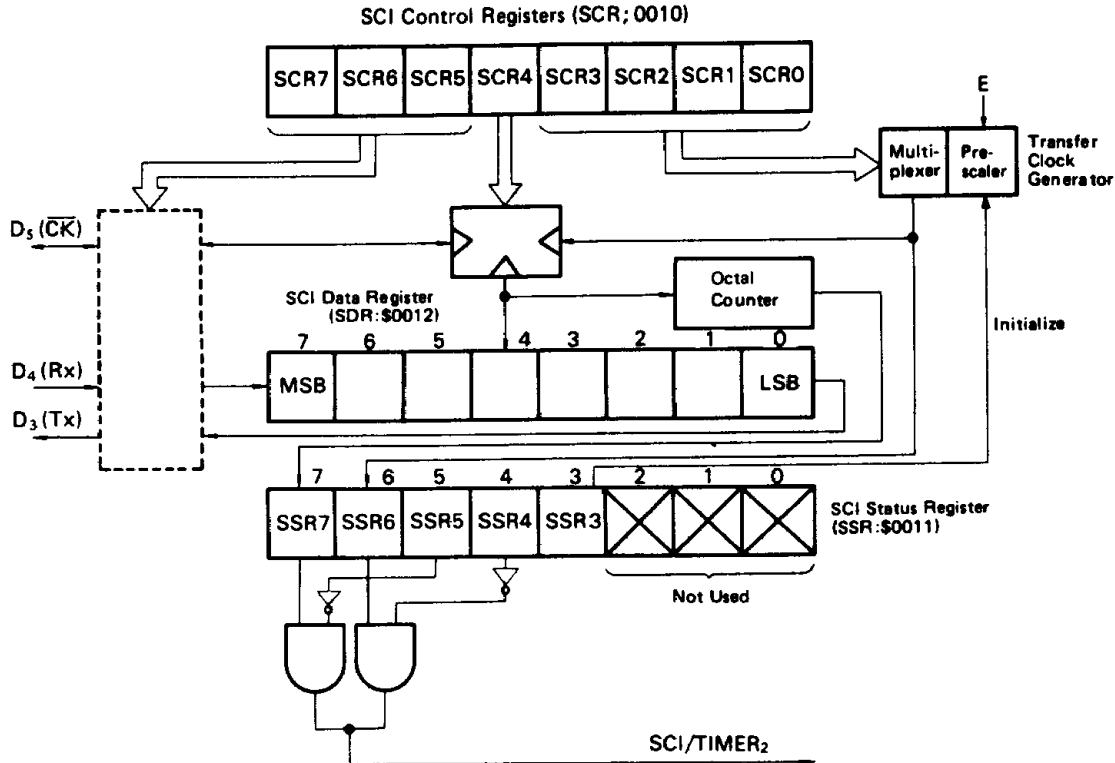
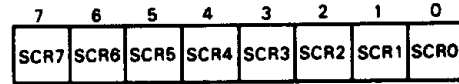


Figure 10 SCI Block Diagram

|      |                                 |
|------|---------------------------------|
| SCR7 | D <sub>3</sub> terminal         |
| 0    | Used as I/O terminal (by DDR)   |
| 1    | Serial data output (DDR output) |

|      |                               |
|------|-------------------------------|
| SCR6 | D <sub>4</sub> terminal       |
| 0    | Used as I/O terminal (by DDR) |
| 1    | Serial data input (DDR input) |

|      |      |              |                               |
|------|------|--------------|-------------------------------|
| SCR5 | SCR4 | Clock source | D <sub>5</sub> terminal       |
| 0    | 0    | —            | Used as I/O terminal (by DDR) |
| 0    | 1    | —            |                               |
| 1    | 0    | Internal     | Clock output (DDR output)     |
| 1    | 1    | External     | Clock input (DDR input)       |

#### Bit 7 (SCR7)

When this bit is set, the DDR corresponding to the D<sub>3</sub> becomes "1" and this terminal serves for output of SCI data. After reset, the bit is cleared to "0".

#### Bit 6 (SCR6)

When this bit is set, the DDR corresponding to the D<sub>4</sub> becomes "0" and this terminal serves for input of SCI data. After reset, the bit is cleared to "0".

#### Bits 5 and 4 (SCR5, SCR4)

These bits are used to select a clock source. After reset, the bits are cleared to "0".

#### Bits 3 ~ 0 (SCR3 ~ SCR0)

These bits are used to select a transfer clock rate. After reset, the bits are cleared to "0".

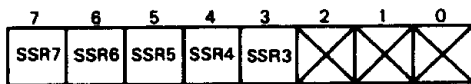
# HD6305U0, HD63A05U0, HD63B05U0

| SCR3 | SCR2 | SCR1 | SCR0 | Transfer clock rate |              |
|------|------|------|------|---------------------|--------------|
|      |      |      |      | 4.00 MHz            | 4.194 MHz    |
| 0    | 0    | 0    | 0    | 1 $\mu$ s           | 0.95 $\mu$ s |
| 0    | 0    | 0    | 1    | 2 $\mu$ s           | 1.91 $\mu$ s |
| 0    | 0    | 1    | 0    | 4 $\mu$ s           | 3.82 $\mu$ s |
| 0    | 0    | 1    | 1    | 8 $\mu$ s           | 7.64 $\mu$ s |
| ?    | ?    | ?    | ?    | ?                   | ?            |
| 1    | 1    | 1    | 1    | 32768 $\mu$ s       | 1/32 s       |

● **SCI Data Register (SDR; \$0012)**

A serial-parallel conversion register that is used for transfer of data.

● **SCI Status Register (SSR; \$0011)**



**Bit 7 (SSR7)**

Bit 7 is the SCI interrupt request bit which is set upon completion of transmitting or receiving 8-bit data. It is cleared when reset or data is written to or read from the SCI data register with the SCR5 = "1". The bit can also be cleared by writing "0" in it.

**Bit 6 (SSR6)**

Bit 6 is the  $TIMER_2$  interrupt request bit.  $TIMER_2$  is used commonly with the serial clock generator, and SSR6 is set each time the internal transfer clock falls. When reset, the bit is cleared. It also is cleared by writing "0" in it. (For details, see  $TIMER_2$ .)

**Bit 5 (SSR5)**

Bit 5 is the SCI interrupt mask bit which can be set or cleared by software. When it is "1", the SCI interrupt (SSR7) is masked. When reset, it is set to "1".

| SSR7 | SCI interrupt request |
|------|-----------------------|
| 0    | Absent                |
| 1    | Present               |

| SSR6 | $TIMER_2$ interrupt request |
|------|-----------------------------|
| 0    | Absent                      |
| 1    | Present                     |

| SSR5 | SCI interrupt mask |
|------|--------------------|
| 0    | Enabled            |
| 1    | Disabled           |

| SSR4 | $TIMER_2$ interrupt mask |
|------|--------------------------|
| 0    | Enabled                  |
| 1    | Disabled                 |

**Bit 4 (SSR4)**

Bit 4 is the  $TIMER_2$  interrupt mask bit which can be set or cleared by software. When the bit is "1", the  $TIMER_2$  interrupt (SSR6) is masked. When reset, it is set to "1".

**Bit 3 (SSR3)**

When "1" is written in this bit, the prescaler of the transfer clock generator is initialized. When read, the bit always is "0".

**Bits 2 ~ 0**

Not used.

● **Data Transmission**

By writing the desired control bits into the SCI control registers, a transfer rate and a source of transfer clock are determined and bits 3 and 5 of port D are set at the serial data output terminal and the serial clock terminal, respectively. The transmit data should be stored from the accumulator or index register into the SCI data register. The data written in the SCI data register is output from the  $D_7/Tx$  terminal, starting with the LSB, synchronously with the falling edge of the serial clock. (See Fig. 11.) When 8 bits of data have been transmitted, the interrupt request bit is set in bit 7 of the SCI status register. This request can be masked by setting bit 5 of the SCI status register. Once the data has been sent, the 8th bit data (MSB) stays at the  $D_7/Tx$  terminal. If an external clock source has been selected, the transfer rate determined by bits 0 ~ 3 of the SCI control register is ignored, and the  $D_7/\overline{CK}$  terminal is set as input. If the internal clock has been selected, the  $D_7/\overline{CK}$  terminal is set as output and clocks are output at the transfer rate selected by bits 0 ~ 3 of the SCI control register.

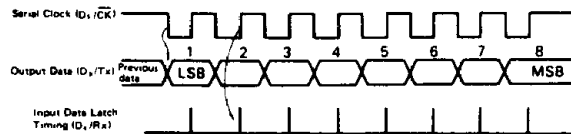


Figure 11 SCI Timing Chart

● **Data Reception**

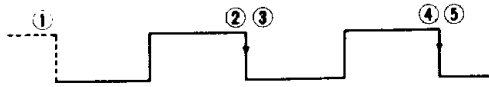
By writing the desired control bits into the SCI control register, a transfer rate and a source of transfer clock are determined and bits 4 and 5 of Port D are set at the serial data input terminal and the serial clock terminal, respectively. Then dummy-writing or -reading the SCI data register, the system is ready for receiving data. (This procedure is not needed for the second and subsequent data receptions. It must be taken only after resetting.)

The data from the  $D_7/Rx$  terminal is input to the SCI data register synchronously with the leading edge of the serial clock (see Fig. 11). When 8 bits of data have been received, the interrupt request bit is set in bit 7 of the SCI status register. This request can be masked by setting bit 5 of the SCI status register. If an external clock source has been selected, the transfer rate determined by bits 0 ~ 3 of the SCI control register is ignored and the data is received synchronously with the clock from the  $D_7/\overline{CK}$  terminal. If the internal clock has been selected, the  $D_7/\overline{CK}$  terminal is set as output and clocks are output at the transfer rate selected by bits 0 ~ 3 of the SCI control register.

●  **$TIMER_2$**

The SCI transfer clock generator can be used as a timer. The clock selected by bits 3 ~ 0 of the SCI control register (4  $\mu$ s ~ approx. 32 ms (for oscillation at 4 MHz)) is input to bit 6 of the SCI status register and the  $TIMER_2$  interrupt request bit is set at each falling edge of the clock. Since interrupt requests occur periodically,  $TIMER_2$  can be used as a reload counter or clock.





- ① : Transfer clock generator is reset and mask bit (bit 4 of SCI status register) is cleared.
- ②, ④ : TIMER<sub>2</sub> interrupt request
- ③, ⑤ : TIMER<sub>2</sub> interrupt request bit cleared

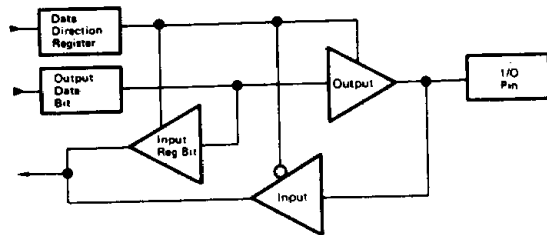
TIMER<sub>2</sub> is commonly used with the SCI transfer clock generator. If wanting to use TIMER<sub>2</sub> independently of the SCI, specify "External" (SCR5 = 1, SCR4 = 1) as the SCI clock source.

If "Internal" is selected as the clock source, reading or writing the SDR causes the prescaler of the transfer clock generator to be initialized.

### ■ I/O PORTS

There are 31 input/output terminals (ports A, B, C, D). Each I/O terminal can be selected for either input or output by the data direction register. More specifically, an I/O port will be input if "0" is written in the data direction register, and output if "1" is written in the data direction register. Port A, B, C or D reads latched data if it has been programmed as output, even with the output level being fluctuated by the output load. (See Fig. 12.)

When reset, the data direction register goes "0" and all the input/output terminals are used as input.



| Bit of data direction register | Bit of output data | Status of output | Input to CPU |
|--------------------------------|--------------------|------------------|--------------|
| 1                              | 0                  | 0                | 0            |
| 1                              | 1                  | 1                | 1            |
| 0                              | X                  | 3-state          | Pin          |

Figure 12 Input/Output Port (Ports A, B, C and D) Diagram

All input/output terminals are TTL compatible and CMOS compatible in respect of both input and output.

If I/O ports are not used, they should be connected to V<sub>SS</sub> via resistors. With none connected to these terminals, there is the possibility of power being consumed despite that they are not used.

### ■ RESET

The MCU can be reset either by external reset input ( $\overline{\text{RES}}$ ) or power-on reset. (See Fig. 13.) On power up, the reset input must be held "Low" for at least t<sub>OSC</sub> to assure that the internal oscillator is stabilized. A sufficient time of delay can be obtained by connecting a capacitance to the  $\overline{\text{RES}}$  input as shown in Fig. 14.

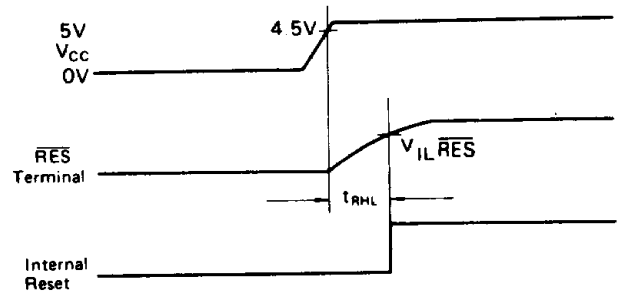


Figure 13 Power On and Reset Timing

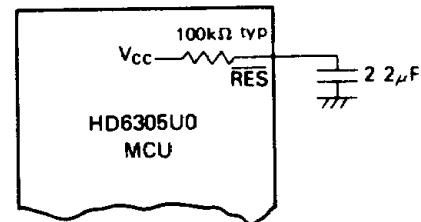


Figure 14 Input Reset Delay Circuit

### ■ INTERNAL OSCILLATOR

The internal oscillator circuit is designed to meet the requirement for minimum external configurations. It can be driven by connecting a crystal (AT cut 2.0 ~ 8.0 MHz) or ceramic oscillator between EXTAL and XTAL pins depending on the required oscillation frequency stability.

Three different terminal connections are shown in Fig. 15. Figs. 16 and 17 illustrate the specifications and typical arrangement of the crystal, respectively.

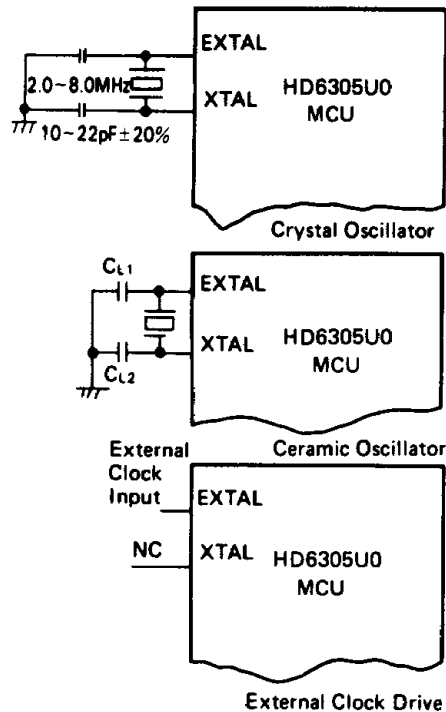


Figure 15 Internal Oscillator Circuit

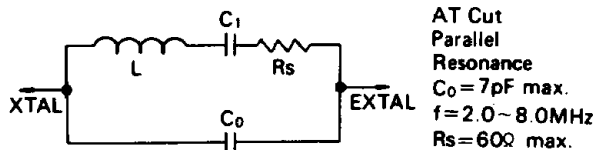
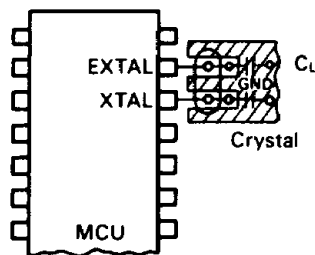


Figure 16 Parameters of Crystal



[NOTE] Use as short wirings as possible for connection of the crystal with the EXTERNAL and XTAL terminals. Do not allow these wirings to cross others.

Figure 17 Typical Crystal Arrangement

## ■ LOW POWER DISSIPATION MODE

The HD6305U0 has three low power dissipation modes: wait, stop and standby.

### ● Wait Mode

When WAIT instruction being executed, the MCU enters into the wait mode. In this mode, the oscillator stays active but the internal clock stops. The CPU stops but the peripheral functions — the timer and the serial communication interface — stay active. (NOTE: Once the system has entered the wait mode, the serial communication interface can no longer be retriggered.) In the wait mode, the registers (except the I bit of the condition code register which is cleared), RAM and I/O terminals hold their condition just before entering into the wait mode.

The escape from this mode can be done by interrupt ( $\overline{\text{INT}}$ ,  $\text{TIMER}/\overline{\text{INT}}_2$  or  $\text{SCI}/\text{TIMER}_2$ ),  $\overline{\text{RES}}$  or  $\text{STBY}$ . The  $\overline{\text{RES}}$  resets the MCU and the  $\text{STBY}$  brings it into the standby mode. (This will be mentioned later.)

When interrupt is requested to the CPU and accepted, the wait mode escapes, then the CPU is brought to the operation mode and vectors to the interrupt routine. If an interrupt other than the  $\overline{\text{INT}}$  (i.e.,  $\text{TIMER}/\overline{\text{INT}}_2$  or  $\text{SCI}/\text{TIMER}_2$ ) is masked by the timer control register, miscellaneous register or serial status register, there is no interrupt request to the CPU, so the wait mode cannot be released.

Fig. 18 shows a flowchart for the wait function.

### ● Stop Mode

When STOP instruction being executed, MCU enters into the stop mode. In this mode, the oscillator stops and the CPU and peripheral functions become inactive, but the RAM, registers (except bits 6 and 7 of the timer control register and the I bit of the condition code register) and I/O terminals hold their condition just before entering the stop mode. Bits 6 and 7 of the timer control register are initialized to "1" and "0", bits 7, 6, 5 and 4 of SCI status register are initialized "0", "0", "1", "1", respectively, and the I bit of the condition code register is cleared.

The escape from this mode can be done by an external interrupt ( $\overline{\text{INT}}$  or  $\overline{\text{INT}}_2$ ),  $\overline{\text{RES}}$  or  $\text{STBY}$ . The  $\overline{\text{RES}}$  resets the MCU and the  $\text{STBY}$  brings into the standby mode.

When interrupt is requested to the CPU and accepted, the stop mode escapes, then the CPU is brought to the operation mode and vectors to the interrupt routine. If the  $\overline{\text{INT}}_2$  interrupt is masked by the miscellaneous register, there is no interrupt request to the MCU, so the stop mode cannot be released.

Fig. 19 shows a flowchart for the stop function. Fig. 20 shows a timing chart of return to the operation mode from the stop mode.

For releasing from the stop mode by an interrupt, oscillation starts upon input of the interrupt and, after the internal delay time for stabilized oscillation, the CPU becomes active. For re-starting by  $\overline{\text{RES}}$ , oscillation starts when the  $\overline{\text{RES}}$  goes "0" and the CPU restarts when the  $\overline{\text{RES}}$  goes "1". The duration of  $\overline{\text{RES}} = "0"$  must exceed  $t_{\text{osc}}$  to assure stabilized oscillation.

### ● Standby Mode

The MCU enters into the standby mode when the  $\overline{\text{STBY}}$  terminal goes "Low". In this mode, all operations stop and the internal condition is reset but the contents of the RAM are hold. The I/O terminals turn to high-impedance state. The standby mode should escape by bringing  $\overline{\text{STBY}}$  "High". The CPU must be restarted by reset. The timing of input signals at the  $\overline{\text{RES}}$  and  $\overline{\text{STBY}}$  terminals is shown in Fig. 21.

Table 4 lists the status of each parts of the MCU in each low power dissipation modes. Transitions between each mode are shown in Fig. 22.

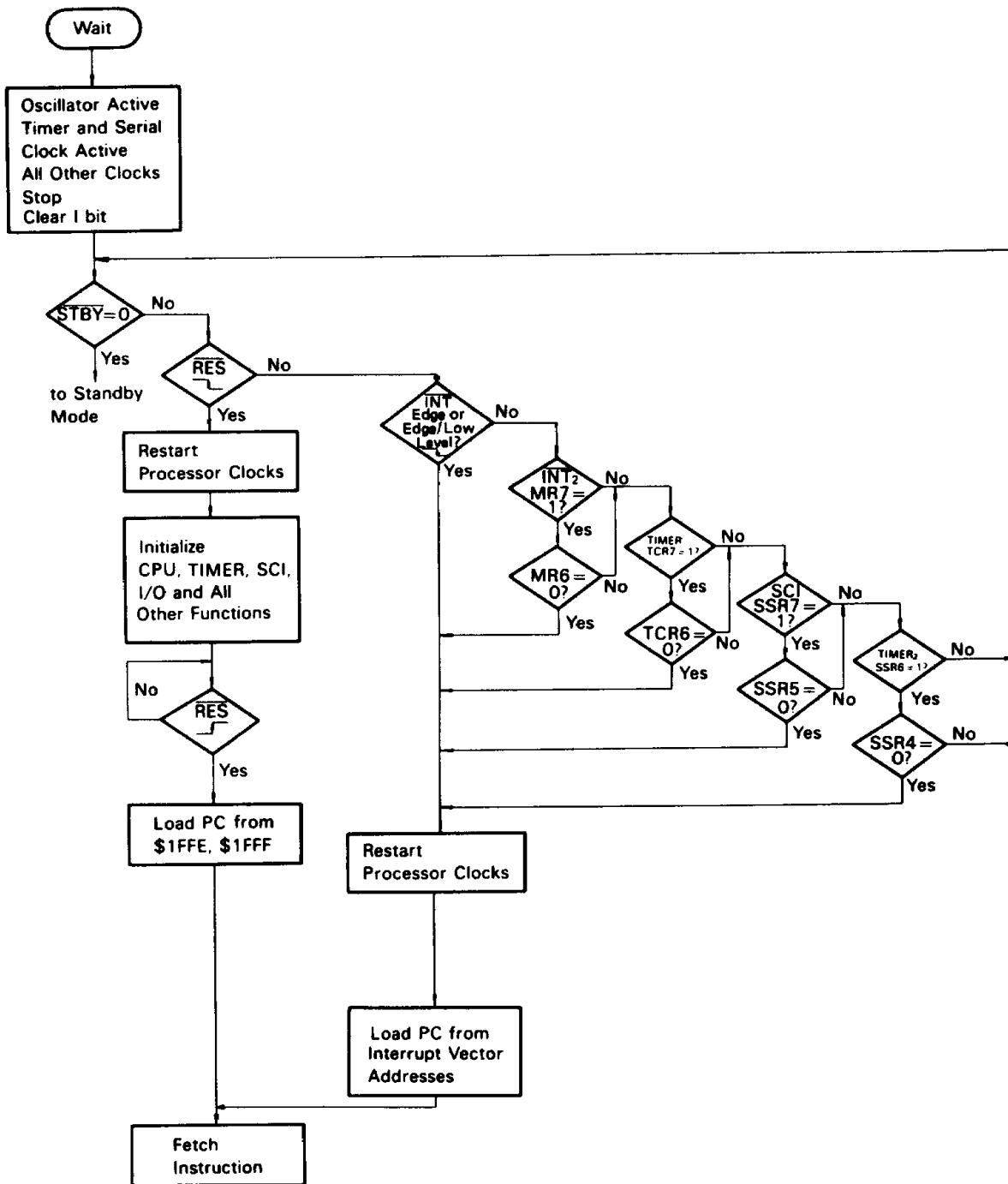


Figure 18 Wait Mode Flowchart

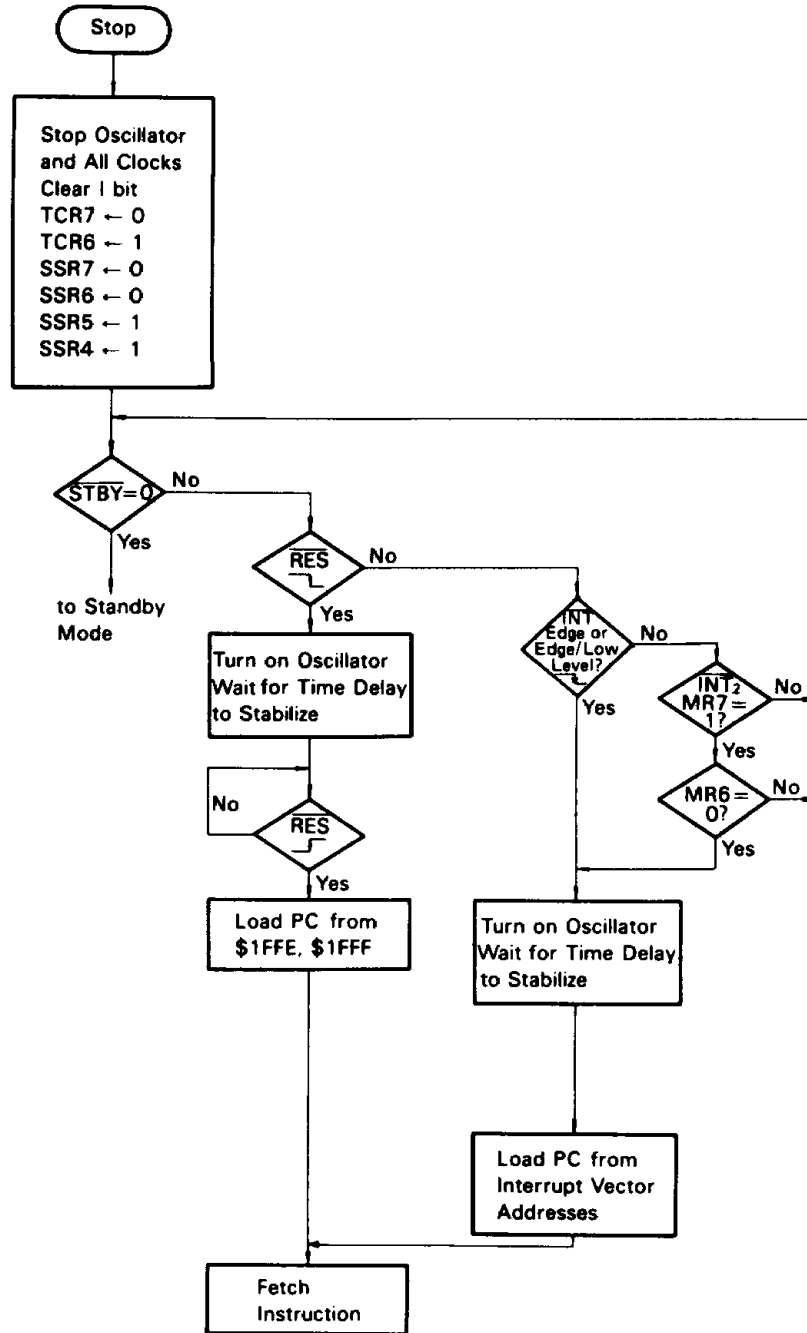


Figure 19 Stop Mode Flowchart



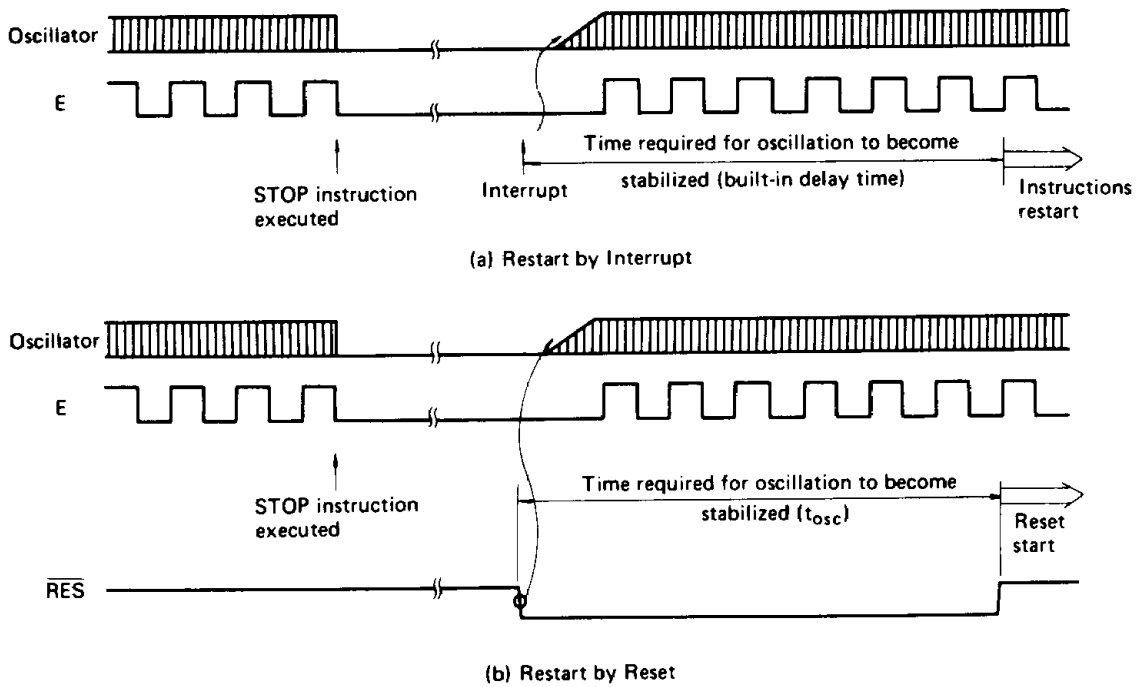


Figure 20 Timing Chart of Releasing from Stop Mode

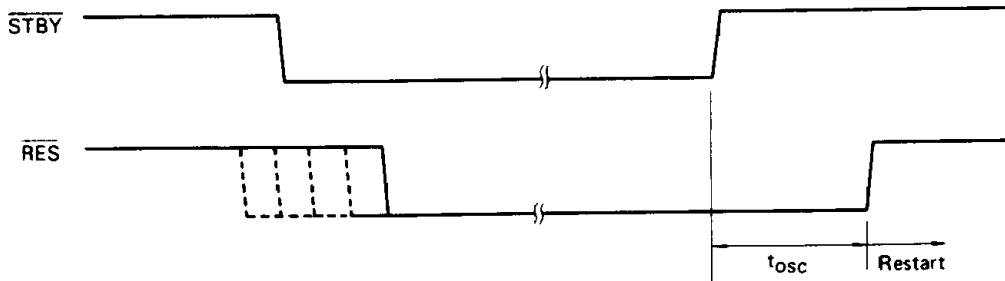


Figure 21 Timing Chart of Releasing from Standby Mode

Table 4 Status of Each Part of MCU in Low Power Dissipation Modes

| Mode     | Start    |                  | Condition  |      |               |           |      |                | Escape   |
|----------|----------|------------------|------------|------|---------------|-----------|------|----------------|--|
|          |          |                  | Oscillator | CPU  | Timer, Serial | Register* | RAM  | I/O terminal   |  |
| WAIT     | Software | WAIT instruction | Active     | Stop | Active        | Keep      | Keep | Keep           | STBY, RES, INT, INT <sub>2</sub> , each interrupt request of TIMER, TIMER <sub>2</sub> , SCI |
| STOP     |          | STOP instruction | Stop       | Stop | Stop          | Keep      | Keep | Keep           | STBY, RES, INT, INT <sub>2</sub>   |
| Stand-by | Hardware | STBY="Low"       | Stop       | Stop | Stop          | Reset     | Keep | High impedance | STBY="High"  |

\* Register in the CPU (except 1 bit in the CCR)

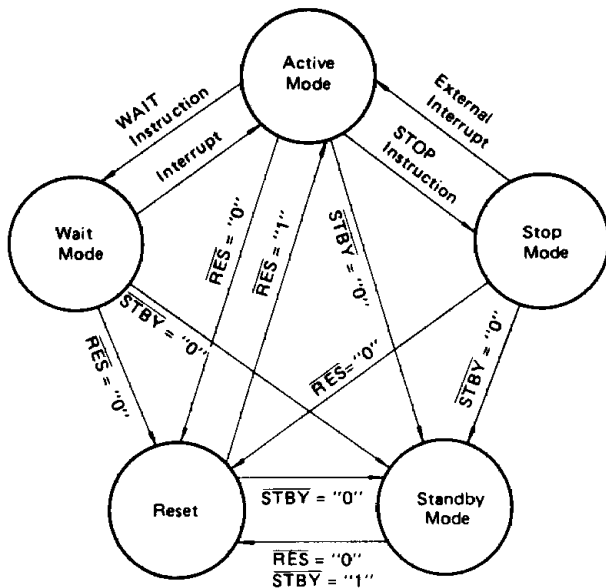


Figure 22 Transitions among Active Mode, Wait Mode, Stop Mode, Standby Mode and Reset

## ■ BIT MANIPULATION

The HD6305U0 MCU can use a single instruction (BSET or BCLR) to set or clear one bit of the RAM or an I/O port. Every bit of memory or I/O within page 0 (\$00 ~ \$FF) can be tested by the BRSET or BRCLR instruction; depending on the result of the test, the program can branch to required destinations. Since bits in the RAM, or I/O can be manipulated, the user may use a bit within the RAM as a flag or handle a single I/O bit as an independent I/O terminal. Fig. 23 shows an example of bit manipulation and the validity of test instructions. In the example, the program is configured assuming that bit 0 of port A is connected to a zero cross detector circuit and bit 1 of the same port to the trigger of a triac.

The program shown can activate the triac within a time of 10 $\mu$ s from zero-crossing through the use of only 7 bytes of the ROM. The on-chip timer provides a required time of delay and pulse width modulation of power is also possible.

```

SELF 1.  BRCLR 0, PORT A, SELF 1
          BSET 1, PORT A
          BCLR 1, PORT A
    
```

Figure 23 Example of Bit Manipulation

## ■ ADDRESSING MODES

Ten different addressing modes are available to the HD6305U0 MCU.

### ● Immediate

See Fig. 24. The immediate addressing mode provides access to a constant which does not vary during execution of the program.

This access requires an instruction length of 2 bytes. The effective address (EA) is PC and the operand is fetched from the byte that follows the operation code.

### ● Direct

See Fig. 25. In the direct addressing mode, the address of the operand is contained in the 2nd byte of the instruction. The user can gain direct access to memory up to the lower 255th address. All RAM and I/O registers are on page 0 of address space so that the direct addressing mode may be utilized.

### ● Extended

See Fig. 26. the extended addressing is used for referencing to all addresses of memory. The EA is the contents of the 2 bytes that follow the operation code. An extended addressing instruction requires a length of 3 bytes.

### ● Relative

See Fig. 27. The relative addressing mode is used with branch instructions only. When a branch occurs, the program counter is loaded with the contents of the byte following the operation code.  $EA = (PC) + 2 + Rel.$ , where Rel. indicates a signed 8-bit data following the operation code. If no branch occurs, Rel. = 0. When a branch occurs, the program jumps to any byte in the range +129 to -127. A branch instruction requires a length of 2 bytes.

### ● Indexed (No Offset)

See Fig. 28. The indexed addressing mode allows access up to the lower 255th address of memory. In this mode, an instruction requires a length of one byte. The EA is the contents of the index register.

### ● Indexed (8-bit Offset)

See Fig. 29. The EA is the contents of the byte following the operation code, plus the contents of the index register. This mode allows access up to the lower 511th address of memory. Each instruction when used in the indexed addressing mode (8-bit offset) requires a length of 2 bytes.

### ● Indexed (16-bit Offset)

See Fig. 30. The contents of the 2 bytes following the operation code are added to content of the index register to compute the value of EA. In this mode, the complete memory can be accessed. When used in the indexed addressing mode (16-bit offset), an instruction must be 3 bytes long.

### ● Bit Set/Clear

See Fig. 31. This addressing mode is applied to the BSET and BCLR instructions that can set or clear any bit on page 0. The lower 3 bits of the operation code specify the bit to be set or cleared. The byte that follows the operation code indicates an address within page 0.

### ● Bit Test and Branch

See Fig. 32. This addressing mode is applied to the BRSET and BRCLR instructions that can test any bit within page 0 and can be branched in the relative addressing mode. The byte to be tested is addressed depending on the contents of the byte following the operation code. Individual bits within the byte to be tested are specified by the lower 3 bits of the operation code. The 3rd byte represents a relative value which will be added to the program counter when a branch condition is established. Each of these instructions should be 3 bytes long. The result of the test is written in the carry bit of the condition code register. (Set if true, cleared otherwise.)

### ● Implied

See Fig. 33. This mode involves no EA. All information needed for execution of an instruction is contained in the operation code. Direct manipulation on the accumulator and index register is included in the implied addressing mode. Other instructions such as SWI and RTI are also used in this mode. All instructions used in the implied addressing mode should have a length of one byte.

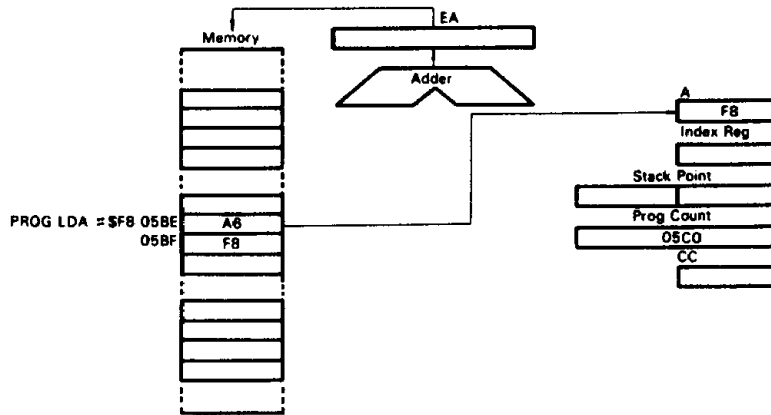


Figure 24 Example of Immediate Addressing

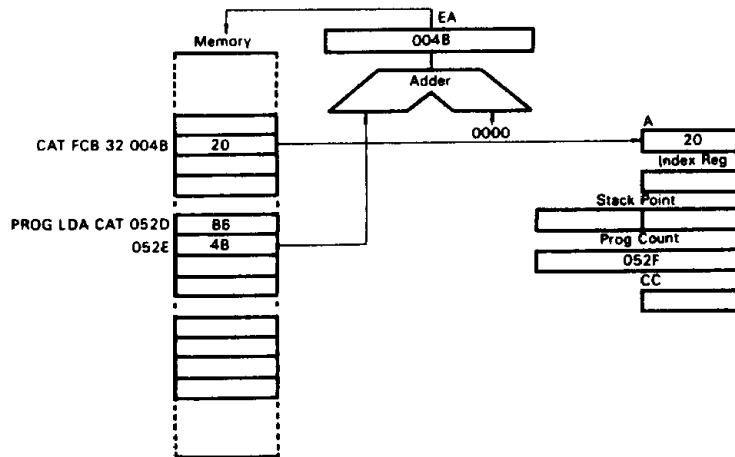


Figure 25 Example of Direct Addressing

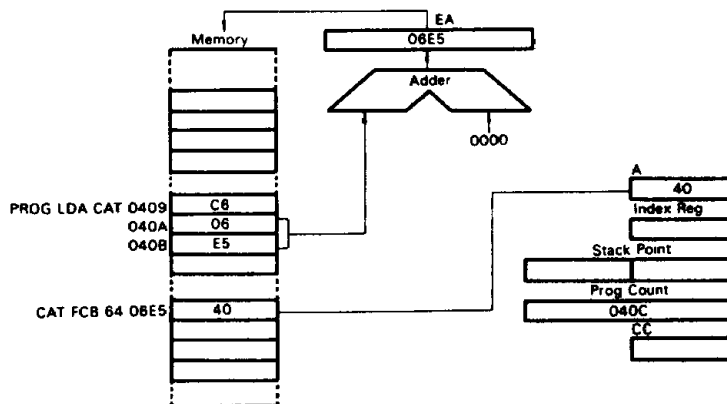


Figure 26 Example of Extended Addressing

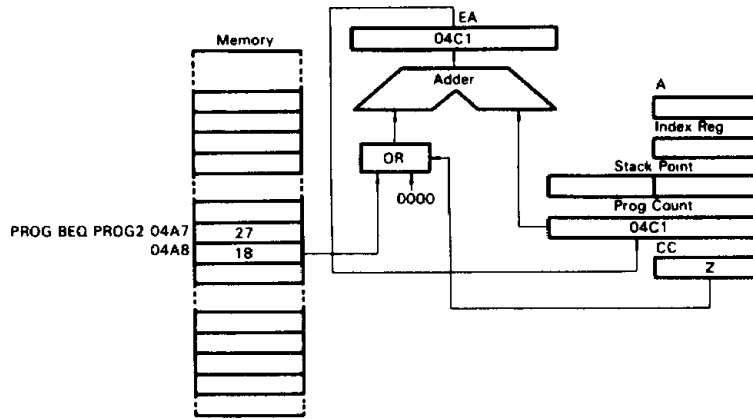


Figure 27 Example of Relative Addressing

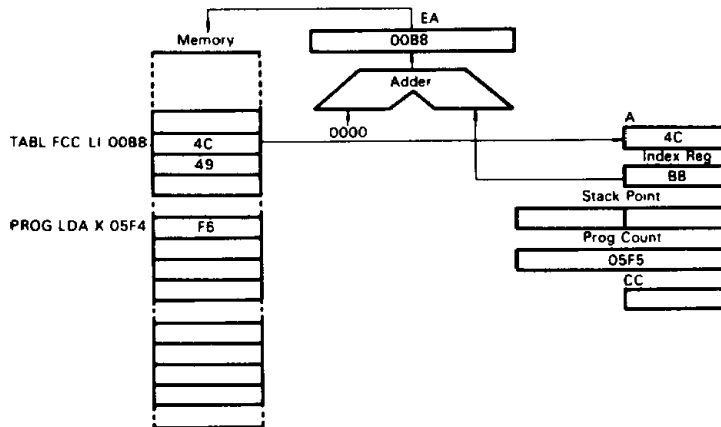


Figure 28 Example of Indexed (No Offset) Addressing

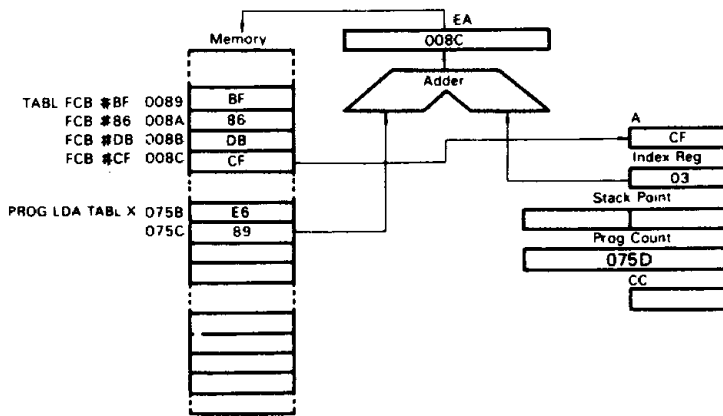


Figure 29 Example of Indexed (8-bit Offset) Addressing

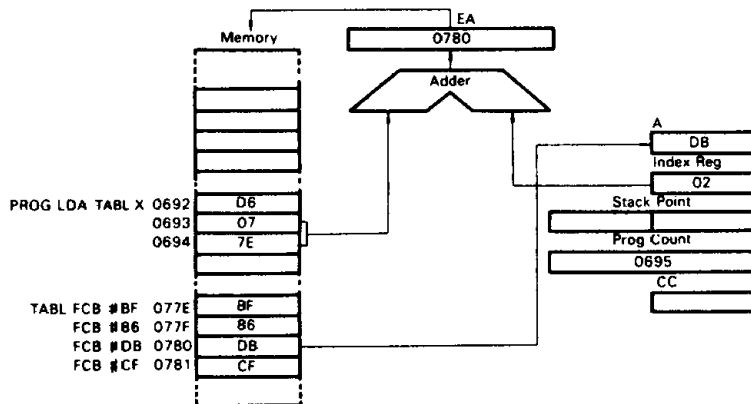


Figure 30 Example of Indexed (16-bit Offset) Addressing

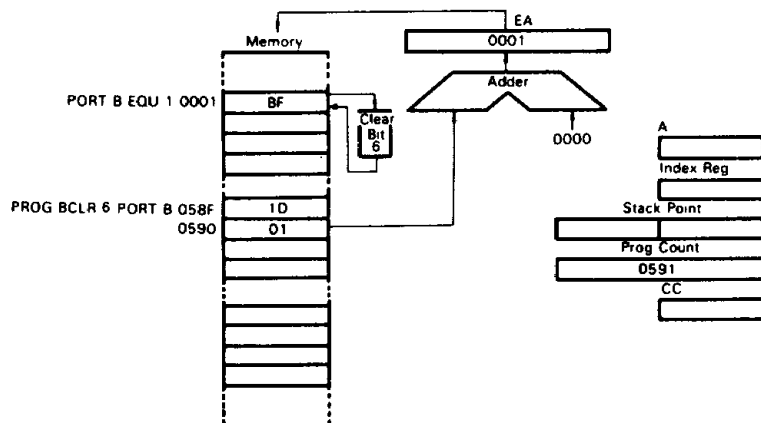


Figure 31 Example of Bit Set/Clear Addressing

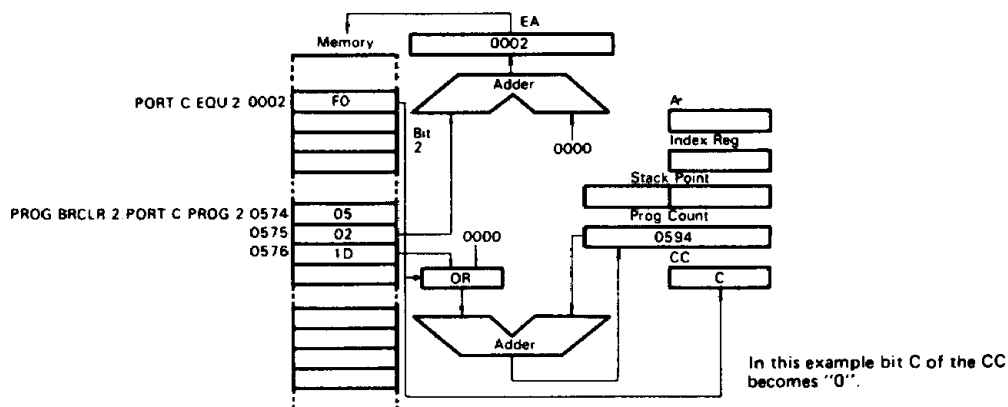


Figure 32 Example of Bit Test and Branch Addressing

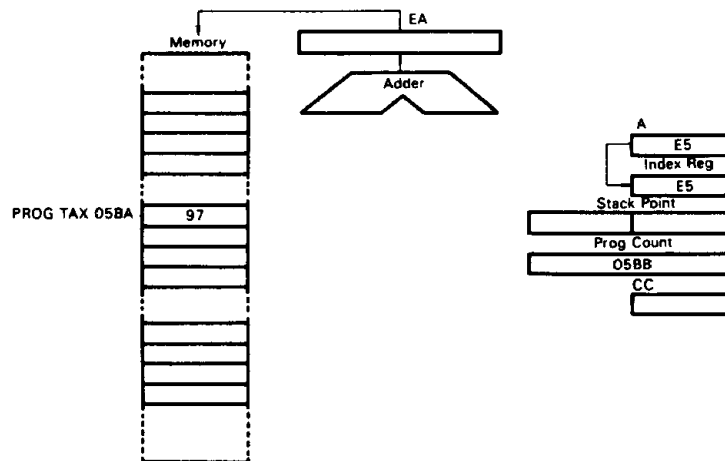


Figure 33 Example of Implied Addressing

■ **INSTRUCTION SET**

There are 62 basic instructions available to the HD6305U0 MCU. They can be classified into five categories: register/memory, read/modify/write, branch, bit manipulation, and control. The details of each instruction are described in Tables 5 through 11.

● **Register/Memory Instructions**

Most of these instructions use two operands. One operand is either an accumulator or index register. The other is derived from memory using one of the addressing modes used on the HD6305U0 MCU. There is no register operand in the unconditional jump instruction (JMP) and the subroutine jump instruction (JSR). See Table 5.

● **Read/Modify/Write Instructions**

These instructions read a memory or register, then modify or test its contents, and write the modified value into the memory or register. Zero test instruction (TST) does not write data, and is handled as an exception in the read/modify/write group. See Table 6.

● **Branch Instructions**

A branch instruction branches from the program sequence in progress if a particular condition is established. See Table 7.

● **Bit Manipulation Instructions**

These instructions can be used with any bit located up to the lower 255th address of memory. Two groups are available; one for setting or clearing and the other for bit testing and branching. See Table 8.

● **Control Instructions**

The control instructions control the operation of the MCU which is executing a program. See Table 9.

● **List of Instructions in Alphabetical Order**

Table 10 lists all the instructions used on the HD6305U0 MCU in the alphabetical order.

● **Operation Code Map**

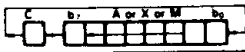
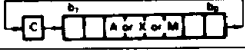

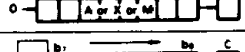
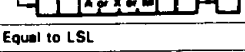
Table 11 shows the operation code map for the instructions used on the MCU.

Table 5 Register/Memory Instructions

| Operations                                  | Mnemonic | Addressing Modes |   |   |        |   |   |          |   |   |                        |   |   | Boolean/<br>Arithmetic<br>Operation | Condition<br>Code         |   |    |                            |   |         |   |   |   |   |   |
|---|----------|------------------|---|---|--------|---|---|----------|---|---|------------------------|---|---|-------------------------------------|---------------------------|---|----|----------------------------|---|---------|---|---|---|---|---|
|   |          | Immediate        |   |   | Direct |   |   | Extended |   |   | Indexed<br>(No Offset) |   |   |                                     | Indexed<br>(8-Bit Offset) |   |    | Indexed<br>(16-Bit Offset) |   |         | H | I | N | Z | C |
|   |          | OP               | # | ~ | OP     | # | ~ | OP       | # | ~ | OP                     | # | ~ |                                     | OP                        | # | ~  | OP                         | # | ~       |   |   |   |   |   |
| Load A from Memory                          | LDA      | A6               | 2 | 2 | B6     | 2 | 3 | C6       | 3 | 4 | F6                     | 1 | 3 | E6                                  | 2                         | 4 | D6 | 3                          | 5 | M→A     | • | • | ∧ | ∧ | • |
| Load X from Memory                          | LDX      | AE               | 2 | 2 | BE     | 2 | 3 | CE       | 3 | 4 | FE                     | 1 | 3 | EE                                  | 2                         | 4 | DE | 3                          | 5 | M→X     | • | • | ∧ | ∧ | • |
| Store A in Memory                           | STA      | —                | — | — | B7     | 2 | 3 | C7       | 3 | 4 | F7                     | 1 | 4 | E7                                  | 2                         | 4 | D7 | 3                          | 5 | A→M     | • | • | ∧ | ∧ | • |
| Store X in Memory                           | STX      | —                | — | — | BF     | 2 | 3 | CF       | 3 | 4 | FF                     | 1 | 4 | EF                                  | 2                         | 4 | DF | 3                          | 5 | X→M     | • | • | ∧ | ∧ | • |
| Add Memory to A                             | ADD      | AB               | 2 | 2 | BB     | 2 | 3 | CB       | 3 | 4 | FB                     | 1 | 3 | EB                                  | 2                         | 4 | DB | 3                          | 5 | A+M→A   | ∧ | • | ∧ | ∧ | ∧ |
| Add Memory and Carry<br>to A                | ADC      | A9               | 2 | 2 | B9     | 2 | 3 | C9       | 3 | 4 | F9                     | 1 | 3 | E9                                  | 2                         | 4 | D9 | 3                          | 5 | A+M+C→A | ∧ | • | ∧ | ∧ | ∧ |
| Subtract Memory                             | SUB      | A0               | 2 | 2 | B0     | 2 | 3 | C0       | 3 | 4 | F0                     | 1 | 3 | E0                                  | 2                         | 4 | D0 | 3                          | 5 | A-M→A   | • | • | ∧ | ∧ | ∧ |
| Subtract Memory from<br>A with Borrow       | SBC      | A2               | 2 | 2 | B2     | 2 | 3 | C2       | 3 | 4 | F2                     | 1 | 3 | E2                                  | 2                         | 4 | D2 | 3                          | 5 | A-M-C→A | • | • | ∧ | ∧ | ∧ |
| AND Memory to A                             | AND      | A4               | 2 | 2 | B4     | 2 | 3 | C4       | 3 | 4 | F4                     | 1 | 3 | E4                                  | 2                         | 4 | D4 | 3                          | 5 | A·M→A   | • | • | ∧ | ∧ | • |
| OR Memory with A                            | ORA      | AA               | 2 | 2 | BA     | 2 | 3 | CA       | 3 | 4 | FA                     | 1 | 3 | EA                                  | 2                         | 4 | DA | 3                          | 5 | A+M→A   | • | • | ∧ | ∧ | • |
| Exclusive OR Memory<br>with A               | EOR      | A8               | 2 | 2 | B8     | 2 | 3 | CB       | 3 | 4 | FB                     | 1 | 3 | EB                                  | 2                         | 4 | DB | 3                          | 5 | A+M→A   | • | • | ∧ | ∧ | • |
| Arithmetic Compare A<br>with Memory         | CMP      | A1               | 2 | 2 | B1     | 2 | 3 | C1       | 3 | 4 | F1                     | 1 | 3 | E1                                  | 2                         | 4 | D1 | 3                          | 5 | A-M     | • | • | ∧ | ∧ | ∧ |
| Arithmetic Compare X<br>with Memory         | CPX      | A3               | 2 | 2 | B3     | 2 | 3 | C3       | 3 | 4 | F3                     | 1 | 3 | E3                                  | 2                         | 4 | D3 | 3                          | 5 | X-M     | • | • | ∧ | ∧ | ∧ |
| Bit Test Memory with<br>A (Logical Compare) | BIT      | A5               | 2 | 2 | B5     | 2 | 3 | C5       | 3 | 4 | F5                     | 1 | 3 | E5                                  | 2                         | 4 | D5 | 3                          | 5 | A·M     | • | • | ∧ | ∧ | • |
| Jump Unconditional                          | JMP      | —                | — | — | BC     | 2 | 2 | CC       | 3 | 3 | FC                     | 1 | 2 | EC                                  | 2                         | 3 | DC | 3                          | 4 |         | • | • | • | • | • |
| Jump to Subroutine                          | JSR      | —                | — | — | BD     | 2 | 5 | CD       | 3 | 6 | FD                     | 1 | 5 | ED                                  | 2                         | 5 | DD | 3                          | 6 |         | • | • | • | • | • |

Symbols: Op = Operation  
# = Number of bytes  
~ = Number of cycles

Table 6 Read/Modify/Write Instructions

| Operations                   | Mnemonic | Addressing Modes |   |   |            |   |   |        |   |   |                        |   |   | Boolean/Arithmetic Operation | Condition<br>Code         |   |   |   |   |  |   |   |   |   |   |
|------------------------------|----------|------------------|---|---|------------|---|---|--------|---|---|------------------------|---|---|------------------------------|---------------------------|---|---|---|---|--|---|---|---|---|---|
|                              |          | Implied(A)       |   |   | Implied(X) |   |   | Direct |   |   | Indexed<br>(No Offset) |   |   |                              | Indexed<br>(8-Bit Offset) |   |   | H | I | N  | Z | C |   |   |   |
|                              |          | OP               | # | ~ | OP         | # | ~ | OP     | # | ~ | OP                     | # | ~ |                              | OP                        | # | ~ |   |   |  |   |   |   |   |   |
| Increment                    | INC      | 4C               | 1 | 2 | 5C         | 1 | 2 | 3C     | 2 | 5 | 7C                     | 1 | 5 | 6C                           | 2                         | 6 |   |   |   | A+1→A or X+1→X or M+1→M  | • | • | ∧ | ∧ | • |
| Decrement                    | DEC      | 4A               | 1 | 2 | 5A         | 1 | 2 | 3A     | 2 | 5 | 7A                     | 1 | 5 | 6A                           | 2                         | 6 |   |   |   | A-1→A or X-1→X or M-1→M  | • | • | ∧ | ∧ | • |
| Clear                        | CLR      | 4F               | 1 | 2 | 5F         | 1 | 2 | 3F     | 2 | 5 | 7F                     | 1 | 5 | 6F                           | 2                         | 6 |   |   |   | 00→A or 00→X or 00→M   | • | • | D | 1 | • |
| Complement                   | COM      | 43               | 1 | 2 | 53         | 1 | 2 | 33     | 2 | 5 | 73                     | 1 | 5 | 63                           | 2                         | 6 |   |   |   | $\bar{A}$ →A or $\bar{X}$ →X or $\bar{M}$ →M   | • | • | ∧ | ∧ | 1 |
| Negate<br>(2's Complement)   | NEG      | 40               | 1 | 2 | 50         | 1 | 2 | 30     | 2 | 5 | 70                     | 1 | 5 | 60                           | 2                         | 6 |   |   |   | 00→A or 00→X or 00→M<br>or 00→M→M  | • | • | ∧ | ∧ | ∧ |
| Rotate Left Thru Carry       | ROL      | 49               | 1 | 2 | 59         | 1 | 2 | 39     | 2 | 5 | 79                     | 1 | 5 | 69                           | 2                         | 6 |   |   |   |  | • | • | ∧ | ∧ | ∧ |
| Rotate Right Thru Carry      | ROR      | 46               | 1 | 2 | 56         | 1 | 2 | 36     | 2 | 5 | 76                     | 1 | 5 | 66                           | 2                         | 6 |   |   |   |  | • | • | ∧ | ∧ | ∧ |
| Logical Shift Left           | LSL      | 48               | 1 | 2 | 58         | 1 | 2 | 38     | 2 | 5 | 78                     | 1 | 5 | 68                           | 2                         | 6 |   |   |   |  | • | • | ∧ | ∧ | ∧ |
| Logical Shift Right          | LSR      | 44               | 1 | 2 | 54         | 1 | 2 | 34     | 2 | 5 | 74                     | 1 | 5 | 64                           | 2                         | 6 |   |   |   |  | • | • | 0 | ∧ | ∧ |
| Arithmetic Shift Right       | ASR      | 47               | 1 | 2 | 57         | 1 | 2 | 37     | 2 | 5 | 77                     | 1 | 5 | 67                           | 2                         | 6 |   |   |   |  | • | • | ∧ | ∧ | ∧ |
| Arithmetic Shift Left        | ASL      | 48               | 1 | 2 | 58         | 1 | 2 | 38     | 2 | 5 | 78                     | 1 | 5 | 68                           | 2                         | 6 |   |   |   | Equal to LSL   | • | • | ∧ | ∧ | ∧ |
| Test for Negative<br>or Zero | TST      | 4D               | 1 | 2 | 5D         | 1 | 2 | 3D     | 2 | 4 | 7D                     | 1 | 4 | 6D                           | 2                         | 5 |   |   |   | A-00 or X-00 or M-00   | • | • | ∧ | ∧ | • |

Symbols: Op = Operation  
# = Number of bytes  
~ = Number of cycles

# HD6305U0, HD63A05U0, HD63B05U0

Table 7 Branch Instructions

| Operations                            | Mnemonic | Addressing Modes |   |   | Branch Test | Condition Code |   |   |   |   |
|---------------------------------------|----------|------------------|---|---|-------------|----------------|---|---|---|---|
|                                       |          | Relative         |   |   |             | H              | I | N | Z | C |
|                                       |          | OP               | # | ~ |             |                |   |   |   |   |
| Branch Always                         | BRA      | 20               | 2 | 3 | None        | •              | • | • | • | • |
| Branch Never                          | BRN      | 21               | 2 | 3 | None        | •              | • | • | • | • |
| Branch IF Higher                      | BHI      | 22               | 2 | 3 | C+Z=0       | •              | • | • | • | • |
| Branch IF Lower or Same               | BLS      | 23               | 2 | 3 | C+Z=1       | •              | • | • | • | • |
| Branch IF Carry Clear                 | BCC      | 24               | 2 | 3 | C=0         | •              | • | • | • | • |
| (Branch IF Higher or Same)            | (BHS)    | 24               | 2 | 3 | C=0         | •              | • | • | • | • |
| Branch IF Carry Set                   | BCS      | 25               | 2 | 3 | C=1         | •              | • | • | • | • |
| (Branch IF Lower)                     | (BLO)    | 25               | 2 | 3 | C=1         | •              | • | • | • | • |
| Branch IF Not Equal                   | BNE      | 26               | 2 | 3 | Z=0         | •              | • | • | • | • |
| Branch IF Equal                       | BEQ      | 27               | 2 | 3 | Z=1         | •              | • | • | • | • |
| Branch IF Half Carry Clear            | BHCC     | 28               | 2 | 3 | H=0         | •              | • | • | • | • |
| Branch IF Half Carry Set              | BHCS     | 29               | 2 | 3 | H=1         | •              | • | • | • | • |
| Branch IF Plus                        | BPL      | 2A               | 2 | 3 | N=0         | •              | • | • | • | • |
| Branch IF Minus                       | BMI      | 2B               | 2 | 3 | N=1         | •              | • | • | • | • |
| Branch IF Interrupt Mask Bit is Clear | BMC      | 2C               | 2 | 3 | I=0         | •              | • | • | • | • |
| Branch IF Interrupt Mask Bit is Set   | BMS      | 2D               | 2 | 3 | I=1         | •              | • | • | • | • |
| Branch IF Interrupt Line is Low       | BIL      | 2E               | 2 | 3 | INT=0       | •              | • | • | • | • |
| Branch IF Interrupt Line is High      | BIH      | 2F               | 2 | 3 | INT=1       | •              | • | • | • | • |
| Branch to Subroutine                  | BSR      | AD               | 2 | 5 | —           | •              | • | • | • | • |

Symbols: Op = Operation  
 # = Number of bytes  
 ~ = Number of cycles

Table 8 Bit Manipulation Instructions

| Operations               | Mnemonic         | Addressing Modes |   |   |                     |   |   | Boolean/<br>Arithmetic<br>Operation | Branch<br>Test | Condition Code |   |   |   |   |
|--------------------------|------------------|------------------|---|---|---------------------|---|---|-------------------------------------|----------------|----------------|---|---|---|---|
|                          |                  | Bit Set/Clear    |   |   | Bit Test and Branch |   |   |                                     |                | H              | I | N | Z | C |
|                          |                  | OP               | # | ~ | OP                  | # | ~ |                                     |                |                |   |   |   |   |
| Branch IF Bit n is set   | BRSET n(n=0...7) | —                | — | — | 2·n                 | 3 | 5 | —                                   | Mn=1           | •              | • | • | • | ^ |
| Branch IF Bit n is clear | BRCLR n(n=0...7) | —                | — | — | 01+2·n              | 3 | 5 | —                                   | Mn=0           | •              | • | • | • | ^ |
| Set Bit n                | BSET n(n=0...7)  | 10+2·n           | 2 | 5 | —                   | — | — | 1→Mn                                | —              | •              | • | • | • | • |
| Clear Bit n              | BCLR n(n=0...7)  | 11+2·n           | 2 | 5 | —                   | — | — | 0→Mn                                | —              | •              | • | • | • | • |

Symbols: Op = Operation  
 # = Number of bytes  
 ~ = Number of cycles





Table 9 Control Instructions

| Operations               | Mnemonic | Addressing Modes |   |    | Boolean Operation                                    | Condition Code |   |   |   |    |
|--------------------------|----------|------------------|---|----|--|----------------|---|---|---|----|
|                          |          | Implied          |   |    |  | H              | I | N | Z | C  |
|                          |          | OP               | # | ~  |  |                |   |   |   |    |
| Transfer A to X          | TAX      | 97               | 1 | 2  | A→X  | ●              | ● | ● | ● | ●  |
| Transfer X to A          | TXA      | 9F               | 1 | 2  | X→A  | ●              | ● | ● | ● | ●  |
| Set Carry Bit            | SEC      | 99               | 1 | 1  | 1→C  | ●              | ● | ● | ● | 1  |
| Clear Carry Bit          | CLC      | 98               | 1 | 1  | 0→C  | ●              | ● | ● | ● | 0  |
| Set Interrupt Mask Bit   | SEI      | 9B               | 1 | 2  | 1→I  | ●              | 1 | ● | ● | ●  |
| Clear Interrupt Mask Bit | CLI      | 9A               | 1 | 2  | 0→I  | ●              | 0 | ● | ● | ●  |
| Software Interrupt       | SWI      | 83               | 1 | 10 |  | ●              | 1 | ● | ● | ●  |
| Return from Subroutine   | RTS      | 81               | 1 | 5  |  | ●              | ● | ● | ● | ●  |
| Return from Interrupt    | RTI      | 80               | 1 | 8  |  | ?              | ? | ? | ? | ?  |
| Reset Stack Pointer      | RSP      | 9C               | 1 | 2  | \$FF→SP  | ●              | ● | ● | ● | ●  |
| No-Operation             | NOP      | 9D               | 1 | 1  | Advance Prog. Cntr. Only                             | ●              | ● | ● | ● | ●  |
| Decimal Adjust A         | DAA      | 8D               | 1 | 2  | Converts binary add of BCD charcters into BCD format | ●              | ● | ∧ | ∧ | ∧* |
| Stop                     | STOP     | 8E               | 1 | 4  |  | ●              | 0 | ● | ● | ●  |
| Wait                     | WAIT     | 8F               | 1 | 4  |  | ●              | 0 | ● | ● | ●  |

Symbols: Op = Operation  
 # = Number of bytes  
 ~ = Number of cycles  
 \* Are BCD characters of upper byte 10 or more? (They are not cleared if set in advance.)

Table 10 Instruction Set (in Alphabetical Order)

| Mnemonic | Addressing Modes |           |        |          |          |                     |                 |                  |               | Condition Code    |   |   |   |   |   |
|----------|------------------|-----------|--------|----------|----------|---------------------|-----------------|------------------|---------------|-------------------|---|---|---|---|---|
|          | Implied          | Immediate | Direct | Extended | Relative | Indexed (No Offset) | Indexed (8-Bit) | Indexed (16-Bit) | Bit Set/Clear | Bit Test & Branch | H | I | N | Z | C |
| ADC      |                  | x         | x      | x        |          | x                   | x               | x                |               |                   | ∧ | ● | ∧ | ∧ | ∧ |
| ADD      |                  | x         | x      | x        |          | x                   | x               | x                |               |                   | ∧ | ● | ∧ | ∧ | ∧ |
| AND      |                  | x         | x      | x        |          | x                   | x               | x                |               |                   | ● | ● | ∧ | ∧ | ● |
| ASL      | x                |           | x      |          |          | x                   | x               |                  |               |                   | ● | ● | ∧ | ∧ | ∧ |
| ASR      | x                |           | x      |          |          | x                   | x               |                  |               |                   | ● | ● | ∧ | ∧ | ∧ |
| BCC      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BCLR     |                  |           |        |          |          |                     |                 |                  | x             |                   | ● | ● | ● | ● | ● |
| BCS      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BEQ      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BHCC     |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BHCS     |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BHI      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| (BHS)    |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BIH      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BIL      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BIT      |                  | x         | x      | x        |          | x                   | x               | x                |               |                   | ● | ● | ∧ | ∧ | ● |
| (BLO)    |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BLS      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BMC      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BMI      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BMS      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BNE      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BPL      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BRA      |                  |           |        |          | x        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |

Condition Code Symbols:  
 H Half Carry (From Bit 3)    C Carry Borrow  
 I Interrupt Mask            ∧ Test and Set if True, Cleared Otherwise  
 N Negative (Sign Bit)       ● Not Affected  
 Z Zero                        ? Load CC Register From Stack

(to be continued)



# HD6305U0, HD63A05U0, HD63B05U0

Table 10 Instruction Set (in Alphabetical Order)

| Mnemonic | Addressing Modes |           |        |          |          |                     |                 |                  |               | Condition Code    |   |   |   |   |   |
|----------|------------------|-----------|--------|----------|----------|---------------------|-----------------|------------------|---------------|-------------------|---|---|---|---|---|
|          | Implied          | Immediate | Direct | Extended | Relative | Indexed (No Offset) | Indexed (8-Bit) | Indexed (16-Bit) | Bit Set/Clear | Bit Test & Branch | H | I | N | Z | C |
| BRN      |                  |           |        |          | X        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| BRCLR    |                  |           |        |          |          |                     |                 |                  |               | X                 | ● | ● | ● | ● | ^ |
| BRSET    |                  |           |        |          |          |                     |                 |                  |               | X                 | ● | ● | ● | ● | ^ |
| BSET     |                  |           |        |          |          |                     |                 |                  | X             |                   | ● | ● | ● | ● | ● |
| BSR      |                  |           |        |          | X        |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| CLC      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | ● | ● | ● | 0 |
| CLI      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | 0 | ● | ● | ● |
| CLR      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | 0 | 1 | ● |
| CMP      |                  | X         | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ^ |
| COM      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | ^ | ^ | 1 |
| CPX      |                  | X         | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ^ |
| DAA      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | ● | ^ | ^ | ^ |
| DEC      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | ^ | ^ | ● |
| EOR      |                  | X         | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ● |
| INC      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | ^ | ^ | ● |
| JMP      |                  |           | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ● | ● | ● |
| JSR      |                  |           | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ● | ● | ● |
| LDA      |                  | X         | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ● |
| LDX      |                  | X         | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ● |
| LSL      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | ^ | ^ | ^ |
| LSR      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | 0 | ^ | ^ |
| NEG      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | ^ | ^ | ^ |
| NOP      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| ORA      |                  | X         | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ● |
| ROL      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | ^ | ^ | ^ |
| ROR      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | ^ | ^ | ^ |
| RSP      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| RTI      | X                |           |        |          |          |                     |                 |                  |               |                   | ? | ? | ? | ? | ? |
| RTS      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| SBC      |                  | X         | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ^ |
| SEC      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | ● | ● | ● | 1 |
| SEI      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | 1 | ● | ● | ● |
| STA      |                  |           | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ● |
| STOP     | X                |           |        |          |          |                     |                 |                  |               |                   | ● | 0 | ● | ● | ● |
| STX      |                  |           | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ● |
| SUB      |                  | X         | X      | X        |          | X                   | X               | X                |               |                   | ● | ● | ^ | ^ | ^ |
| SWI      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | 1 | ● | ● | ● |
| TAX      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| TST      | X                |           | X      |          |          | X                   | X               |                  |               |                   | ● | ● | ^ | ^ | ● |
| TXA      | X                |           |        |          |          |                     |                 |                  |               |                   | ● | ● | ● | ● | ● |
| WAIT     | X                |           |        |          |          |                     |                 |                  |               |                   | ● | 0 | ● | ● | ● |

Condition Code Symbols:

- |   |                         |   |   |
|---|-------------------------|---|---|
| H | Half Carry (From Bit 3) | C | Carry Borrow                            |
| I | Interrupt Mask          | ^ | Test and Set if True, Cleared Otherwise |
| N | Negative (Sign Bit)     | ● | Not Affected                            |
| Z | Zero                    | ? | Load CC Register From Stack             |



Table 11 Operation Code Map

|   | Bit Manipulation |           | Branch | Read/Modify/Write |     |         |      |     | Control |         | Register/Memory |         |         |         |         |         |   |   |
|---|------------------|-----------|--------|-------------------|-----|---------|------|-----|---------|---------|-----------------|---------|---------|---------|---------|---------|---|---|
|   | Test & Branch    | Set/Clear | Rel    | DIR               | A   | X       | .X1  | .X0 | IMP     | IMP     | IMM             | DIR     | EXT     | .X2     | .X1     | .X0     |   |   |
|   | 0                | 1         | 2      | 3                 | 4   | 5       | 6    | 7   | 8       | 9       | A               | B       | C       | D       | E       | F       |   |   |
| 0 | BRSET0           | BSET0     | BRA    | NEG               |     |         |      |     | RTI*    | —       | SUB             |         |         |         |         |         | 0 |   |
| 1 | BRCLR0           | BCLR0     | BRN    | —                 |     |         |      |     | RTS*    | —       | CMP             |         |         |         |         |         | 1 |   |
| 2 | BRSET1           | BSET1     | BHI    | —                 |     |         |      |     | —       | —       | SBC             |         |         |         |         |         | 2 |   |
| 3 | BRCLR1           | BCLR1     | BLS    | COM               |     |         |      |     | SWI*    | —       | CPX             |         |         |         |         |         | 3 |   |
| 4 | BRSET2           | BSET2     | BCC    | LSR               |     |         |      |     | —       | —       | AND             |         |         |         |         |         | 4 |   |
| 5 | BRCLR2           | BCLR2     | BCS    | —                 |     |         |      |     | —       | —       | BIT             |         |         |         |         |         | 5 |   |
| 6 | BRSET3           | BSET3     | BNE    | ROR               |     |         |      |     | —       | —       | LDA             |         |         |         |         |         | 6 |   |
| 7 | BRCLR3           | BCLR3     | BEQ    | ASR               |     |         |      |     | —       | TAX*    | —               | STA     |         |         |         | STA(+1) | 7 |   |
| 8 | BRSET4           | BSET4     | BHCC   | LSL ASL           |     |         |      |     | —       | CLC     | EOR             |         |         |         |         |         | 8 |   |
| 9 | BRCLR4           | BCLR4     | BHCS   | ROL               |     |         |      |     | —       | SEC     | ADC             |         |         |         |         |         | 9 |   |
| A | BRSET5           | BSET5     | BPL    | DEC               |     |         |      |     | —       | CLI*    | ORA             |         |         |         |         |         | A |   |
| B | BRCLR5           | BCLR5     | BMI    | —                 |     |         |      |     | —       | —       | ADD             |         |         |         |         |         | B |   |
| C | BRSET6           | BSET6     | BMC    | INC               |     |         |      |     | —       | RSP*    | —               | JMP(-1) |         |         |         |         |   | C |
| D | BRCLR6           | BCLR6     | BMS    | TST(-1)           | TST | TST(-1) | DAA* | NOP | BSR*    | JSR(+2) | JSR(+1)         | JSR(+2) | JSR(+1) | JSR(+2) | JSR(+1) | D       |   |   |
| E | BRSET7           | BSET7     | BIL    | —                 |     |         |      |     | STOP*   | —       | LDX             |         |         |         |         |         | E |   |
| F | BRCLR7           | BCLR7     | BIH    | CLR               |     |         |      |     | WAIT*   | TXA*    | —               | STX     |         |         |         | STX(+1) | F |   |
|   | 3/5              | 2/5       | 2/3    | 2/5               | 1/2 | 1/2     | 2/6  | 1/5 | 1/*     | 1/1     | 2/2             | 2/3     | 3/4     | 3/5     | 2/4     | 1/3     |   |   |

- (NOTES) 1. "—" is an undefined operation code.  
 2. The lowermost numbers in each column represent a byte count and the number of cycles required (byte count/number of cycles).  
 The number of cycles for the mnemonics asterisked (\*) is as follows:  
 RTI = 8                      DAA = 2                      TAX = 2                      BSR = 5  
 RTS = 5                      STOP = 4                      RSP = 2                      CLI = 2  
 SWI = 10                      WAIT = 4                      TXA = 2                      SEI = 2  
 3. The parenthesized numbers must be added to the cycle count of the particular instruction.

● **Additional Instructions**

The following new instructions are used on the HD6305U0:

- DAA** Converts the contents of the accumulator into BCD code.
- WAIT** Causes the MCU to enter the wait mode. For this mode, see the topic, Wait Mode.
- STOP** Causes the MCU to enter the stop mode. For this mode, see the topic, Stop Mode.

■ **PRECAUTION 1—BOARD DESIGN OF OSCILLATION CIRCUIT**

When connecting crystal and ceramic resonator with the XTAL and EXTAL pins to oscillate, observe the followings in designing the board.

- (1) Locate crystal, ceramic resonator, and load capacity C<sub>1</sub> and C<sub>2</sub> as near the LSI as possible. (Induction of noise from outside to the XTAL and EXTAL pins may cause trouble in oscillation.)
- (2) Wire the signal lines to the neighboring XTAL and EXTAL pins as far apart as possible.
- (3) Board design of situating signal lines or power supply lines near the oscillator circuit as shown as Figure 35, should not be used because of trouble in oscillation by induction. The resistor between the XTAL and EXTAL, and pins close to them should be 10MΩ or more. The circuit in Fig. 34 is an example of good board design.

■ **PRECAUTION 2—SENDING/RECEIVING PROGRAM OF SERIAL DATA**

Reading from or Writing into the SCI data register (SDR: \$0012) during sending/receiving of serial data may make sending/receiving operation of SCI out of order.

■ **PRECAUTION 3—WAIT/STOP INSTRUCTIONS PROGRAM**

When I bit of condition code register is "1" and an interrupt (INT, TIMER/INT<sub>2</sub>, SCI/TIMER<sub>2</sub>) is held, the MCU does not enter into WAIT mode by executing the WAIT instruction.

In that case, the MCU executes the corresponding interrupt processing routine after the 4 dummy cycle.

When external interrupts (INT), INT<sub>20</sub> are held at the I bit mask, the MCU does not enter into the STOP mode by the STOP instruction execution. The MCU executes the corresponding interrupt processing routine after the 4 dummy cycles, in this case, either.

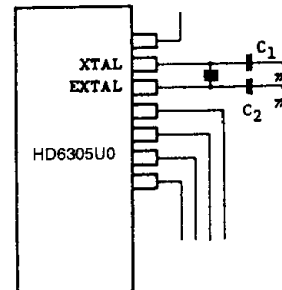


Figure 34 Design of Oscillation Circuit Board

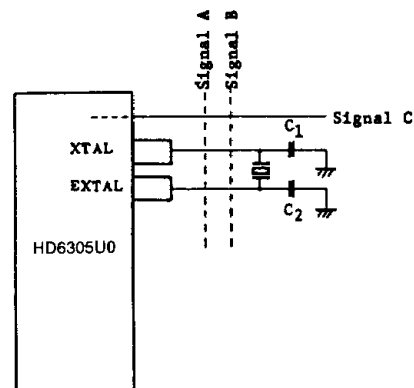
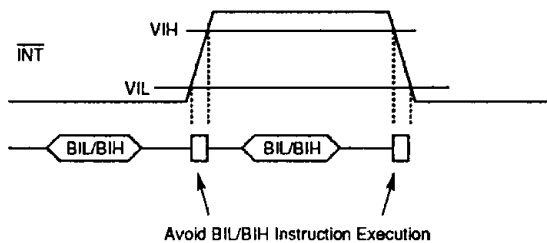


Figure 35 Example of Circuit Causing Trouble in Oscillation

**PRECAUTION WHEN USING BIL/BIH INSTRUCTION**

- (1) Execute instruction after the  $\overline{INT}$  voltage level has stabilized above  $V_{IH}$  or below  $V_{IL}$ .
- (2)  $\overline{INT}$  voltage level needs to be stabilized while BIL/BIH instruction execution.

There may be a malfunction by glitch on control signal is BIL/BIH instruction execution has exercised in unstabilized  $\overline{INT}$  signal level.

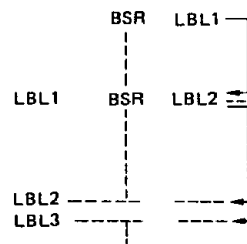


**PRECAUTION TO USE BSR**

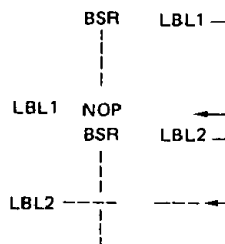
If there is 2nd BSR programmed on the address which is directed by first BSR, 2nd BSR may not be executed correctly. For this reason, BSR should not be programmed on the address which is directed by first BSR.

If necessary, please program as following

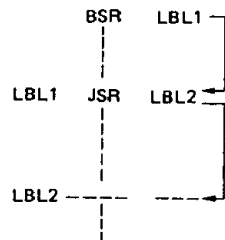
- (1) On the address which first BSR directed, NOP instruction should be inserted before second BSR.
- (2) On the address which first BSR direct, JSR instruction should be programmed instead of 2nd BSR.



example of malfunction of 2nd BSR execution



example of counter measure (NOP is inserted)



example of counter measure (JSR is used instead of BSR)