HD14522B, HD14526B

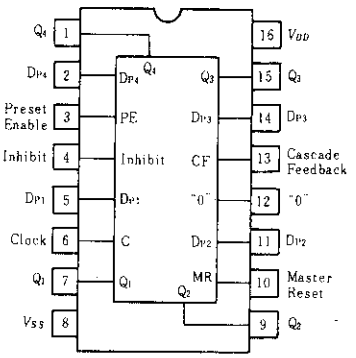
Programmable Divide-by-N 4-bit Counter

The HD14522B BCD counter and the HD14526B binary counter are programmable, cascadable down counters with a decoded " 0 " atate output for divide-by-N applications. In single stage applications the " 0 " output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Clock Inhibit input allows disabling low power dissipation and/or high noise immunity.

■ FEATURES

- Quiescent Current=5nA/pkg typ. @5V
- Supply Voltage Range=3 to 18V
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-clocked Design . . . Incremented on Positive transition of Clock or Negative Transition of Clock Inhibit
- 5MHz Counting Rate
- Asynchronous Preset Enable
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperture Range

■ PIN ARRANGEMENT



(Top View)

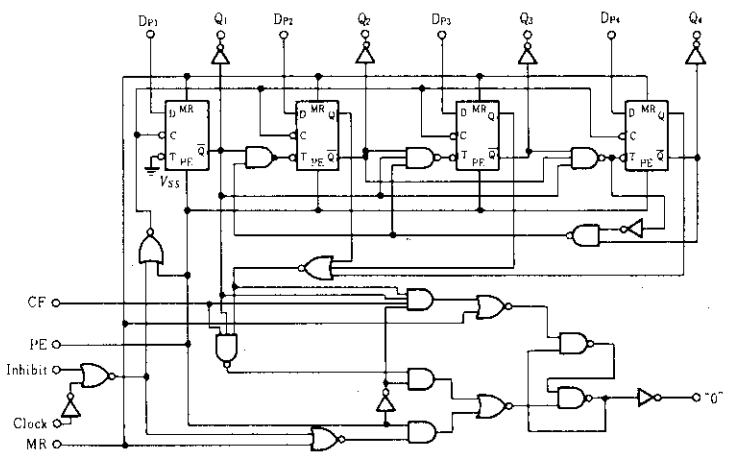
■ TRUTH TABLE

● Both Types

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
⌐	0	0	0	Count 1
×	1	0	0	No Count
1	⌙	0	0	Count 1
×	×	1	0	Preset
×	×	×	1	Reset

■ LOGIC DIAGRAM

● HD14522B



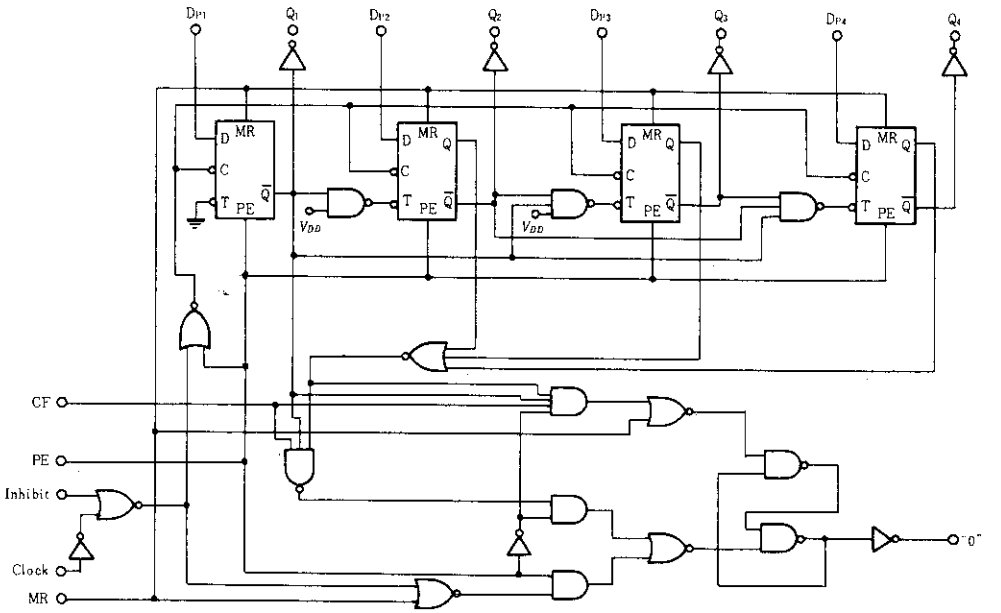
● HD14522B

Count	Q_4	Q_3	Q_2	Q_1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

● HD14526B

Count	Q_4	Q_3	Q_2	Q_1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

● HD14526B



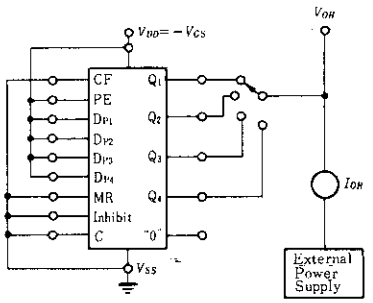
■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40℃ min	−40℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5$V	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
		5.0	$V_{OH}=4.6$V	−0.2	—	−0.16	−0.36	—	−0.12	—	
		10	$V_{OH}=9.5$V	−0.5	—	−0.4	−0.9	—	−0.3	—	
		15	$V_{OH}=13.5$V	−1.4	—	−1.2	−3.5	—	−1.0	—	
	I_{OL}	5.0	$V_{OL}=0.4$V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5$V	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5$V	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}	—	$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I_T	5.0	Dynamic+I_{DD}, per Gate $C_L=50$pF, $f=1$kHz	—	—	—	1.7	—	—	—	μA
		10		—	—	—	3.4	—	—	—	
		15		—	—	—	5.1	—	—	—	

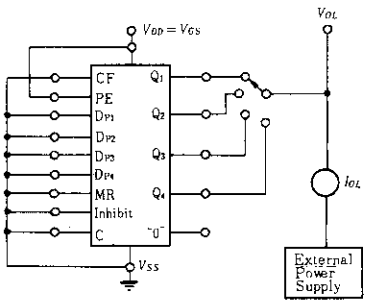
* To calculate total supply current at frequency other than 1kHz,
@V_{DD}=5.0V $I_T=(1.7\mu A/kHz)f+I_{DD}$, @$V_{DD}$=10V $I_T=(3.4\mu A/kHz)f+I_{DD}$, @$V_{DD}$=15V $I_T=(5.1\mu A/kHz)f+I_{DD}$

■DC CHARACTERISTIC TEST CIRCUIT

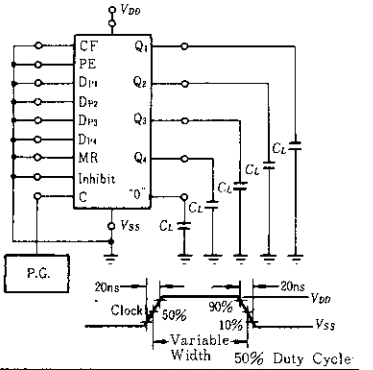
●I_{OH}



●I_{OL}



●POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

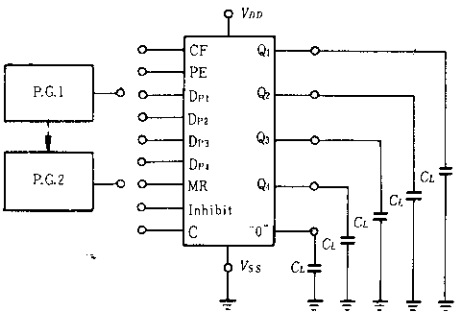


■SWITCHING CHARACTERISTICS ($C_L=50$ pF, $Ta=25$℃)

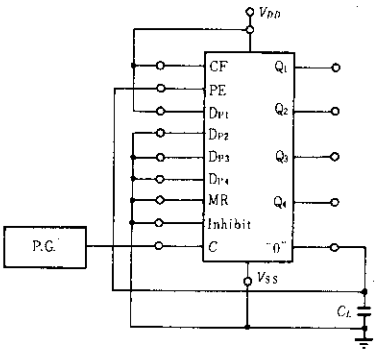
Characteristic		Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		t_f	5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	Q Outputs	t_{PLH}, t_{PHL}	5.0	—	550	1100	ns
			10	—	230	450	
			15	—	160	340	
	"0" Outputs		5.0	—	240	500	
			10	—	120	300	
			15	—	90	225	
Clock Pulse Width		PW_C	5.0	300	100	—	ns
			10	150	50	—	
			15	115	40	—	
Clock Frequency		PRF	5.0	—	2.0	1.0	MHz
			10	—	5.0	2.5	
			15	—	6.6	3.0	
Maximum Clock or Inhibit Rise and Fall Time		t_r, t_f	5.0	—	—	15	μs
			10	—	—	15	
			15	—	—	15	
Hold Time		t_{hold}	5.0	150	75	—	ns
			10	75	25	—	
			15	60	20	—	
Minimum Preset Enable Pulse Width		PW_{PE}	5.0	300	100	—	ns
			10	150	50	—	
			15	115	40	—	
Minimum Master Reset Pulse Width		PW_{MR}	5.0	350	200	—	ns
			10	300	100	—	
			15	225	75	—	

■ SWITCHING TIME TEST CIRCUIT

● Test No. 1 ~ 6

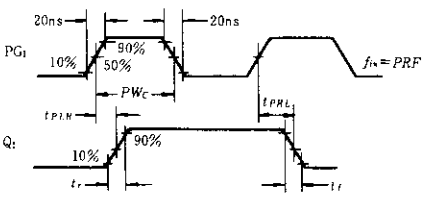


● Test No. 7



■ AC TEST METHOD AND SWITCHING WAVEFORMS

● Test No. 1



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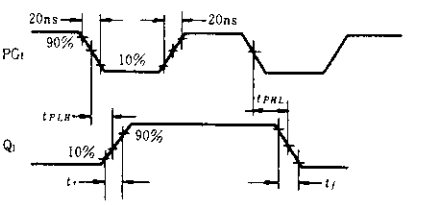

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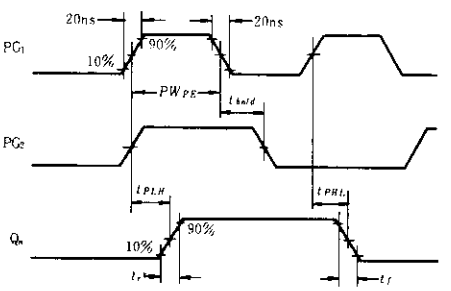

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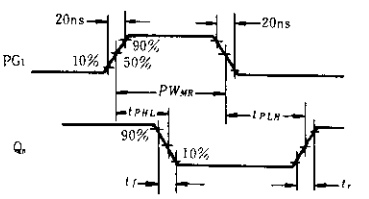
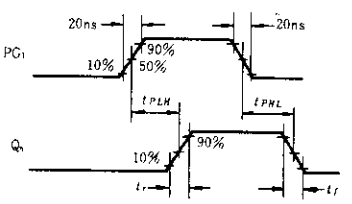
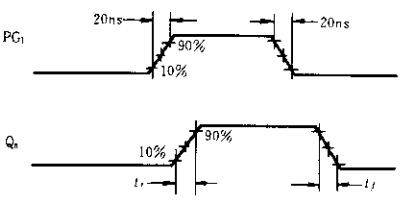


● Test No. 5 & 7

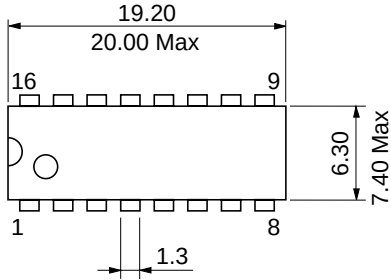


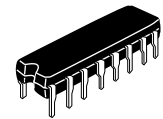
● Test No. 6

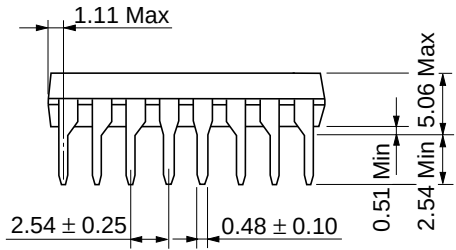


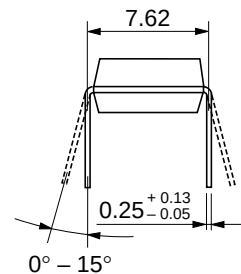
Characteristic	Test No.	Clock	Inhibit	PE	MR	D_{Pn}	CF	Output
t_r, t_f, t_{PLH}, t_{PHL}	1	PG_1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q_1
	2	V_{DD}	PG_1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q_1
	3	V_{SS}	V_{SS}	PG_1	V_{SS}	PG_2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG_1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG_1	V_{SS}	Q_n
PW_{MR}	4	V_{SS}	V_{SS}	V_{DD}	PG_1	V_{DD}	V_{SS}	Q_n
PW_{PE}	3	V_{SS}	V_{SS}	PG_1	V_{SS}	PG_2	V_{SS}	Q_n
PW_C	1	PG_1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q_1
PRF	1	PG_1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q_1
t_{hold}	3	V_{SS}	V_{SS}	PG_1	V_{SS}	PG_2	V_{SS}	Q_n
t_r, t_f	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG_1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	See Test Circuit	V_{SS}	See Test Circuit	V_{DD}	"0"

Unit: mm









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