HD14519B

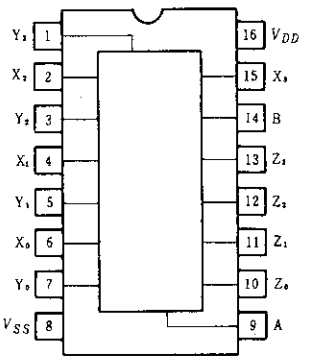
4-bit AND/OR Selector or Quadruple 2-Channel Data Selector or Quadruple Exclusive-NOR Gate

The HD14519B finds primary use where low power dissipation and/or high noise immunity is desired. This device exemplifies the design versatility of CMOS logic structure. This part provides three functions in one package; a 4-bit AND/OR Selector, a Quad 2-channel Data Selector, or a Quad Exclusive NOR Gate.

■ FEATURES

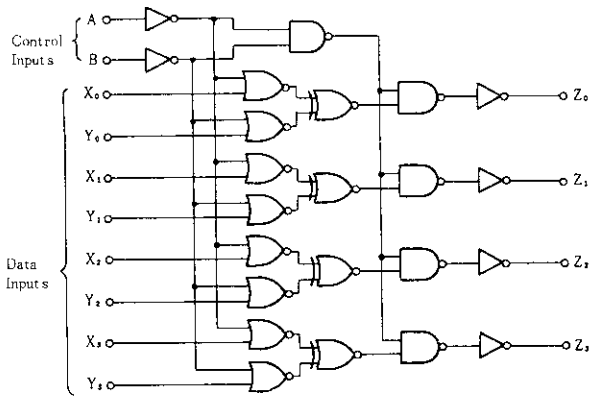
- Quiescent Current = 5nA/pkg typ. @5V
- Noise Immunity = 45% of V_{DD} typ.
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Compatible with HD14519B.

■ PIN ARRANGEMENT



(Top View)

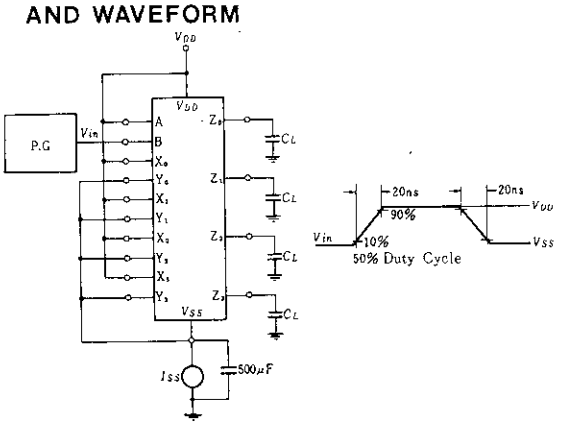
■ LOGIC DIAGRAM



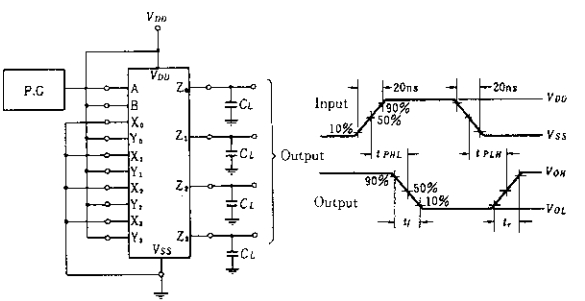
■ TRUTH TABLE

Control Inputs		Outputs
A	B	Zn
0	0	0
0	1	Yn
1	0	Xn
1	1	$\overline{Xn \oplus Yn}$

■ POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



■ SWITCHING TIME TEST CIRCUIT



■ELECTRICAL CHARACTERISTICS

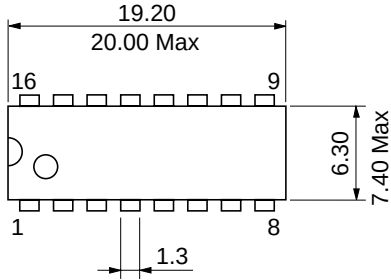
Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40°C min	−40°C max	25°C min	25°C typ	25°C max	85°C min	85°C max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	V_{out}=4.5 or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	V_{out}=9.0 or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	V_{out}=13.5 or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	V_{out}=0.5 or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	V_{out}=1.0 or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	V_{out}=1.5 or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	V_{OH}=2.5V	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
		5.0	V_{OH}=4.6V	−0.2	—	−0.16	−0.36	—	−0.12	—	
		10	V_{OH}=9.5V	−0.5	—	−0.4	−0.9	—	−0.3	—	
		15	V_{OH}=13.5V	−1.4	—	−1.2	−3.5	—	−1.0	—	
	I_{OL}	5.0	V_{OL}=0.4V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	V_{OL}=0.5V	1.3	—	1.1	2.25	—	0.9	—	
		15	V_{OL}=1.5V	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}		V_{in}=0	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I_T	5.0	Dynamic+I_{DD}, C_L=50pF, f=1 kHz per Gate	—	—	—	1.2	—	—	—	μA
		10		—	—	—	2.4	—	—	—	
		15		—	—	—	3.6	—	—	—	
Three-State Output Leakage Current	I_{TL}	15		—	±1.0	—	±0.00001	±1.0	—	±7.5	μA

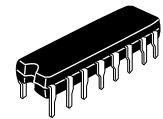
* To calculate total supply current at frequency other than 1kHz.
@ V_{DD}=5.0V $I_T=(1.2\mu A/kHz)f+I_{DD}$ @ V_{DD}=10V $I_T=(2.4\mu A/kHz)f+I_{DD}$ @ V_{DD}=15V $I_T=(3.6\mu A/kHz)f+I_{DD}$

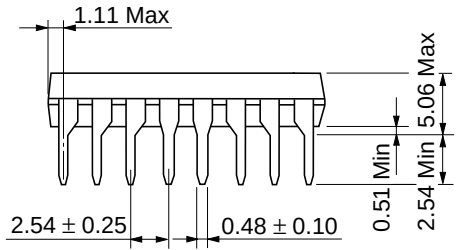
■SWITCHING CHARACTERISTICS (C_L=50pF, Ta=25°C)

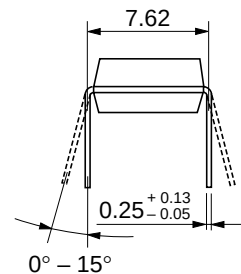
Characteristic	Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time	t_r	5.0	—	180	400	ns
		10	—	90	200	
		15	—	65	160	
Output Fall Time	t_f	5.0	—	100	200	ns
		10	—	50	100	
		15	—	37	80	
Propagation Delay Time	t_{PLH}	5.0	—	250	500	ns
		10	—	115	225	
		15	—	90	165	
	t_{PHL}	5.0	—	250	500	ns
		10	—	115	225	
		15	—	90	165	

Unit: mm









Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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