HD66728

(112 x 80-dot Graphics LCD Controller/Driver)

HITACHI

Preliminary
Rev 0.5
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Description

The HD66728, 112-by-80 dot-matrix graphics LCD controller and driver LSI, displays characters such as alphanumerics, katakana, hiragana and symbols as well as graphics such as kanji and pictograms. It can be configured to drive a dot-matrix liquid crystal display and control key scan functions under the control of the microprocessor connected via the clock-synchronized serial or 4/8-bit bus. The HD66728 has a smooth vertical scroll display and a double-height display for the remaining bit map areas. It fixed-displays a part of the graphics icons so that the user can easily see a variety of information.

The HD66728 has various functions to reduce the power consumption of an LCD system such as low-voltage operation of 1.8 V min., a booster to generate maximum five-times LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions such as standby and sleep modes allows fine power control. The HD66728 is suitable for any portable battery-driven product requiring long-term driving capabilities such as cellular phones, pagers, or electronic wallets.

Features

- Control and drive of a character and graphics LCD
- 112 x 80-dot graphics and 16-character x 10-line display
- Combined display (superimposed display) of graphics and characters
- Fixed display of graphics icons (pictograms)
- Control up to a 4 × 8 (32-key) matrix key scan.
- 3 general ports built-in
- Low-power operation support:
  - — Vcc = 1.8 to 5.5 V (low voltage)
  - — V_{LCD} = 4.5 to 15.0 V (liquid crystal drive voltage)
  - — Triple, quadruple, or five-times booster for liquid crystal drive voltage
  - — 64-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors

  - — Power-save functions such as the standby mode and sleep mode supported
  - — Wake-up feature using key scan interrupt
  - — Programmable drive duty ratios and bias values displayed on LCD
- High-speed clock-synchronized serial interface (serial transfer rate: 5 MHz max.)
- High-speed 4-/8-bit bus interface capability (except when key scan circuit is used)
- 112-segment × 80-common liquid crystal display driver
- 160-byte display data RAM (160 characters max)
- 20,736-bit (6 × 8 dots : 432 characters) character generator ROM
- 1,120-byte (112 × 80 dots) character generator RAM
- Vertical smooth scroll
- Partial smooth scroll control (fixed display of graphics icons)
- Vertical double-height display by each display line
- Black-and-white reversed display
- Selectable CGROM memory bank by each display line (max. 432 fonts)
- Wide range of instruction functions:
  - — Clear display, display on/off control, character blink, black-and-white reversed blink cursor, return home, cursor on/off, black-and-white reversed raster-row
- Synchronous blink-cycle function (for blink display by second colon)
- No wait time for instruction execution and RAM access
- Internal oscillation and hardware reset
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Shift change of segment and common driver
- Slim chip with bumps for chip-on-glass (COG) mounting, and tape carrier package (TCP)

Table 1 Progammable Display Sizes and Duty Ratios

		Graphics Display				Character Display
Duty Ratio	**Optimum Drive Bias**	**Bit Map**	**12 x 13-dot Font Width**	**14 x 15-dot Font Width**	**16 x 16-dot Font Width**	**6 x 8-dot Font Width**
1/32	1/7	112 x 32 dots	2 lines x 9 characters	2 lines x 8 characters	2 lines x 7 characters	4 lines x 16 characters
1/40	1/7	112 x 40 dots	3 lines x 9 characters	2.5 lines x 8 characters	2.5 lines x 7 characters	5 line x 16 characters
1/48	1/8	112 x 48 dots	3 lines x 9 characters	3 lines x 8 characters	3 line x 7 characters	6 lines x 16 characters
1/56	1/8	112 x 56 dots	4 lines x 9 characters	3.5 lines x 8 characters	3.5 lines x 7 characters	7 lines x 16 characters
1/64	1/9	112 x 64 dots	5 lines x 9 characters	4 lines x 8 characters	4 lines x 7 characters	8 lines x 16 characters
1/72	1/9.5	112 x 72 dots	6 lines x 9 characters	4.5 lines x 8 characters	4.5 lines x 7 characters	9 lines x 16 characters
1/80	1/10	112 x 80 dots	6 lines x 9 characters	5 lines x 8 characters	5 lines x 7 characters	10 lines x 16 characters

<Target values>

Total Current Consumption Characteristics (Vcc = 3 V, TYP Conditions, LCD Drive Power Current Included)

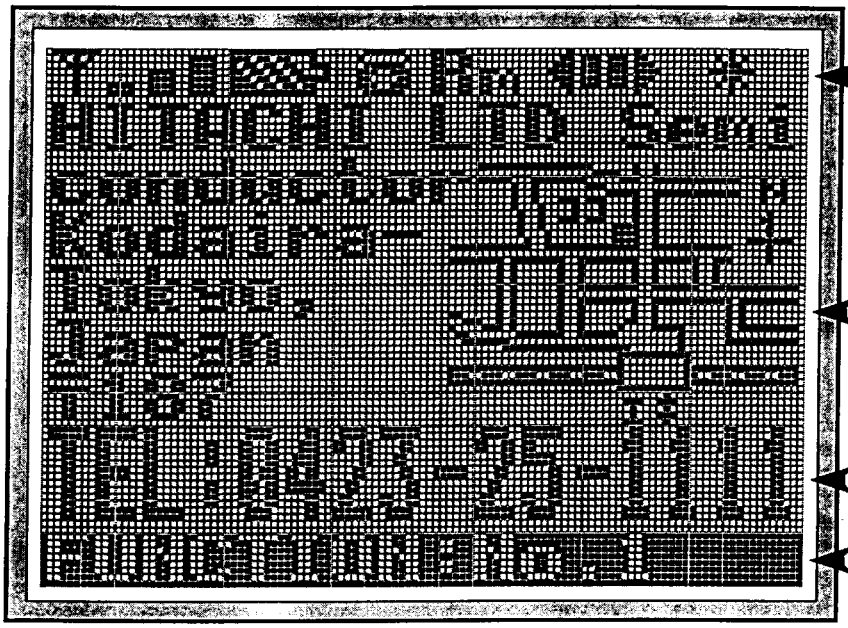
				Total Power Consumption				
				Normal Display Operation				
Character Display Dot Size	Duty Ratio	R-C Oscillation Frequency	Frame Frequency	Internal Logic	LCD Power	Total*	Sleep Mode	Standby Mode
112 x 32 dots	1/32	75 kHz	73 Hz	(27 µA)	(16 µA)	Triple (75 µA)	(15 µA)	0.1 µA
112 x 40 dots	1/40	75 kHz	73 Hz	(27 µA)	(16 µA)	Triple (75 µA)	(15 µA)	
112 x 48 dots	1/48	75 kHz	74 Hz	(27 µA)	(16 µA)	Triple (75 µA)	(15 µA)	
112 x 56 dots	1/56	75 kHz	74 Hz	(27 µA)	(16 µA)	Triple (75 µA)	(15 µA)	
112 x 64 dots	1/64	75 kHz	73 Hz	(27 µA)	(18 µA)	Quadruple (99 µA)	(15 µA)	
112 x 72 dots	1/72	80 kHz	70 Hz	(32 µA)	(18 µA)	Quadruple (104 µA)	(15 µA)	
112 x 80 dots	1/80	90 kHz	70 Hz	(35 µA)	(20 µA)	Five-times (135 µA)	(15 µA)	

Note : When a triple, quadruple, or five-times booster is used:
the total power consumption = Internal logic current + LCD power current x 3 (triple booster),
the total power consumption = Internal logic current + LCD power current x 4 (quadruple booster), and
the total power consumption = Internal logic current + LCD power current x 5 (five-times booster)

Type Name

Types	External Dimensions	Operation Voltages	Internal Fonts
HD66728A05TB0	Bending TCP	1.8 V to 5.5 V	Katakana, alphanumerics, symbols and
HCD66728A05BP	Au-bumped chip		European fonts

LCD Display Example



- 1/80 duty
- Graphics display area: 112 x 80 dots (dot matrix)
- Text display area: 16 characters x 10 lines
- Graphics-icon (pictogram) display at the top and bottom of the screen

Figure 1 LCD Display Example

System Configuration Example

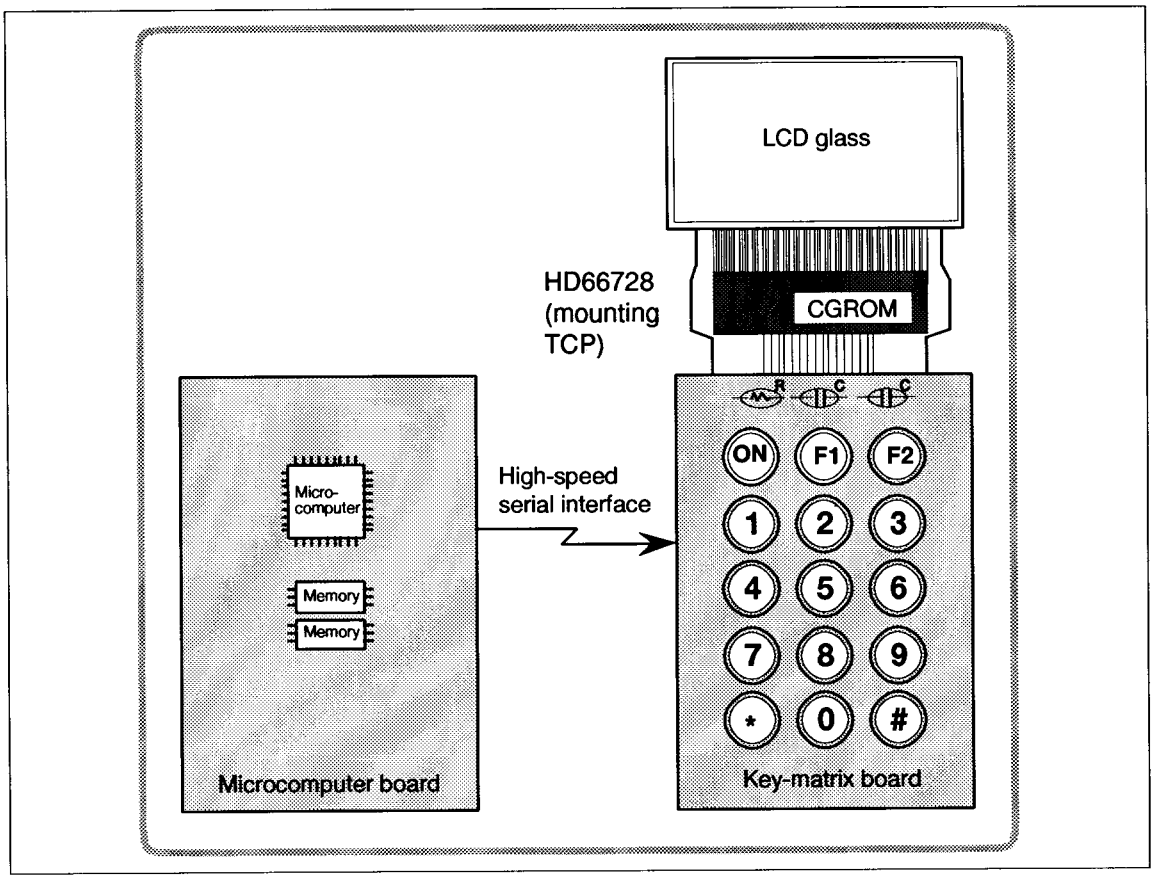


Figure 2 System Configuration Example

LCD Specification Comparison

Items	HD44780U	HD66701	HD66702R	HD66710
Character display sizes	8 characters x 2 lines	16 characters x 2 lines	20 characters x 2 lines	8 characters x 4 lines
Graphic display sizes	—	—	—	—
Multiplexing icons	—	—	—	40
Annunciator	—	—	—	—
Key scan control	—	—	—	—
LED control port	—	—	—	—
General output port	—	—	—	—
Operating power voltages	2.7 V to 5.5 V	2.7 V to 5.5 V	2.7 V to 5.5 V	2.7 V to 5.5 V
Liquid crystal drive voltages	3 V to 11 V	2.7 V to 8.3 V	3 V to 8.3 V	3 V to 13 V
Serial bus	—	—	—	—
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Expansion driver control	Possible	Impossible	Possible	Used in common with SEGDr
Liquid crystal drive duty ratios	1/8, 11, 16	1/8, 11, 16	1/8, 11, 16	1/17, 33
Liquid crystal drive biases	1/4 to 1/5	1/2 to 1/5	1/4 to 1/5	1/4 to 1/6.7
Liquid crystal drive waveforms	A	B	B	B
Liquid crystal voltage booster	—	—	—	Double or triple
Bleeder-resistor for liquid crystal drive	External	External	External	External
Liquid crystal drive operational amplifier	—	—	—	—
Liquid crystal contrast adjuster	—	—	—	—
Horizontal smooth scroll	—	—	—	Dot unit
Vertical smooth scroll	—	—	—	—
Double-height display	—	—	—	—
DDRAM	80 × 8	40 x 8	80 x 8	80 x 8
CGROM	9.960	7,200	7,200	9,600
CGRAM	64 x 8	64 x 8	64 x 8	64 x 8
SEGRAM	—	—	—	8 x 8
No. of CGROM fonts	240	192	192	240
No. of CGRAM fonts	8	8	8	8
Font sizes	5 x 8, 5 x 10	5 x 7, 5 x 10	5 x 7, 5 x 10	5 x 8
Bit map area	—	—	—	—
R-C oscillation resistor/ oscillation frequency	External resistor (270 kHz)	External resistor (320 kHz)	External resistor (320 kHz)	External resistor (270 kHz)
Reset function	Incorporated	Incorporated	Incorporated	Incorporated
Low power control		Low bias drive		LP display mode
SEG/COM direction switching	—	—	—	—
QFP package	QFP-1420	—	—	QFP-1420
TQFP package	TQFP-1414	—	LQFP-2020	TQFP-1414
TCP package	—	—	—	—
Bare chip	Yes	Yes	Yes	Yes
Bumped chip	—	—	—	—
No. of pins	80	120	144	100
Chip sizes	4.90 x 4.90	5.20 x 5.20	5.20 x 5.20	5.63 x 6.06
Pad intervals	160 μm	130 μm	130 μm	160 μm

LCD-II Family Comparison (cont)

Items	HD66712U	HD66720	HD66705U
Character display sizes	12 characters x 4 lines	8 characters x 2 lines	12 characters x 2 lines
Graphic display sizes	—	—	—
Multiplexing icons	60	42	40
Annunciator	—	—	Static: 10
Key scan control	—	5 x 6	—
LED control ports	—	2	—
General output port	—	—	—
Operating power voltages	2.7 V to 5.5 V	2.7 V to 5.5 V	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 13 V	3 V to 11 V	3 V to 9 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	—	4 bits, 8 bits
Expansion driver control	Possible	Possible	Impossible
Liquid crystal drive duty ratios	1/17, 33	1/9, 17	1/10, 18
Liquid crystal drive biases	1/4 to 1/6, 7	1/4 to 1/5	1/4
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Double or triple	Double or triple	Double or triple
Bleeder-resistor for liquid crystal drive	External	External	Incorporated (external)
Liquid crystal drive operational amplifier	—	—	Incorporated
Liquid crystal contrast adjuster	—	—	Incorporated
Horizontal smooth scroll	Dot unit	Dot unit	—
Vertical smooth scroll	—	—	Line unit
Double-height display	—	—	Yes
DDRAM	80 x 8	40 x 8	60 x 8
CGROM	9,600	9,600	9,600
CGRAM	64 x 8	64 x 8	32 x 5
SEGRAM	16 x 8	16 x 8	8 x 5
No. of CGROM fonts	240	240	240
No. of CGRAM fonts	8	8	4
Font sizes	5 x 8	5 x 8	5 x 8
Bit map area	—	—	—
R-C oscillation resistor/oscillation frequency	External resistor (270 kHz)	External resistor (150 kHz)	External resistor (40, 80 kHz)
Reset function	Incorporated, external	Incorporated, external	External
Low power control	LP display mode	LP display mode Simple standby	Partial display off Oscillation off Liquid crystal power off
SEG/COM direction switching	—	—	SEG only
QFP package	(S mask)	QFP-1420	—
TQFP package	—	TQFP-1414	—
TCP package	TCP-128	—	TCP-153
Bare chip	Yes	Yes	Yes
Bumped chip	Yes	—	Yes
No. of pins	128	100	153
Chip sizes	4.95 x 5.27	5.60 x 6.00	9.69 x 2.73
Pad intervals	128 μm	160 μm	120 μm

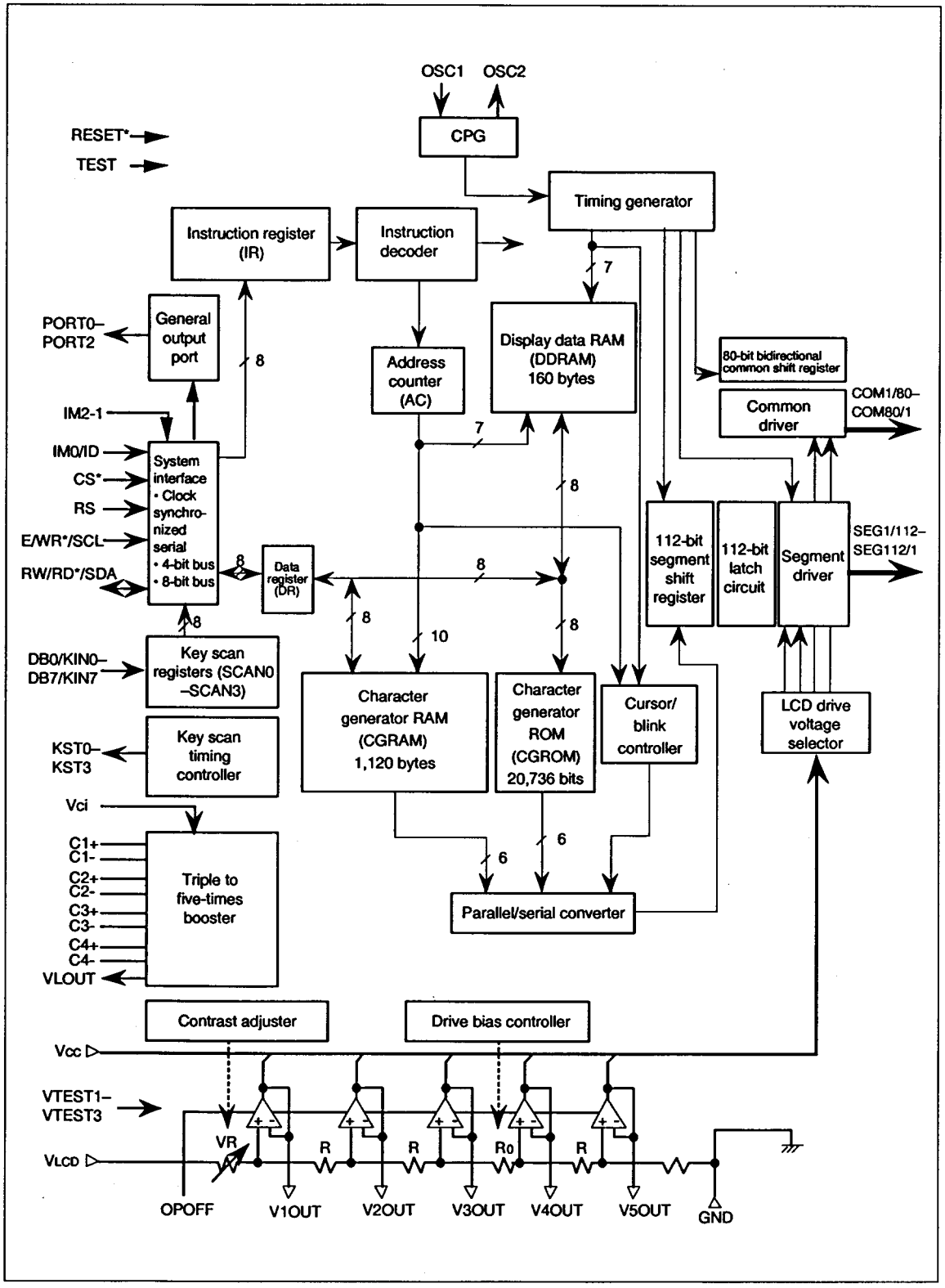
LCD-II Family Comparison (cont)

Items	HD66717	HD66727	HD66724
Character display sizes	12 characters x 4 lines	12 characters x 4 lines	12 characters x 3 lines
Graphic display sizes	—	—	72 x 26 dots
Multiplexing icons	40	40	144
Annunciator	Static: 10	Static: 12	1/2 duty: 144
Key scan control	—	4 x 8	8 x 4
LED control ports	—	3	—
General output ports	—	3	3
Operating power voltages	2.4 V to 5.5 V	2.4 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	3 V to 13 V	3 V to 13 V	3 V to 6 V
Serial bus	I2C, Clock-synchronized serial	I2C, Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	—	4 bits, 8 bits
Expansion driver control	Impossible	Impossible	Impossible
Liquid crystal drive duty ratios	1/10, 18, 26, 34	1/10, 18, 26, 34	1/2, 10, 18, 26
Liquid crystal drive biases	1/4, 1/6	1/4, 1/6	1/4 to 1/6.5
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Double or triple	Double or triple	Single, double or triple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	—	—	3-dot unit
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	60 x 8	60 x 8	80 x 8
CGROM	9,600	11,520	20,736
CGRAM	32 x 5	32 x 6	384 x 8
SEGRAM	8 x 5	8 x 6	72 x 8
No. of CGROM fonts	240	240	240 + 192
No. of CGRAM fonts	4	4	64
Font sizes	5 x 8	5 x 8, 6 x 8	6 x 8
Bit map area	—	—	72 x 26
R-C oscillation resistor/ oscillation frequency	External resistor (40-160 kHz)	External resistor (40-160 kHz)	External resistor, incorporated (32 kHz)
Reset function	External	External	External
Low power control	Partial display off Oscillation off Liquid crystal power off	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG only	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-153	TCP-158	TCP-146
Bare chip	Yes	Yes	—
Bumped chip	Yes	Yes	Yes
No. of pins	153	158	146
Chip sizes	10.88 x 2.89	11.39 x 2.89	10.34 x 2.51
Pad intervals	120 μm	120 μm	80 μm

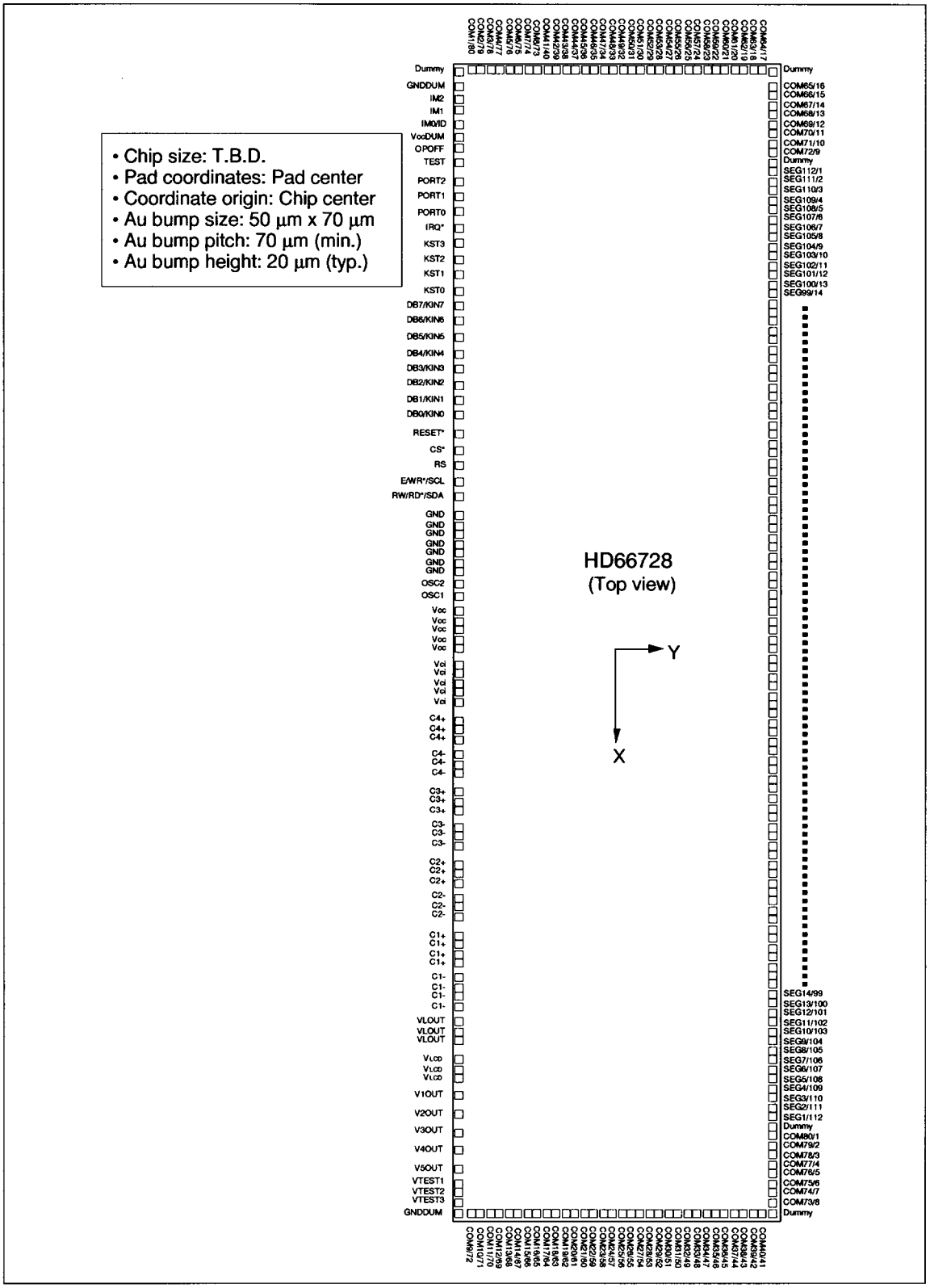
LCD-II Family Comparison (cont)

Items	HD66725	HD66726	(Under development) HD66728
Character display sizes	16 characters x 3 lines	16 characters x 5 lines	16 characters x 10 lines
Graphic display sizes	96 x 26 dots	96 x 42 dots	112 x 80 dots
Multiplexing icons	192	192	—
Annunciator	1/2 duty: 192	1/2 duty: 192	—
Key scan control	8 x 4	8 x 4	8 x 4
LED control ports	—	—	—
General output ports	3	3	3
Operating power voltages	1.8 V to 5.5 V	1.3 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	3 V to 6 V	4 V to 13 V	4.5 V to 15 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Expansion driver control	Impossible	Impossible	Impossible
Liquid crystal drive duty ratios	1/2, 10, 18, 26	1/2, 10, 18, 26, 34, 42	1/8, 16, 24, 32, 40, 48, 56, 64, 72, 80
Liquid crystal drive biases	1/4 to 1/6.5	1/2 to 1/8	1/4 to 1/10
Liquid crystal drive waveforms	B	B	B, C
Liquid crystal voltage booster	Single, double, or triple	Single, double, triple, or quadruple	Triple, quadruple, or five-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	3-dot unit	—	—
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	80 x 8	80 x 8	160 x 8
CGROM	20,736	20,736	20,736
CGRAM	384 x 8	480 x 8	1,120 x 8
SEGRAM	96 x 8	96 x 8	—
No. of CGROM fonts	240 + 192	240 + 192	240 + 192
No. of CGRAM fonts	64	64	64
Font sizes	6 x 8	6 x 8	6 x 8
Bit map areas	96 x 26	96 x 42	112 x 80
R-C oscillation resistor/ oscillation frequency	External resistor, incorporated (32 kHz)	External resistor, incorporated (50 kHz)	External resistor (70–90 kHz)
Reset function	External	External	External
Low power control	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-170	TCP-188	TCP-243
Bare chip	—	Yes	—
Bumped chip	Yes	Yes	Yes
No. of pins	170	188	243
Chip sizes	10.97 x 2.51	13.13 x 2.51	T.B.D.
Pad intervals	80 μm	100 μm	70 μm

HD66728 Block Diagram

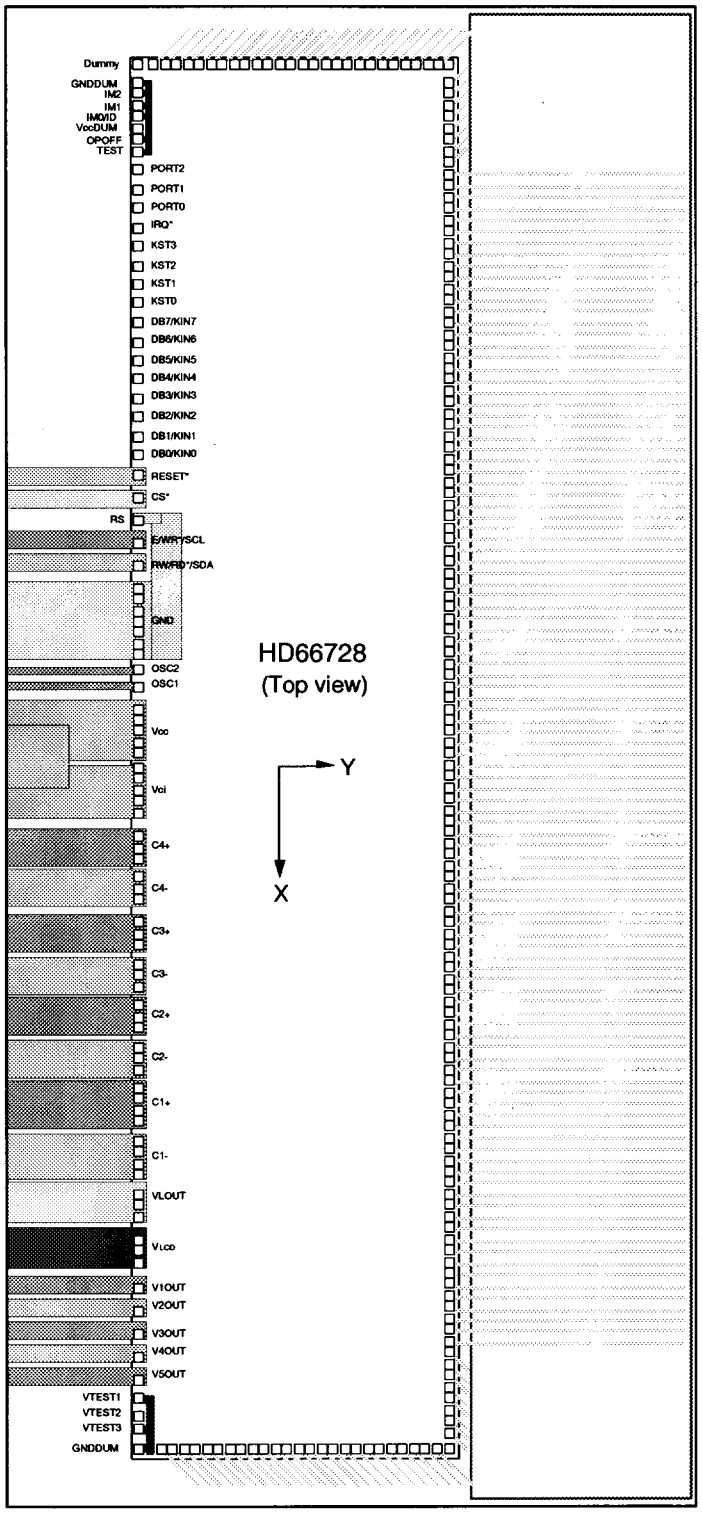


HD66728 Pad Arrangement

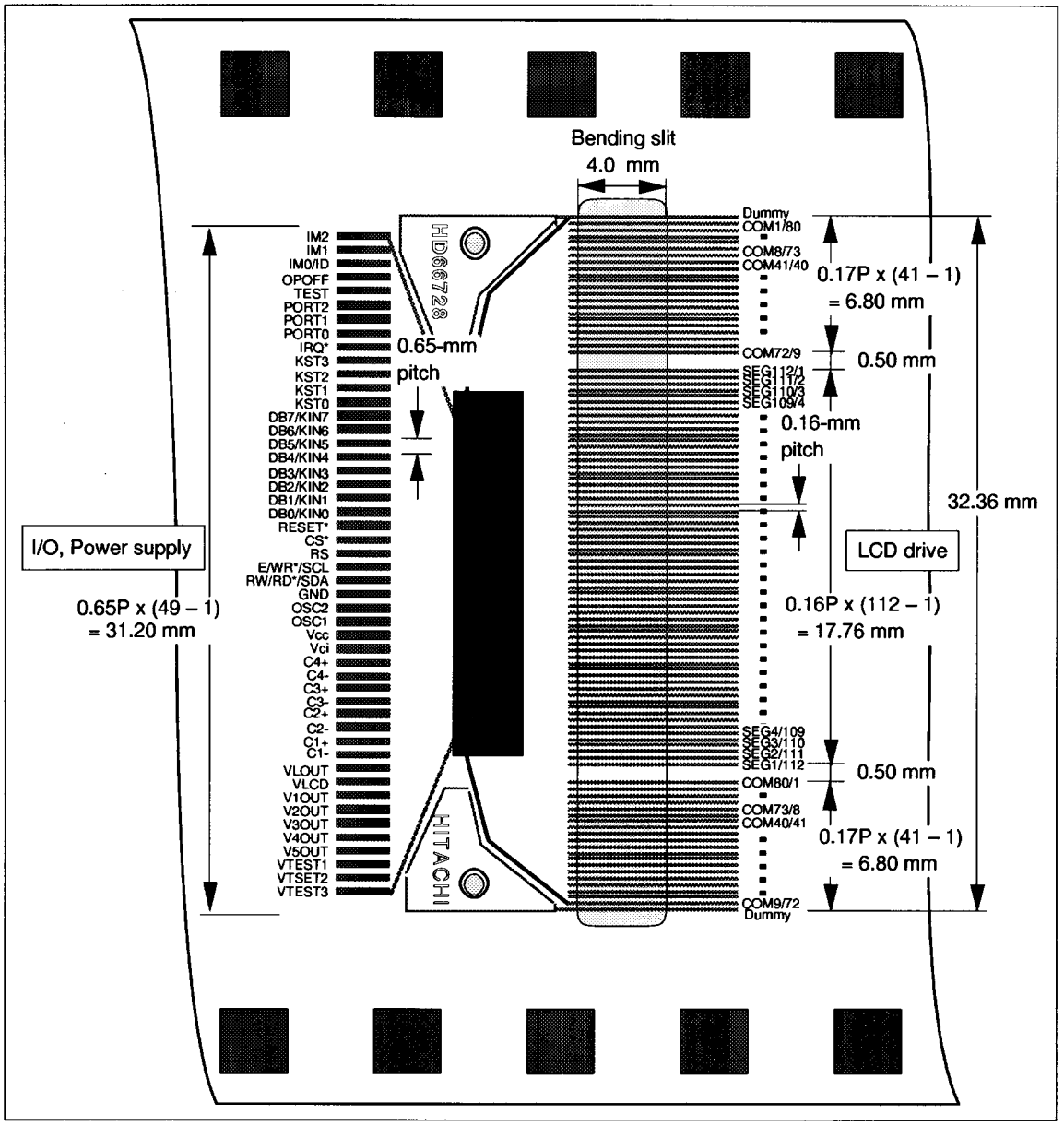


Chip-on-Glass (COG) Routing Example

- Clock-synchronized serial bus
- Unused key scan
- Unused port output
- Five-times booster
- Internal operational amplifier



TCP Dimensions (HD66728xxxTB0)



Pin Functions

Table 2 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM2, IM1	2	I	GND or V_{cc}	Selects the MPU interface mode: IM2 "GND" IM1 "GND" — Clock-synchronized serial interface IM2 "GND" IM1 "Vcc" — 68-system parallel bus interface IM2 "Vcc" IM1 "GND" — Setting inhibited IM2 "Vcc" IM1 "Vcc" — 80-system parallel bus interface
IM0/ID	1	I	GND or V_{cc}	Selects the transfer bus length for a parallel bus interface. GND: 8-bit bus, Vcc: 4-bit bus Inputs the ID of the device ID code for a serial bus interface.
CS*	1	I	MPU	Selects the HD66728: Low: HD66728 is selected and can be accessed High: HD66728 is not selected and cannot be accessed Must be fixed at GND level when not in use.
RS	1	I	MPU	Selects the register for a parallel bus interface. Low: Instruction High: RAM access Selects the key scan interrupt method in the standby period for a serial interface. Monitors a total of eight keys connected to KST0 at the GND level and monitors all keys at the Vcc level to generate an interrupt.
E/WR*/SCL	1	I	MPU	For an 80-system parallel bus interface, serves as a write strobe signal and writes data at the low level. For a 68-system parallel bus interface, serves as an enable signal to activate data read/write operation. Inputs the serial transfer clock for a serial interface. Fetches data at the rising edge of a clock.
RW/RD*/ SDA	1	I or I/O	MPU	For an 80-system parallel bus interface, serves as a write strobe signal and reads data at the low level. For a 68-system parallel bus interface, serves as a signal to select data read/write operation. Low: Write High: Read Serves as the bidirectional serial transfer data for a serial interface. Sends/Receives data.
IRQ*	1	O	MPU	Generates the key scan interrupt signal.
KST0– KST3	4	O	Key matrix	Generates strobe signals for latching scanned data from the key matrix at specific time intervals. Available for a serial interface only.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
DB0/KIN0–DB7/KIN7	8	I/O or I	MPU or key matrix	Serves as a bidirectional data bus for a parallel bus interface. For a 4-bit bus, data transfer uses KIN7/DB7-KIN4/DB4; leave KIN3/DB3-KIN0/DB0 disconnected. Samples key state from key matrix synchronously with strobe signals for a serial interface.
PORT0–PORT2	3	O	General output	General output ports. These ports cannot drive current such as for LEDs or backlighting control. Boost the current using an external transistor.
COM1/80–COM80/1	80	O	LCD	Common output signals for character/graphics display: COM1 to COM8 for the first line, COM9 to COM16 for the second line, COM17 to COM24 for the third line, COM25 to COM32 for the fourth line, and COM73 to COM80 for the 10th line. All the unused pins output unselected waveforms. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1/80 is COM1. If CMS = 1, COM1/80 is COM80. Note that the start position of the common output (the first line) is shifted by CN1–CN0 bits.
SEG1/112–SEG112/1	112	O	LCD	Segment output signals for character or graphics display. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, SEG1/112 is SEG1. If SGS = 1, SEG1/112 is SEG112.
V1OUT–V5OUT	5	I or O	Open or external bleeder-resistor	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins externally.
V_{LCD}	3	—	Power supply	Power supply for LCD drive. V_{LCD} – GND = 15 V max.
V_{CC}, GND	12	—	Power supply	V_{CC}: +1.8 V to +5.5 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation-resistor or clock	For R-C oscillation using an external resistor, connect an external resistor. For external clock supply, input clock pulses to OSC1.
Vci	5	I	Power supply	Inputs a reference voltage and supplies power to the booster; generates the liquid crystal display drive voltage from the operating voltage. The boosting output voltage must not be larger than the absolute maximum ratings. Must be left disconnected when the booster is not used.
VLOUT	3	O	V_{LCD} pin/booster capacitance	Potential difference between Vci and GND is triple- to five-times-boosted and then output. Magnitude of boost is selected by instruction.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
C1+, C1–	8	—	Booster capacitance	External capacitance should be connected here for boosting.
C2+, C2–	6	—	Booster capacitance	External capacitance should be connected here when using the triple or more booster.
C3+, C3–	6	—	Booster capacitance	External capacitance should be connected here when using the quadruple and five-times booster.
C4+, C4–	6	—	Booster capacitance	External capacitance should be connected here when using the five-times booster.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low.
OPOFF	1	I	V_{cc} or GND	Turns the internal operational amplifier off when OPOFF = V_{cc}, and turns it on when OPOFF = GND. If the amplifier is turned off (OPOFF = V_{cc}), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
VccDUM	1	O	Input pins	Outputs the internal V_{cc} level; shorting this pin sets the adjacent input pin to the V_{cc} level.
GNDDUM	1	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy	5	—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST1	1	I	GND or V_{cc}	Adjusts the driving capability of the internal operational amplifier for the LCD. This signal enters the normal drive mode in the GND side, and it enters the high-power drive mode in the V_{cc} side. When the display quality is not sufficient, use the high-power drive mode even though the power-consumption current is large.
VTEST2	1	—	—	Test pin. Must be left disconnected.
VTEST3	1	I	V_{cc} or GND	Adjusts the driving capability of the internal operational amplifier for the LCD. This signal enters the normal drive mode or high-power mode in the GND side according to the VTEST1 pin setting, and it enters the low-power drive mode in the V_{cc} side. Use this signal in the low-power mode so that the display quality is not lowered.

Block Function Description

System Interface

The HD66728 has five types of system interfaces, and a clock-synchronized serial, a 68-system 4-bit/8-bit bus, and a 80-system 4-bit/8-bit bus. The interface mode is selected by the IM2-0 pins. The key scan of the HD66728 is not available for the 4-bit/8-bit bus interface. Instead, use the clock-synchronized serial interface.

The HD66728 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as clear display, display control, and address information for the display data RAM (DDRAM) and character generator RAM (CGRAM).

The DR temporarily stores data to be written into the DDRAM or CGRAM. Data written into the DR from the MPU is automatically written into the DDRAM or CGRAM by internal operation. When address information is written into the IR, data is read and then stored in the DR from the DDRAM or CGRAM by internal operation. Data is read through the DR when reading from the RAM, and the first read data is invalid and the second and the following data are normal. After reading, data in the DDRAM or CGRAM at the next address is sent to the DR for the next reading from the MPU.

Execution time for instruction excluding clear display is 0 clock cycle and instructions can be written in succession.

Table 3 Register Selection by RS and R/W Bits

R/W Bits	RS Bits	Operations
0	0	Write instructions to IR
1	0	Read key scan data (SCAN0-3)
0	1	DR write as an internal operation (DR to DDRAM or CGRAM)
1	1	DR read as an internal operation (DDRAM or CGRAM to DR)

Key Scan Registers (SCAN0 to SCAN3)

The key matrix scanner senses and holds the key states at each rising edge of the key strobe signals that are output by the HD66728. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key status on eight inputs from KIN0 to KIN7, enabling up to 32 keys to be scanned.

The states of inputs KIN0 to KIN7 are sampled by key strobe signal KST0 and latched into register SCAN0. Similarly, the data sampled by strobe signals KST1 to KST3 is latched into registers SCAN1 to SCAN3, respectively.

General Output Ports (PORT0 to PORT 2)

The HD66728 has three general output ports. These ports control drive current such as that for LEDs or backlighting by using the current boosted by an external transistor.

Address Counter (AC)

The address counter (AC) assigns addresses to the DDRAM or CGRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC. Selection of the DDRAM and CGRAM is also determined concurrently by the RAM select bit (RM1/0).

After writing into the DDRAM or CGRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the RDM bit automatically updates or does not update the AC. The cursor display position is determined by the address counter value.

Display Data RAM (DDRAM)

The display data RAM (DDRAM) stores display data represented in 8-bit character codes in the character display mode. Its capacity is 160 × 8 bits, or 160 characters, which is equivalent to an area of 16 characters × 10 lines. Any number of display lines (LCD drive duty ratio) from 1 to 10 can be selected by software. Here, assignment of DDRAM addresses is the same for all display modes (table 5). The line to be displayed at the top of the display (display-start line) can also be selected by register settings. The graphics display mode does not use data in the DDRAM.

Character Generator ROM (CGROM)

The character generator ROM (CGROM) generates 6 × 8-dot character patterns from 8-bit character codes. It is equipped with a memory bank to generate 240 character patterns or 192 character patterns, switch able according to applications. For details, see the CGROM Bank Switching Function section. Table 6 illustrates the relation between character codes and character patterns for the Hitachi standard CGROM. User-defined character patterns are also available using a mask-programmed ROM (see the Modifying Character Patterns section).

Character Generator RAM (CGRAM)

The character generator RAM (CGRAM) allows the user to redefine the character patterns in the character display mode. Up to 64 character patterns of 7 x 8-dot characters can be simultaneously displayed. DRAM-specified character code can be selected to display one of these user font patterns.

The CGRAM serves as a RAM to store 112 x 80-dot bit pattern data in the graphics display mode. Here, display patterns are directly written into CGRAM. Character codes set in the DDRAM are not used. For details, see the Graphics Display section.

The CGRAM stores the bit-pattern data in the superimposed display mode as well as in the graphics display mode. Here, the CGRAM cannot be used for displaying the user font pattern as the character. For details, see the Superimposed Display Function section.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the DDRAM, CGROM, and CGRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. This prevents flickering in areas other than the display area when writing data to the DDRAM, for example.

Cursor/Blink Controller

The cursor/blink (or black-and-white reversed) control is used to create a cursor or a flashing area on the display in a position corresponding to the location stored in the address counter (AC).

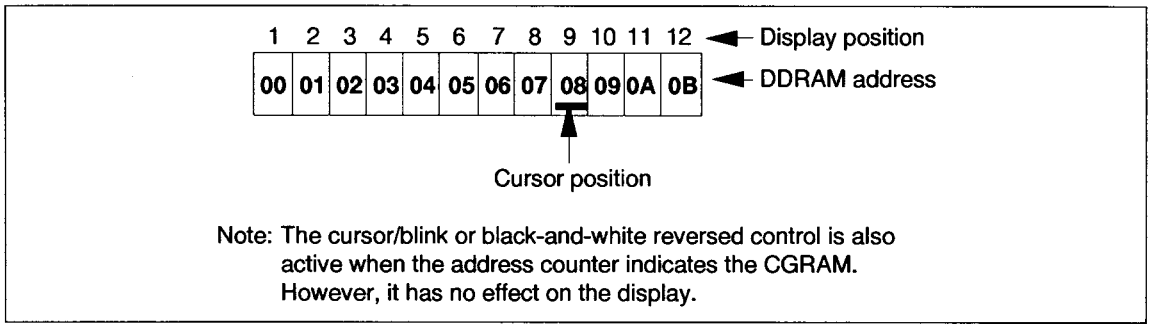


Figure 3 Cursor Position and DDRAM Address (AC = 08H)

Oscillation Circuit (OSC)

The HD66728 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 80 common signal drivers (COM1 to COM80) and 112 segment signal drivers (SEG1 to SEG112). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output unselected waveforms.

Character pattern data is sent serially through a 112-bit shift register and latched when all needed data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs.

The shift direction of 112-bit data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Booster (DC-DC Converter)

The booster generates triple, quadruple, or five-times voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Boost output level from triple to five-times boost can be selected by software. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/4 bias to 1/10 bias, according to the liquid crystal display drive duty value. The voltage followers can be turned off while multiplexing drive is not being used. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 64 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

DDRAM Address Map

Table 4 DDRAM Addresses and Display Positions

Display Line	1st Char.	2nd Char.	3rd Char.	4th Char.	5th Char.	6th Char.	7th Char.	8th Char.	9th Char.	10th Char.	11th Char.	12th Char.	13th Char.	14th Char.	15th Char.	16th Char.
1st	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
3rd	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
4th	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
5th	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
6th	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
7th	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F
8th	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
9th	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
10th	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F

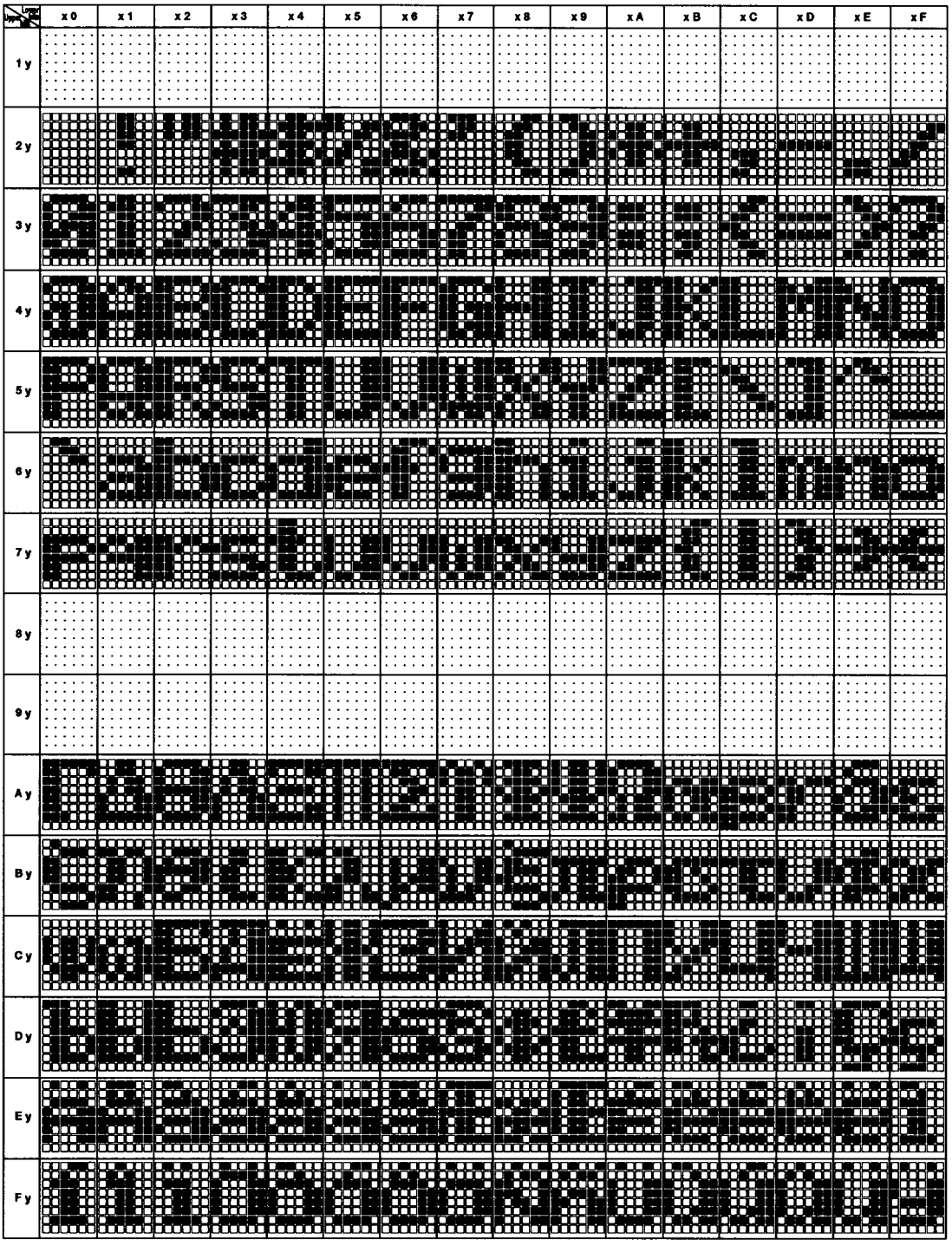
Note: When SGS = 0, SEG1/112 to SEG7/106 appear at the first character at the extreme left of the screen.
When SGS = 1, SEG112/1 to SEG106/7 appear at the first character at the extreme left of the screen.

Table 5 **Display-line Modes, Display-start Line, and DDRAM Addresses (10-line Display Mode)**

	Display-start Lines (SN3–0)									
Common Driver	1st Line (0000)	2nd Line (0001)	3rd Line (0010)	4th Line (0011)	5th Line (0100)	6th Line (0101)	7th Line (0110)	8th Line (0111)	9th Line (1000)	10th Line (1001)
COM1–COM8	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH	50H–5FH	60H–6FH	70H–7FH	80H–8FH	90H–9FH
COM9–COM16	10H–1FH	20H–2FH	30H–3FH	40H–4FH	50H–5FH	60H–6FH	70H–7FH	80H–8FH	90H–9FH	00H–0FH
COM17–COM24	20H–2FH	30H–3FH	40H–4FH	50H–5FH	60H–6FH	70H–7FH	80H–8FH	90H–9FH	00H–0FH	10H–1FH
COM25–COM32	30H–3FH	40H–4FH	50H–5FH	60H–6FH	70H–7FH	80H–8FH	90H–9FH	00H–0FH	10H–1FH	20H–2FH
COM33–COM40	40H–4FH	50H–5FH	60H–6FH	70H–7FH	80H–8FH	90H–9FH	00H–0FH	10H–1FH	20H–2FH	30H–3FH
COM41–COM48	50H–5FH	60H–6FH	70H–7FH	80H–8FH	90H–9FH	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH
COM49–COM56	60H–6FH	70H–7FH	80H–8FH	90H–9FH	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH	50H–5FH
COM57–COM64	70H–7FH	80H–8FH	90H–9FH	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH	50H–5FH	60H–6FH
COM65–COM72	80H–8FH	90H–9FH	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH	50H–5FH	60H–6FH	70H–7FH
COM73–COM80	90H–9FH	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH	50H–5FH	60H–6FH	70H–7FH	80H–8FH

Table 6 CGROM Memory Bank 0 (ROM Bit = 0)

Table 7 CGROM Memory Bank 1 (ROM Bit = 1)



CGRAM Address Map

Table 8 Relationship between Character Code in Character Display Mode (GR = 0) and CGRAM (RM = 1) Address

Font Bank	Memory Bank: ROM = 0, 1															
Character Code	"00"H	"01"H	"02"H	"03"H	"04"H	"05"H	"06"H	"07"H	"08"H	"09"H	"0A"H	"0B"H	"0C"H	"0D"H	"0E"H	"0F"H
CGRAM Address (HEX)	000 to 006	007 to 00D	00E to 014	015 to 01B	01C to 022	023 to 029	02A to 030	031 to 037	038 to 03E	03F to 045	046 to 04C	04D to 053	054 to 05A	05B to 061	062 to 068	069 to 06F
Font Bank	Memory Bank: ROM = 1															
Character Code	"10"H	"11"H	"12"H	"13"H	"14"H	"15"H	"16"H	"17"H	"18"H	"19"H	"1A"H	"1B"H	"1C"H	"1D"H	"1E"H	"1F"H
CGRAM Address (HEX)	080 to 086	087 to 08D	08E to 094	095 to 09B	09C to 0A2	0A3 to 0A9	0AA to 0B0	0B1 to 0B7	0B8 to 0BE	0BF to 0C5	0C6 to 0CC	0CD to 0D3	0D4 to 0DA	0DB to 0E1	0E2 to 0E8	0E9 to 0EF
Font Bank	Memory Bank: ROM = 1															
Character Code	"80"H	"81"H	"82"H	"83"H	"84"H	"85"H	"86"H	"87"H	"88"H	"89"H	"8A"H	"8B"H	"8C"H	"8D"H	"8E"H	"8F"H
CGRAM Address (HEX)	100 to 106	107 to 10D	10E to 114	115 to 11B	11C to 122	123 to 129	12A to 130	131 to 137	138 to 13E	13F to 145	146 to 14C	14D to 153	154 to 15A	15B to 161	162 to 168	169 to 16F
Font Bank	Memory Bank: ROM = 1															
Character Code	"90"H	"91"H	"92"H	"93"H	"94"H	"95"H	"96"H	"97"H	"98"H	"99"H	"9A"H	"9B"H	"9C"H	"9D"H	"9E"H	"9F"H
CGRAM Address (HEX)	180 to 186	187 to 18D	18E to 194	195 to 19B	19C to 1A2	1A3 to 1A9	1AA to 1B0	1B1 to 1B7	1B8 to 1BE	1BF to 1C5	1C6 to 1CC	1CD to 1D3	1D4 to 1DA	1DB to 1E1	1E2 to 1E8	1E9 to 1EF

Notes:
1. In the character display mode (SPR = 0 and GR = 0), RM = 1 is set and CGRAM is used. The CGRAM font pattern is displayed using character codes set to the DDRAM as per the above table.
2. In the graphics display mode (SPR = 0 and GR = 1), the CGRAM bit map data is displayed irrespective of the DDRAM set character code.
3. In the superimposed display mode (SPR = 1), the CGRAM bit map data is displayed.
4. When the memory bank switching bit generates ROM = 0, CGRAM fonts for 16 character codes "00"H to "0F"H can be displayed. When ROM = 1, CGRAM fonts for 64 character codes "00"H to "1F"H and "80"H to "9F"H can be displayed.

Table 9 Relationship between CGRAM Address and Character Pattern (CGRAM Data)

Character Code	00H							01H								9FH						
CGRAM Address	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	...	1E9	1EA	1EB	1EC	1ED	1EE	1EF
DB0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	...	0	1	1	1	1	1	1
DB1	0	1	1	0	0	1	1	0	1	1	0	0	1	1	...	0	1	1	0	0	0	0
DB2	0	1	1	0	0	1	1	0	1	1	0	0	1	1	...	0	1	1	0	0	0	0
DB3	0	1	1	0	0	1	1	0	1	1	1	1	0	0	...	0	1	1	1	1	0	0
DB4	0	1	1	1	1	1	1	0	1	1	0	0	1	1	...	0	1	1	0	0	0	0
DB5	0	1	1	0	0	1	1	0	1	1	0	0	1	1	...	0	1	1	0	0	0	0
DB6	0	1	1	0	0	1	1	0	1	1	1	1	1	0	...	0	1	1	0	0	0	0
DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	0	0

Notes: 1. The least significant bit (LSB) of the write data is displayed on the first line. The most significant bit (MSB) is displayed on the 8th raster-row.

2. The 8th raster-row is the cursor position and its display is formed by a logical OR with the cursor.

3. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Table 10 Relationship between Display Position and CGRAM Address in Graphics Display Mode (GR = 1 and SPR = 0) and Superimposed Display Mode (SPR = 1) (CGRAM (1): RM = 1)

Segment Driver		SEG1/112	SEG2/111	SEG3/110	SEG4/109	SEG5/108	SEG6/107	SEG7/106	SEG8/105	SEG9/104	SEG10/103	SEG11/102	SEG12/101	SEG13/100	SEG14/99	SEG15/98	SEG16/97	SEG17/96	...	SEG108/5	SEG109/4	SEG110/3	SEG111/2	SEG112/1	Segment / Common
Address	SGS="0"	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	...	06B	06C	06D	06E	06F	(HEX)
	SGS="1"	06F	06E	06D	06C	06B	06A	069	068	067	066	065	064	063	062	061	060	05F	...	004	003	002	001	000	
	DB0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	...	0	0	1	0	0	COM1
	DB1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	...	0	1	1	0	0	COM2
	DB2	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	...	0	0	1	0	0	COM3
	DB3	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	0	1	0	0	COM4
	DB4	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	1	0	0	COM5
	DB5	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	1	0	0	COM6
	DB6	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	1	1	1	0	COM7
	DB7	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	0	0	0	COM8
Address	SGS="0"	080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F	090	...	0EB	0EC	0ED	0EE	0EF	(HEX)
	SGS="1"	0EF	0EE	0ED	0EC	0EB	0EA	0E9	0E8	0E7	0E6	0E5	0E4	0E3	0E2	0E1	0E0	0DF	...	084	083	082	081	080	
	DB0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	1	1	1	0	COM9
	DB1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	1	0	0	0	1	COM10
	DB2	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	...	0	0	0	0	1	COM11
	DB3	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	...	0	0	0	1	0	COM12
	DB4	0	0	0	0	1		0	0	1	0	0	0	1	0	0	0	0	...	0	0	1	0	0	COM13
	DB5	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	1	0	0	0	COM14
	DB6	0	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	...	1	1	1	1	1	COM15
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	COM16
Address	SGS="0"	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	...	16B	16C	16D	16E	16F	(HEX)
	SGS="1"	16F	16E	16D	16C	16B	16A	169	168	167	166	165	164	163	162	161	160	15F	...	104	103	102	101	100	
	DB0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	...	1	1	1	1	1	COM17
	DB1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	0	0	1	0	COM18
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	0	0	0	0	COM24
Address	SGS="0"	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	180	...	1EB	1EC	1ED	1EE	1EF	(HEX)
	SGS="1"	1EF	1EE	1ED	1EC	1EB	1EA	1E9	1E8	1E7	1E6	1E5	1E4	1E3	1E2	1E1	1E0	1DF	...	184	183	182	181	180	
	DB0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	...	0	0	0	1	0	COM25
	DB1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	...	0	0	1	1	0	COM26
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	COM32
Address	SGS="0"	200	201	202	203	204	205	206	207	208	209	20A	20B	20C	20D	20E	20F	210	...	26B	26C	26D	26E	26F	(HEX)
	SGS="1"	26F	26E	26D	26C	26B	26A	269	268	267	266	265	264	263	262	261	260	25F	...	204	203	202	201	200	
	DB0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	...	0	0	0	1	0	COM33
	DB1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	...	0	0	1	1	0	COM34
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	COM40

Notes: 1. When the RM bit is set to 1, the CGRAM can be selected.

2. In the graphics display mode (SPR = 0 and GR = 1) and the superimposed mode (SPR = 1), the CGRAM bit map data is displayed irrespective of the DDRAM set data.

3. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Table 11 Relationship between Display Position and CGRAM Address in Graphics Display Mode (GR = 1 and SPR = 0) and Superimposed Display Mode (SPR = 1) (CGRAM (2): RM = 1)

Segment Driver		SEG1/112	SEG2/111	SEG3/110	SEG4/109	SEG5/108	SEG6/107	SEG7/106	SEG8/105	SEG9/104	SEG10/103	SEG11/102	SEG12/101	SEG13/100	SEG14/99	SEG15/98	SEG16/97	SEG17/96	...	SEG108/5	SEG109/4	SEG110/3	SEG111/2	SEG112/1	Segment / Common
Address	SGS="0"	280	281	282	283	284	285	286	287	288	289	28A	28B	28C	28D	28E	28F	290	...	2EB	2EC	2ED	2EE	2EF	(HEX)
Address	SGS="1"	2EF	2EE	2ED	2EC	2EB	2EA	2E9	2E8	2E7	2E6	2E5	2E4	2E3	2E2	2E1	2E0	2DF	...	284	283	282	281	280	(HEX)
	DB0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	1		...	1	1	1	1	1	COM41
	DB1	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	...	0	0	0	1	0	COM42
	DB2	1	1	1	1	1	1	1	1	1	0	0	0	1	0	1	0	0	...	0	1	1	0	0	COM43
	DB3	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	0	...	0	0	0	1	0	COM44
	DB4	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	...	0	0	0	0	1	COM45
	DB5	0	1	1	1	1	1	1	1	0	0	1	1	0	0	0	1	1	...	1	0	0	0	1	COM46
	DB6	0	0	1	1	1	1	1	0	0	0	1	1	1	0	1	1	1	...	0	1	1	1	0	COM47
	DB7	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	0	...	0	0	0	0	0	COM48
Address	SGS="0"	300	301	302	303	304	305	306	307	308	309	30A	30B	30C	30D	30E	30F	310	...	36B	36C	36D	36E	36F	(HEX)
Address	SGS="1"	36F	36E	36D	36C	36B	36A	369	368	367	366	365	364	363	362	361	360	35F	...	304	303	302	301	300	(HEX)
	DB0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1		...	1	1	1	1	1	COM49
	DB1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	...	1	0	0	0	0	COM50
	DB2	0	0	1	1	1	1	1	0	0	0	0	0	1	0	1	0	0	...	1	1	1	1	0	COM51
	DB3	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	0	...	0	0	0	0	1	COM52
	DB4	0	0	1	1	1	1	1	0	0	0	1	1	1	0	1	1	1	...	0	0	0	0	1	COM53
	DB5	0	0	0	1	1	1	0	0	0	0	1	1	0	0	0	1	1	...	1	0	0	0	1	COM54
	DB6	0	0	0	0	1	0	0	0	0	0	1	1	1	0	1	1	1	...	0	1	1	1	0	COM55
	DB7	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	...	0	0	0	0	0	COM56
Address	SGS="0"	380	381	382	383	384	385	386	387	388	389	38A	38B	38C	38D	38E	38F	390	...	3EB	3EC	3ED	3EE	3EF	(HEX)
Address	SGS="1"	3EF	3EE	3ED	3EC	3EB	3EA	3E9	3E8	3E7	3E6	3E5	3E4	3E3	3E2	3E1	3E0	3DF	...	384	383	382	381	380	(HEX)
	DB0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1		...	0	0	1	0	0	COM57
	DB1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	...	0	1	1	0	0	COM58
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1	1	0	...	0	0	0	0	0	COM64
Address	SGS="0"	400	401	402	403	404	405	406	407	408	409	40A	40B	40C	40D	40E	40F	410	...	46B	46C	46D	46E	46F	(HEX)
Address	SGS="1"	46F	46E	46D	46C	46B	46A	469	468	467	466	465	464	463	462	461	460	45F	...	404	403	402	401	400	(HEX)
	DB0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	1		...	0	1	1	1	0	COM65
	DB1	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	...	1	0	0	0	1	COM66
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	0	...	0	0	0	0	0	COM72
Address	SGS="0"	480	481	482	483	484	485	486	487	488	489	48A	48B	48C	48D	48E	48F	490	...	4EB	4EC	4ED	4EE	4EF	(HEX)
Address	SGS="1"	4EF	4EE	4ED	4EC	4EB	4EA	4E9	4E8	4E7	4E6	4E5	4E4	4E3	4E2	4E1	4E0	4DF	...	484	483	482	481	480	(HEX)
	DB0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	1		...	0	1	1	1	0	COM73
	DB1	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	...	1	0	0	0	1	COM74
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	0	...	0	0	0	0	0	COM80

Notes: 1. When the RM bit is set to 1, the CGRAM can be selected.

2. In the graphics display mode (SPR = 0 and GR = 1) and the superimposed mode (SPR = 1), the CGRAM bit map data is displayed irrespective of the DDRAM set data.

3. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Modifying Character Patterns

Character Pattern Development Procedure

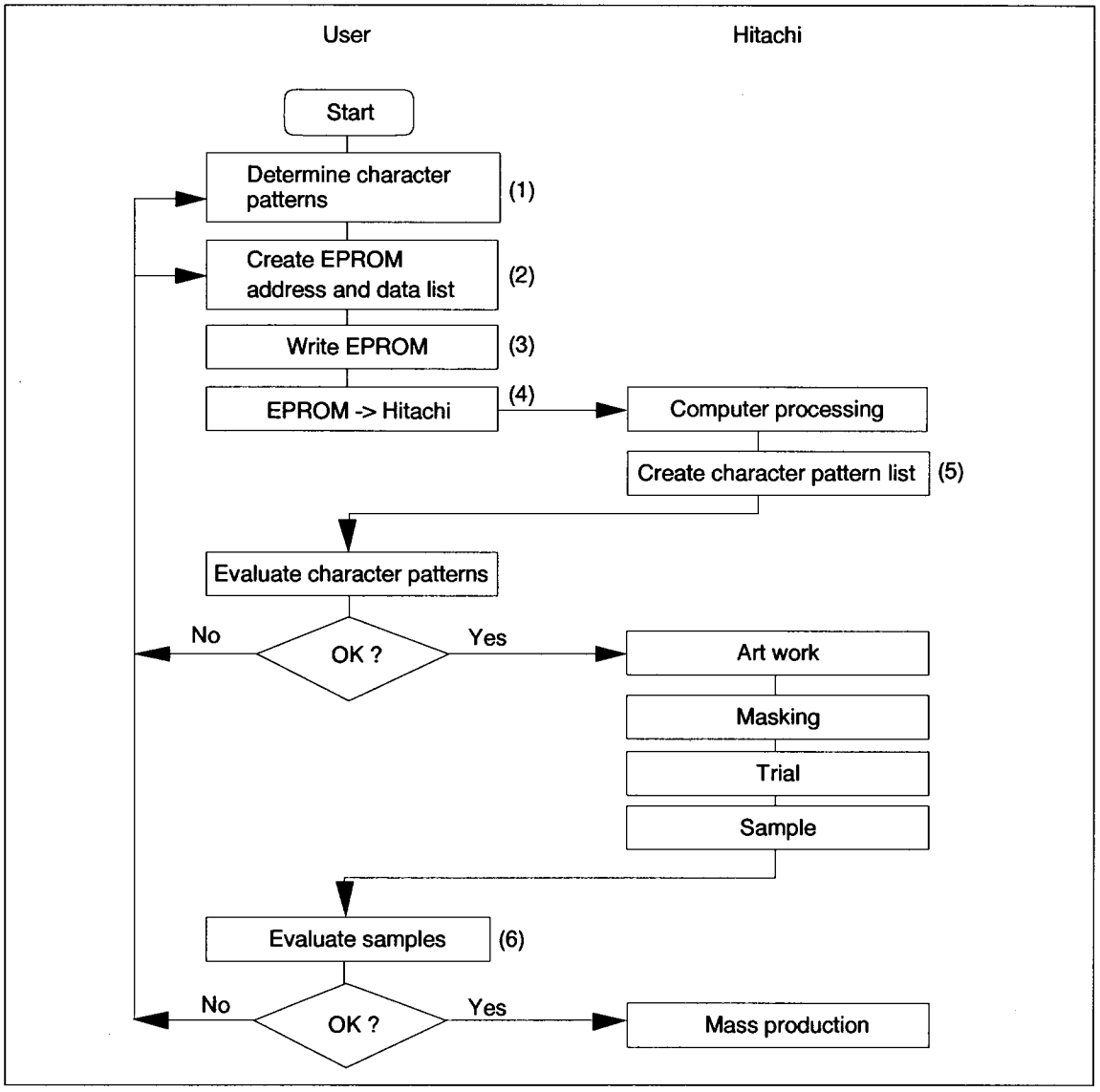


Figure 4 Character Pattern Development Procedure

The following operations correspond to the numbers listed in figure 4:

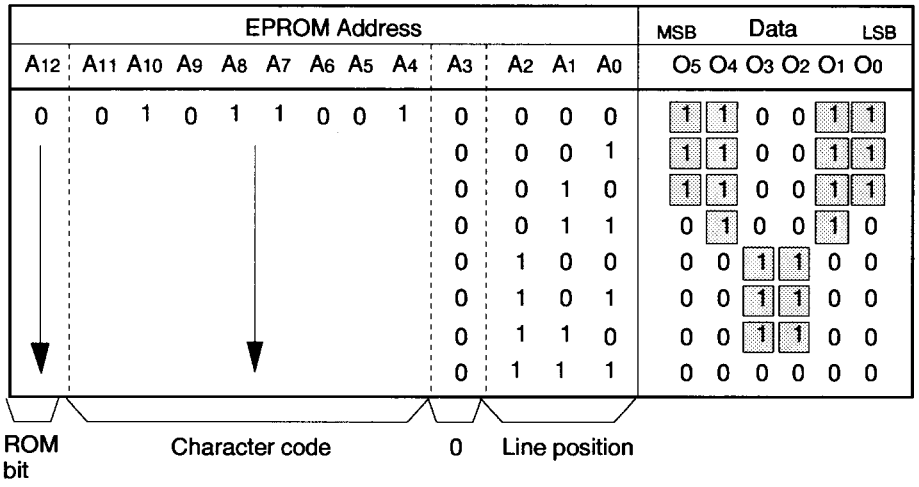
1. Determine the correspondence between character codes and character patterns.
2. Create a list indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing of the EPROM is performed at Hitachi to create a character pattern list, which is sent to the user.
6. If there are no problems within the character pattern list, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When the user confirms that the character patterns are correctly written, Hitachi will start LSI mass production.

Programming Character Patterns

This section explains the correspondence between addresses and data used for program character patterns in EPROM.

Programming to EPROM: The HD66728 character generator ROM can generate 432 6 × 8-dot character patterns. Table 12 shows the correspondence between the EPROM address, data, and the character pattern.

Table 12 Examples of Correspondence between EPROM Address, Data, and Character Pattern (6 × 8 Dots)



Notes:
1. EPROM address: Bit A12 corresponds to the CGROM memory bank switch bit ("ROM").
2. EPROM address: Bits A11 to A4 correspond to a character code.
3. EPROM address: Bits A2 to A0 specify the line position of the character pattern. EPROM address: Bit A3 must be set to 0.
4. EPROM data: Bits O5 to O0 correspond to character pattern data.
5. Areas which are lit (indicated by shading) are stored as 1, and unlit areas as 0.
6. The eighth raster-row is also stored in the CGROM, and must also be programmed. If the eighth raster-row is used for a cursor, this data must all be set to zero.
7. EPROM data: Bits O7 to O6 are invalid. 0 must be written in all bits.

Handling Unused Character Patterns:

1. EPROM data outside the character pattern area: This is ignored by character generator ROM for display operation so any data is acceptable.
2. EPROM data in CGRAM area: Always fill with zeros.
3. Treatment of unused user patterns in the HD66728 EPROM: Depending on to the user application, these are handled in either of two ways:
   a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.
   b. When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66728 can be controlled by the MPU. Before starting internal operation of the HD66728, control information is temporarily stored in these registers to allow interfacing with various peripheral control devices or MPUs which operate at different speeds. The internal operation of the HD66728 is determined by signals sent from the MPU. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signal (DB0 to DB7), make up the HD66728 instructions. There are five categories of instructions that:

- Control the display
- Control power management
- Set internal RAM addresses
- Transfer data with the internal RAM
- Control key scan (when serial interface mode)

Normally, instructions that perform data transfer with the internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66728 RAM addresses after each data write can lighten the MPU program load.

Because instructions other than clear display instruction are executed in 0 cycle, instructions can be written in succession.

While the clear display instruction is being executed for internal operation, or during reset, no instruction other than the key scan read instruction can be executed.

Instruction Descriptions

Key Scan Data Read

In the serial interface mode, the key scan data read instruction reads scan data in scan registers SCAN0 to SCAN3. Following transfer of the start byte, scan data read operation starts from scan register SCAN0 and proceeds in the order of SCAN1, SCAN2, and SCAN3. When data read from SCAN 0 to SCAN3 is complete, the operation starts from SCAN0 again. For details, see the Key Scan Control section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	**SD7**	**SD6**	**SD5**	**SD4**	**SD3**	**SD2**	**SD1**	**SD0**

Figure 5 Key Scan Data Read Instruction

Blink Synchronization

The blink synchronization instruction initializes the blink counter which controls the cursor blink cycle. After initialization, the counter starts from display lighting. When this instruction is issued in each second, the blink cycle becomes one second without depending on the LCD frame frequency.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Figure 6 Blink Synchronization Instruction

Clear Display

The clear display instruction writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter (AC). It also sets I/D to 1 (increment mode) in the entry mode set instruction. Since the execution time of this instruction is 167 clock cycles, do not transfer the next instruction during this time.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Figure 7 Clear Display Instruction

Return Home

The return home instruction sets DDRAM address 0 into the address counter. The DDRAM contents do not change. The cursor or blinking goes to the top left of the display.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0

Figure 8 Return Home Instruction

Start Oscillation

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	1

Figure 9 Start Oscillation Instruction

Driver Output Control

CMS: Selects the output shift direction of a common driver. When CMS = "0", COM1/80 shifts to COM1, and COM80/1 to COM80. When CMS = "1", COM1/80 shifts to COM80, and COM80/1 to COM1. Output position of a common driver shifts depending on the CN1–0 bit setting. For details, see the Display On/Off Control section.

SGS: Selects the output shift direction of a segment driver. When SGS = "0", SEG1/112 shifts to SEG1, and SEG112/1 to SEG112. When SGS = "1", SEG1/112 shifts SEG112, and SEG112/1 to SEG1.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	CMS	SGS

Figure 10 Driver Output Control Instruction

Power Control

AMP: When AMP = 1, each voltage follower for V1 to V5 pins and the booster are turned on. When AMP = 0, current consumption can be reduced while the display is not being used.

SLP: When SLP = 1, the HD66728 enters the sleep mode, where the internal operations are halted except for the key scan function and the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

a. Key scan data read
b. Key scan control (IRE, KF1/0, KSB bits)
c. Power control (AMP, SLP, and STB bits)
d. Port control (PT2-0 bits)

During the sleep mode, the other RAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66728 enters the standby mode, where display operation and key scan completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. This setting can be used as the system wake-up, because an interrupt is generated when a specific key is pressed. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Voltage follower circuit on/off (AMP = 1/0)
c. Start oscillation
d. Key scan interrupt generation enabled/disabled (IRE = 1/0)
e. Port control (PT2-0 bits)

During the standby mode, the other RAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	AMP	SLP	STB

Figure 11 Power Control Instruction

Contrast Control 1/2

SW: Switches the bit configuration for the contrast control instruction.

CT4–CT0: When SW = 0, they control the LCD drive voltage (potential difference between V1 and GND) to adjust contrast. A 64-step adjustment is also possible by using the CT5 bit which are set in the entry mode register. For details, see the Contrast Adjuster section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	0	SW	CT4	CT3	(SW = 0)
								BT1	BT0	(SW = 1)
0	0	0	0	0	1	1	CT2	CT1	CT0	(SW = 0)
							BS2	BS1	BS0	(SW = 1)

Figure 12 Contrast-Control 1/2 Instruction

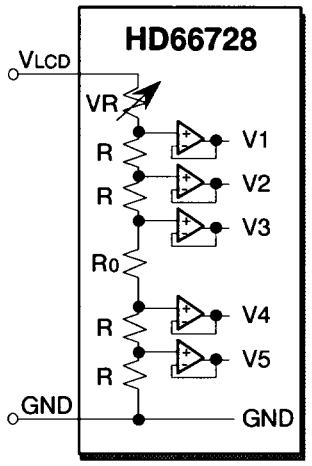


Figure 13 Contrast Adjuster

Table 13 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value						
CT5	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**	**Variable Resistor (VR)**
0	0	0	0	0	0	3.20 x R
0	0	0	0	0	1	3.15 x R
0	0	0	0	1	0	3.10 x R
0	0	0	0	1	1	3.05 x R
0	0	0	1	0	0	3.00 x R
			•			•
			•			•
0	1	1	1	1	1	1.65 x R
1	0	0	0	0	0	1.60 x R
1	0	0	0	0	1	1.55 x R
1	0	0	0	1	0	1.50 x R
			•			•
			•			•
1	1	1	1	0	1	0.15 x R
1	1	1	1	1	0	0.10 x R
1	1	1	1	1	1	0.05 x R

BT1-0: When SW = 1, they switch the output of V5OUT between triple, quadruple, and five-times boost. The liquid crystal display drive voltage level can be selected according to its drive duty ratio and bias. A lower amplification of the booster consumes less current.

BS2-0: When SW = 1, they set the crystal display drive bias value within the range of 1/4 to 1/10 bias. The liquid crystal display drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector section.

Table 14 BT Bits and Output Level

BT1	BT0	V5OUT Output Level
0	0	Triple boost (no boost)
0	1	Quadruple boost
1	0	Five-times boost
1	1	Setting inhibited

Table 15 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	Liquid Crystal Display Drive Bias Value
0	0	0	1/10 bias drive
0	0	1	1/9.5 bias drive
0	1	0	1/9 bias drive
0	1	1	1/8 bias drive
1	0	0	1/7 bias drive
1	0	1	1/6 bias drive
1	1	0	1/5 bias drive
1	1	1	1/4 bias drive

Entry Mode

REV: Displays all character and graphics display sections with black-and-white reversal when SW = 0 and REV = 1. For details, see the Reversed Display Function section.

I/D: When SW = 0, increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from the DDRAM. The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to the writing and reading of CGRAM.

GR: Sets the GR bit when SW = 0. Activates the character display mode when GR = 0 and SPR = 0. Displays the font pattern on the CGROM or CGRAM according to the character code written in the DDRAM. Activates the graphics display mode when GR = 1 and SPR = 0. Displays a given pattern according to the bit map data written in the CGRAM. In this case, the data in the DDRAM is not used for display. For details, see the Graphics Display Function section.

CT5: Sets the most significant bit (CT5) for contrast adjustment when SW = 1. A 64-step adjustment is also possible by using the CT4–CT0 bits which are set in the contrast-control 1/2 instruction.

RDM: When SW = 1 and RDM = 0, the RDM increments or decrements the address counter value according to the I/D bit setting after reading the data from the DDRAM or CGRAM. When RDM = 1, the address counter value is not updated after the data has been read from the DDRAM or CGRAM. The address counter value is used when the RAM data is read, modified, and written. Since the first read data is invalid, the read must be continuously done twice. After writing to the RAM, the address counter value must be updated.

SPR: When SW = 1 and SPR = 1, the SPR displays combined character and graphics display screens (the superimposed display mode). When SPR = 1, the GR bit setting is invalid. In this case, user fonts using the CGRAM in the character display mode cannot be displayed. For details, see the Superimposed Display Function section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	0	0	REV	I/D	GR	(SW = 0)
							CT5	RDM	SPR	(SW = 1)

Figure 14 Entry Mode Set Instruction

Cursor Control

B/W: When B/W = 1 and LC = 1, the character at the cursor position is cyclically (every 32 frames) blink-displayed with black-and-white reversal.

When B/W = 1 and LC = 1, all characters including the cursor on the display line appear with black-and-white reversal. The characters do not blink. For details, see the Line-cursor Display section.

C: The cursor is displayed on the 8th raster-row when C = 1. The 7-dot cursor is ORed with the character pattern and displayed on the 8th raster-row.

B: The character indicated by the cursor blinks when B = 1. The blinking is displayed as switching between all black dots and displayed characters every 32 frames. The cursor and blinking can be set to display simultaneously. When LC =1, setting B = 1 alternately displays all white dots and character pattern in a line unit.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	B/W	C	B

Figure 15 Cursor Control Instruction

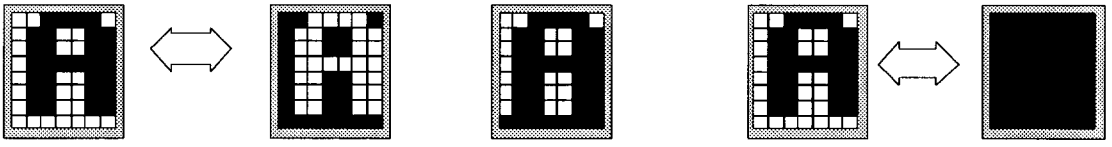


Figure 16 Cursor Blink Width Control

Display On/Off Control

D: Display is on when SW = 0 and D = 1 and off when D = 0. When off, the display data remains in the DDRAM or CGRAM, and can be displayed instantly by setting D = 1. When D is 0, the display is off with the SEG1 to SEG112 outputs and COM1 to COM80 outputs set to the GND level. Because of this, the HD66728 can control charging current for the LCD with AC driving.

LC: When SW = 0 and LC = 1, a cursor attribute is assigned to the line that contains the address counter (AC) value. Cursor mode can be selected in the black-and-white reversed display, underline display, and blink display with the B/W, C, and B bits. For details, see the Line-cursor Display section.

DL10: When SW = 0, DL10 can be set. When DL10 = 1, the 10th line is displayed at double height.

DL9–DL7: When SW = 1, DL9–DL7 can be set. Double-height display is specified for any display line. When DL7 = 1, the seventh line is displayed at double height. Double-height display is used for the eighth line when DL8 = 1 and for the ninth line when DL9 = 1. For double-height display for the first to the sixth lines, control them by using DL1–DL6 bits in the display-line control instruction.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	1	0	D	DL10	LC	(SW = 0)
							DL9	DL8	DL7	(SW = 1)

Figure 17 Display On/Off Control Instruction

Display Line Control

NL3-0: Set NL2–NL0 bits when SW = 0, and the NL3 bit when SW = 1 to specify the display lines. Display lines change the liquid crystal display drive duty ratio. DDRAM or CGRAM address mapping does not depend on the number of display lines.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
	0	0	0	0	1	1	1	NL2	NL1	NL0	(SW = 0)
								CN1	CN0	NL3	(SW = 1)

Figure 18 Display-line Control Instruction

Table 16 NL Bits and Display Lines

NL3	NL2	NL1	NL0	Character Display	Graphics Display	LCD Drive Duty	Common Driver Used
0	0	0	0	16 character x 1 line	112 x 8 dots	1/8 Duty	COM1–COM8
0	0	0	1	16 character x 2 lines	112 x 16 dots	1/16 Duty	COM1–COM16
0	0	1	0	16 character x 3 lines	112 x 24 dots	1/24 Duty	COM1–COM24
0	0	1	1	16 character x 4 lines	112 x 32 dots	1/32 Duty	COM1–COM32
0	1	0	0	16 character x 5 lines	112 x 40 dots	1/40 Duty	COM1–COM40
0	1	0	1	16 character x 6 lines	112 x 48 dots	1/48 Duty	COM1–COM48
0	1	1	0	16 character x 7 lines	112 x 56 dots	1/56 Duty	COM1–COM56
0	1	1	1	16 character x 8 lines	112 x 64 dots	1/64 Duty	COM1–COM64
1	0	0	0	16 character x 9 lines	112 x 72 dots	1/72 Duty	COM1–COM72
1	0	0	1	16 character x 10 lines	112 x 80 dots	1/80 Duty	COM1–COM80

CN1–CN0: Set CN1–CN0 bits when SW = 1. When CN1–0 = 01, the display position is shifted by 16 dots (two lines) below and display starts from COM17. When the liquid crystal is driven at low duty in the system wait state, it can display partially at the center of the screen. For details, see the Partial-display-on Function section.

When CN1–CN0 = 10, the display position is shifted by 8 dots (one line) above and second-line display starts from COM1. The 8 dots of the first line are moved to the lowest edge of the display screen. The output position of the lowest edge depends on the drive duty setting. In vertical smooth scrolling, PS1–PS0 bits can selectively fixed-display only the first to the third lines. Combining these functions enables the fixed display of one line of the lowest edge. For details, see the Partial Smooth Scroll Display Function section.

Table 17 Common Driver Pin Function

Common Driver Pin	Common Driver Pin Function					
	CN 1–0 = 00 (Normal Output)		CN 1–0 = 01 (Center Output)		CN1–0 = 10 (Lowest-edge Output)	
	CMS = 0	CMS = 1	CMS = 0	CMS = 1	CMS = 0	CMS = 1
COM1/80	**COM1**	COM80	COM65	COM64	COM9	COM8
COM2/79	COM2	COM79	COM66	COM63	COM10	COM7
:	:	:	:	:	:	:
COM7/72	COM7	COM74	COM71	COM58	COM15	COM2
COM8/73	COM8	COM73	COM72	COM57	COM16	**COM1**
COM9/72	COM9	COM72	COM73	COM56	COM17	COM80
COM10/71	COM10	COM71	COM74	COM55	COM18	COM79
:	:	:	:	:	:	:
COM15/66	COM15	COM66	COM79	COM50	COM23	COM73
COM16/65	COM16	COM65	COM80	COM49	COM24	COM72
COM17/64	COM17	COM64	**COM1**	COM48	COM25	COM71
COM18/63	COM18	COM63	COM2	COM47	COM26	:
:	:	:	:	:	:	COM66
COM24/57	COM24	COM57	COM8	COM41	COM32	COM65
COM25/56	COM25	COM56	COM9	COM40	COM33	COM64
:	:	:	:	:	:	:
COM32/49	COM32	COM49	COM16	COM33	COM40	COM57
COM33/48	COM33	COM48	COM17	COM32	COM41	COM56
:	:	:	:	:	:	:
COM40/41	COM40	COM41	COM24	COM25	COM48	COM49
COM41/40	COM41	COM40	COM25	COM24	COM49	COM48
:	:	:	:	:	:	:
COM48/33	COM48	COM33	COM32	COM17	COM56	COM41
COM49/32	COM49	COM32	COM33	COM16	COM57	COM40
:	:	:	:	:	:	:
COM56/25	COM56	COM25	COM40	COM9	COM64	COM33
COM57/24	COM57	COM24	COM41	COM8	COM65	COM32
:	:	:	:	:	:	:
COM64/17	COM64	COM17	COM48	**COM1**	COM72	COM25
COM65/16	COM65	COM16	COM49	COM80	COM73	COM24
:	:	:	:	:	:	:
COM72/9	COM72	COM9	COM56	COM73	COM80	COM17
COM73/8	COM73	COM8	COM57	COM72	**COM1**	COM16
:	:	:	:	:	COM2	COM15
COM79/2	COM79	COM2	COM63	COM66	:	:
COM80/1	COM80	**COM1**	COM64	COM65	COM8	COM9

Double-height Display Control

DL3-1: Can be specified when SW = 0. Specify the double-height display for any line. When DL1 = 1, the first line is displayed at double height. When DL2 = 1, the second line is displayed at double height. When DL3 = 1, the third line is displayed at double height. Double-height display of multiple lines is possible. For details, see the Double-height Display section.

DL6-4: Can be specified when SW = 1. Specify the double-height display for any line. When DL4 = 1, the fourth line is displayed at double height. When DL5 = 1, the fifth line is displayed at double height. When DL6 = 1, the sixth line is displayed at double height. For the seventh to 10th lines, control double-height display by using the DL7–DL10 bits in the display-line control instruction. For details, see the Double-height Display section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	DL3 DL6	DL2 DL5	DL1 DL4

Figure 19 Double-height Display Control Instruction

Vertical Scroll Control 1/2

SN3-0: Set SN2 to SN0 bits when SW = 0. Set the SN3 bit when SW = 1. Specify the display start line output from COM1. Because the DDRAM is assigned a 10-line display area, the data is displayed sequentially from the first line to the 10th line then repeated from the first line again. In partial smooth scrolling, these bits specify the display start line for the next line of the fixed-display line. For details, see the Partial Smooth Scroll Display Function section.

SL2–0: Select the top raster-row to be displayed (display-start raster-row) in the display-start line specified by SN2 to SN0. Any raster-row from the first to eighth can be selected (table 19). This function is used to achieve vertical smooth scrolling together with SN2 to SN0. For details, see the Vertical Smooth Scroll section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	0	0	1	SN2	SN1	SN0	(SW = 0)
							<0>	<0>	SN3	(SW = 1)
0	0	0	1	0	1	0	SL2	SL1	SL0	(SW = 0)
							<0>	PS1	PS0	(SW = 1)

Figure 20 Vertical Scroll Control 1/2 Instruction

Table 18 SN Bits and Display-start Lines

SN3	SN2	SN1	SN0	Display-start Line
0	0	0	0	1st line
0	0	0	1	2nd line
0	0	1	0	3rd line
0	0	1	1	4th line
0	1	0	0	5th line
0	1	0	1	6th line
0	1	1	0	7th line
0	1	1	1	8th line
1	0	0	0	9th line
1	0	0	1	10th line

Table 19 SL Bits and Display-start Raster-row

SL2	SL1	SL0	Display-start Raster-row
0	0	0	1st raster-row
0	0	1	2nd raster-row
0	1	0	3rd raster-row
0	1	1	4th raster-row
1	0	0	5th raster-row
1	0	1	6th raster-row
1	1	0	7th raster-row
1	1	1	8th raster-row

PS1–0: Specify PS1 to PS0 bits when SW = 1. When PS1–0 = 01, only the first line is fixed-displayed in vertical smooth scrolling, and the other display lines are smooth-scrolled. When PS1–0 = 10, the first and second lines are fixed-displayed. When PS1–0 = 11, the first to third lines are fixed-displayed. For details, see the Partial Smooth Scroll Display Function section.

CGROM Bank Control 1/2

RL6–1: Set RL1 to RL6 bits when SW = 0. Switch the CGROM memory bank for any line. Bank 0 and bank 1 of the CGROM incorporate 240 and 192 fonts, respectively, and can display 432 fonts in total. Bits RL1–RL6 select CGROM bank 0/1 for each display line unit. When RL1 = 0, the first line selects bank 0. When RL1 = 1, the first line selects bank 1. Bits RL2, RL3, RL4, and RL6 select the memory banks in the second to sixth lines. For details, see the CGROM Bank Switching Function section.

RL10–7: Set the RL7 to RL10 bits when SW = 1. The RL7 to RL10 bits are set when SW = 1. And the DL7 to DL10 bits switch the CGROM memory bank in the seventh to 10th lines.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	0	1	1	RL3	RL2	RL1	(SW = 0)
							RL9	RL8	RL7	(SW = 1)
0	0	0	1	1	0	0	RL6	RL5	RL4	(SW = 0)
							<0>	<0>	RL10	(SW = 1)

Figure 21 CGROM Bank Control 1/2 Instruction

Key Scan Control

IRE: When SW = 0 and IRE = 1, it permits interrupts when a key is pressed. This causes interrupts to occur in the standby period when the oscillator clock is halted, as well as key scan interrupts during normal operation, allowing system wake-up.

KF1-0: Set the key scan cycle when SW = 0. The following table shows the key scan pulse width and key scan cycle used when the oscillation frequency (fosc) is 80 kHz, which depend on the oscillation frequency. For details, see the Key Scan Control section.

KSB: When SW = 1 and KSB = 1, the KSB enters the key standby mode to stop key scanning. In this case, as well as in the standby mode, key scan interrupts can be generated. When KSB = 0, keys are scanned normally.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	1	0	1	IRE	KF1	KF0	(SW = 0)
							KSB	<0>	<0>	(SW = 1)

Figure 22 Key Scan Control Instruction

Table 20 KF Bits and Key Scan Cycle

KF1	KF0	Key Scan Pulse Width	Key Scan Cycle
0	0	0.2 ms (16 clocks)	0.8 ms (64 clocks)
0	1	0.4 ms (32 clocks)	1.6 ms (128 clocks)
1	0	0.8 ms (64 clocks)	3.2 ms (256 clock cycles)
1	1	1.6 ms (128 clocks)	6.4 ms (512 clock cycles)

Note: The data is a value obtained when the oscillation frequency (fosc) is 80 kHz. The value depends on the oscillation frequency.

Port Control

PT2-0: Control the output level of a port output pin (PORT2-PORT0). When PT0 = 0, the PORT0 pin outputs the GND level, and when PT0 = 1, it outputs the VCC level. Similarly, PT1 and PT2 bits control PORT1 and PORT2 output levels respectively.

B/C: When SW = 1 and B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD driving. When B/C = 1, a C-pattern waveform is generated and alternates (n-raster-row reversed AC drive) in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

DCC: When SW = 1 and DCC = 0, a booster operates with the 64-divided clock of the operating frequency. When DCC = 1, the booster operates with the 32-divided clock. When the booster operates with the 64-divided clock, current consumption in the booster is low, but boosting ability is weak.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	1	1	0	PT2	PT1	PT0	(SW = 0)
							<0>	DCC	B/C	(SW = 1)

Figure 23 Port Control Instruction

LCD-Driving-Waveform Control

EOR: When the C-pattern waveform is set (B/C = 1) and SW = 1 and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate in every set value + 1 raster-row, and the first to the 32nd raster-rows can be selected. When SW = 0, bits NW2, NW1, and NW0 can be set. When SW = 1, bits NW4 and NW3 can be set.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	1	1	1	NW2	NW1	NW0	(SW = 0)
							EOR	NW4	NW3	(SW = 1)

Figure 24 LCD-Driving-Waveform Control Instruction

RAM Address Set

RM: Selects DDRAM or CGRAM. When RM = 0, the DDRAM is selected. When RM = 1, the CGRAM is selected. The selected RAM is accessed with this setting.

AD10-0: Initially set RAM addresses to the address counter (AC). Once the RAM data is written, the AC is automatically updated according to the I/D bit. This allows consecutive accesses without resetting addresses. Once the RAM data is read, the AC is automatically updated according to the I/D bit when RDM = 0, and not updated when RDM = 1. Set RDM to 1 when read, modify, and write are done in every one-byte data. RAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	RM	AD10	AD9	AD8	AD7	AD6
0	0	1	1	AD5	AD4	AD3	AD2	AD1	AD0

Figure 25 RAM Address Set Instruction

Table 21 AD Bits and DDRAM Setting

RM	AD10–AD0	DDRAM Setting
0	"000"H–"00F"H	Character code on the 1st line
0	"010"H–"01F"H	Character code on the 2nd line
0	"020"H–"02F"H	Character code on the 3rd line
0	"030"H–"03F"H	Character code on the 4th line
0	"040"H–"04F"H	Character code on the 5th line
0	"050"H–"05F"H	Character code on the 6th line
0	"060"H–"06F"H	Character code on the 7th line
0	"070"H–"07F"H	Character code on the 8th line
0	"080"H–"08F"H	Character code on the 9th line
0	"090"H–"09F"H	Character code on the 10th line

Table 22 AD Bits and CGRAM Setting

RM	AD9–AD0	CGRAM Setting in the Character Mode
1	"000"H–"06F"H	Font pattern of CGRAM characters (1) to (16)
1	"080"H–"0EF"H	Font pattern of CGRAM characters (17) to (32)
1	"100"H–"16F"H	Font pattern of CGRAM characters (33) to (48)
1	"180"H–"1EF"H	Font pattern of CGRAM characters (49) to (64)

Table 23 AD Bits and CGRAM Settings

RM	AD10–AD0	CGRAM Setting in the Graphics Mode and Superimposed Display Mode
1	"000"H–"06F"H	Bit map data for COM1 to COM8
1	"080"H–"0EF"H	Bit map data for COM9 to COM16
1	"100"H–"16F"H	Bit map data for COM17 to COM24
1	"180"H–"1EF"H	Bit map data for COM25 to COM32
1	"200"H–"26F"H	Bit map data for COM33 to COM40
1	"280"H–"2EF"H	Bit map data for COM41 to COM48
1	"300"H–"36F"H	Bit map data for COM49 to COM56
1	"380"H–"3EF"H	Bit map data for COM57 to COM64
1	"400"H–"46F"H	Bit map data for COM65 to COM72
1	"480"H–"4EF"H	Bit map data for COM73 to COM80

Write Data to RAM

WD7-0 : Write 8-bit data to the DDRAM and CGRAM. The DDRAM or CGRAM is selected by the previous specification of the RM bit. After a write, the address is automatically incremented or decremented by 1 according to the I/D bit setting. During the sleep and standby modes, the DDRAM or CGRAM cannot be accessed.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	**WD7**	**WD6**	**WD5**	**WD4**	**WD3**	**WD2**	**WD1**	**WD0**

Figure 26 Write Data to RAM Instruction

Read Data from RAM

RD7-0 : Read 8-bit data from the DDRAM or CGRAM. The DDRAM or CGRAM is selected by the previous specification of the RM 1/0 bit. In the parallel bus interface mode, the first-byte data read will be invalid immediately after the RAM address set, and the consecutive second-byte data will be read normally. In the serial interface mode, two bytes will be invalid immediately after the start byte, and the consecutive third-byte data will be read normally. For details, see the Serial Data Transfer section.

After a RAM read, when RDM = 0, the address is automatically incremented or decremented by 1 according to the I/D bit. When RDM = 1, the address is not updated.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Figure 27 Read Data from RAM Instruction

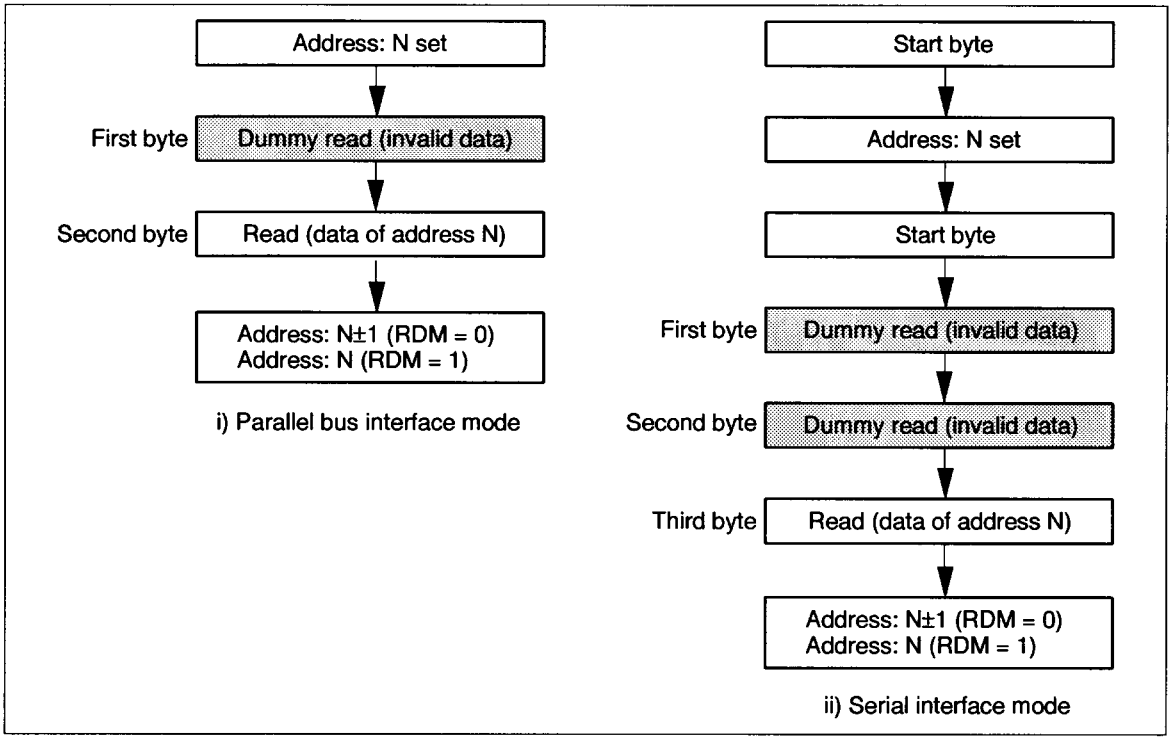


Figure 28 RAM Read Sequence

Table 24 Instruction List

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
Key scan data read	1	0				KSD					Reads key scan data (KSD) (only in the serial interface mode).	0
Blink synchronization	0	0	0	0	0	0	0	0	0	0	Synchronizes the blink counter.	0
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets address 0 into the address counter (AC).	166*1
Return home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 into the address counter.	0
Start oscillation	0	0	0	0	0	0	0	0	1	1	Starts the oscillation standby mode.	—
Driver output control	0	0	0	0	0	0	0	1	CMS	SGS	Selects the common driver shift direction (CMS) and segment driver shift direction (SGS).	0
Power control	0	0	0	0	0	0	1	AMP	SLP	STB	Turns on LCD power supply (AMP), and sets the sleep mode (SLP) and standby mode (STB).	0
Contrast control 1	0	0	0	0	0	1	0	SW	CT4	CT3	Sets the register selection (SW) or upper contrast adjustment bits (CT4-3).	0
									BT1	BT0	Sets the register selection (SW) or boost level (BT1/0).	0
Contrast control 2	0	0	0	0	0	1	1	CT2	CT1	CT0	Sets the lower contrast adjustment bits (CT2-0).	0
								BS2	BS1	BS0	Sets the LCD bias value (BS2-0).	0
Entry mode set	0	0	0	0	1	0	0	REV	I/D	GR	Sets the black-and-white reversal (REV), address update direction after RAM access (I/D), and graphics mode (GR).	0
								CT5	RDM	SPR	Sets the higher contrast adjustment bit (CT5), read, modify, write (RDM), or superimposed display (SPR).	0
Cursor control	0	0	0	0	1	0	1	B/W	C	B	Sets black-and-white reversed cursor (B/W), 8th raster-row cursor (C), and blink cursor (B).	0

Table 24 Instruction List (cont)

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
Display on/off control	0	0	0	0	1	1	0	D	DL10	LC	Sets display on (D), double-height display line (DL10), or line cursor display (LC).	0
								DL9	DL8	DL7	Specifies double-height display lines (DL9–DL7).	0
Display line control	0	0	0	0	1	1	1	NL2	NL1	NL0	Sets the number of display lines (NL2-0).	0
								CN1	CN0	NL3	Specifies centering (CN1–0) or the number of display lines (NL3).	0
Double-height display control	0	0	0	1	0	0	0	DL3	DL2	DL1	Specifies double-height display lines (DL3-1).	0
								DL6	DL5	DL4	Specifies double-height display lines (DL6–4).	0
Vertical scroll control 1	0	0	0	1	0	0	1	SN2	SN1	SN0	Sets the display-start line (SN2-0).	0
								<0>	<0>	SN3	Sets the display-start line (SN3).	0
Vertical scroll control 2	0	0	0	1	0	1	0	SL2	SL1	SL0	Sets the display-start raster-row (SL2-0).	0
								<0>	PS1	PS0	Sets the partial scroll (PS1–0).	0
CGROM bank control 1	0	0	0	1	0	1	1	RL3	RL2	RL1	Selects the CGROM memory bank in the first to third lines.	0
								RL9	RL8	RL7	Selects the CGROM memory bank in the seventh to ninth lines.	0
CGROM bank control 2	0	0	0	1	1	0	0	RL6	RL5	RL4	Selects the CGROM memory bank in the fourth to sixth lines.	0
								<0>	<0>	RL10	Selects the CGROM memory bank in the 10th line.	0
Key scan control	0	0	0	1	1	0	1	IRE	KF1	KF0	Sets the key scan interrupt (IRE) and key scan cycle (KF1/0).	0
								KSB	<0>	<0>	Sets the key standby mode (KSB).	0
Port control	0	0	0	1	1	1	0	PT2	PT1	PT0	Sets the general port output (PT2-0).	0
								<0>	DCC	BC	Selects the boosting cycle (DCC) or LCD drive AC waveform (B/C).	0

Table 24 Instruction List (cont)

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
LCD-driving-waveform control	0	0	0	1	1	1	1	NW2	NW1	NW0	Sets the number of n-raster-rows (NW2–0) in C-pattern AC drive.	0
								EOR	NW4	NW3	Sets the EOR output (EOR) or the number of n-raster-rows (NW4–3) in C-pattern AC drive.	0
RAM address set (upper bits)	0	0	1	0	RM			AD10–6 (upper bits)			Selects RAM (RM), or initially sets the upper addresses of the RAM to the address counter (AC).	0
RAM address set (lower bits)	0	0	1	1				AD5-0 (lower bits)			Initially sets the lower addresses of the RAM to the AC.	0
Write data to RAM	0	1				Write data					Writes data to DDRAM or CGRAM.	0
Read data from RAM	1	1				Read data					Reads data from DDRAM or CGRAM.	0

Notes: 1. Represented by the number of operating clock pulses; the execution time depends on the supplied clock frequency or the internal oscillation frequency.
2. The upper column of each register can be set when SW = 0. The lower column can be set when SW = 1.

Bit definition:

CMS = 0: COM1/80 => COM1

SGS = 0: SEG1/112 => SEG1

AMP = 1: Operational amplifier and booster circuit on

SLP = 1: Sleep mode

STB = 1: Standby mode

SW = 0: Upper register setting

SW = 1: Lower register setting

CT5-0: Contrast adjustment

BT1/0: Boost level selection (00: Triple, 01: Quadruple, 10: Five-times)

BS2-0: LCD drive bias selection

REV = 0: Normal display

REV = 1: Black-and-white reversed display of the character and graphics display

ID = 1: Address increment

ID = 0: Address decrement

GR = 1: Graphics display mode

GR = 0: Character display mode

RDM = 1: Read, modify, and write mode (Not automatically update the address counter after reading)

SPR = 1: Superimposed display of the character and graphics

B/W = 1: Black-and-white reversed cursor on

C = 1: 8th raster-row cursor on

B = 1: Blink cursor on

D = 1: Display on

LC = 1: Cursor display for the all display lines including AC

NL3-0: Display line setting (0000: 1/8 duty ratio, 0001: 1/16 duty ratio, 0010: 1/24 duty ratio, 0011: 1/32 duty ratio, 0100: 1/40 duty ratio, 0101: 1/48 duty ratio, 0110: 1/56 duty ratio, 0111: 1/64 duty ratio, 1000: 1/72 duty ratio, 1001: 1/80 duty ratio)

DL1-10: Double-height line specifications (DL1: 1st line, DL2: 2nd line, DL3: 3rd line, DL4: 4th line, DL5: 5th line, DL6: 6th line, DL7: 7th line, DL8: 8th line, DL9: 9th line, DL10: 10th line)

SN3-0: Display-start line (0000: 1st line, 0001: 2nd line, 0010: 3rd line, 0011: 4th line, 0100: 5th line, 0101: 6th line, 0110: 7th line, 0111: 8th line, 1000: 9th line, 1001: 10th line)

SL2-0: Display-start raster-row specifications (000: 1st raster-row...111: 8th raster-row)

CN1–0 Centering specifications (00: no centering, 01: 16-dot shift below, 10: 8-dot shift above)

RL1–10: CGROM memory bank switching selection (0: bank 0, 1: bank 1, RL1: 1st line, RL2: 2nd line, RL3: 3rd line, RL4: 4th line, RL5: 5th line, RL6: 6th line, RL7: 7th line, RL8: 8th line, RL9: 9th line, RL10: 10th line)

IRE = 1: Key scan interrupt generation enabled

KF1/0: Key scan cycle set

KSB = 1: Key scan standby mode

PT2-0: Port output control (PT2 = 1: PORT2 = Vcc, PT1 = 1: PORT1 = Vcc, PT0 = 1: PORT0 = Vcc)

B/C = 0: B-pattern waveform drive

B/C = 1: C-pattern waveform drive

EOR = 1: EOR alternating drive at C-pattern waveform

NW4–0: Reversed number of n raster-rows at C-pattern waveform drive (alternating with the set value + one raster-row)

DCC = 0: Boosted at 1/64-divided clock

DCC = 1: Boosted at 1/32-divided clock

RM: RAM selection (0: DDRAM, 1: CGRAM)
ADD10-0: DDRAM/CGRAM address set (DDRAM: 000H-09FH, CGRAM: 000H-4EFH)

Reset Function

The HD66728 is internally initialized by RESET input. During initialization, the system executes a clear display instruction after reset is canceled. The system executes the other instructions during the reset period. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period and the clear display instruction is executed following reset cancellation, no instruction or RAM data access from the MPU is accepted. The reset input must be held for at least 1 ms. Any initializing instruction must wait for 1,000 clock cycles after the reset is canceled so that execution of the clear display instruction can be completed.

Instruction Set Initialization:

1. Clear display executed (Writes 20H to DDRAM)
2. Return home executed (Sets the address counter (AC) to 00H to select DDRAM)
3. Start oscillation executed
4. Driver output control (SGS = 0, CMS = 0)
5. Power control (AMP = 0: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
6. Single boost (BT1/0 = 00), 1/10 bias drive (BS2/1/0 = 000), Weak contrast (CT5-0 = 00000)
7. Entry mode set (REV = 0: Normal display, I/D = 1: Increment by 1, GR = 0: Character display mode, RDM = 0: Automatically update after reading, SPR = 0: Character display mode)
8. Cursor display off (B/W = 0, C = 0, B = 0)
9. Display on/off control (D = 0: Display off, CEN = 0: Normal position, LC = 0: Line-cursor off)
10. Display line control (NL3/2/1/0 = 1001: 1/80 duty ratio)
11. Double-height display off (DL10–1 = 0000000000)
12. Vertical scroll control (SN3/2/1/0 = 0000: First line displayed at the top, SL2/1/0: First raster-row displayed at the top of the first line, PS1/0 = 00: Partial scroll off)
13. CGROM memory bank 0 selection (RL10–1 = 0000000000)
14. Key scan control (IRE = 0: Key scan interrupt (IRQ) generation disabled, KF1/0 = 00: Key scan set to 64 cycles, KSB = 0: Key standby mode off)
15. Port control (PT2/1/0 = 000: PORT2/1/0 output = GND level)
16. 1/64-divided clock boost (DCC = 0)
17. B-pattern waveform AC drive (B/C = 0, EOR = 0, NW4/3/2/1/0 = 00000)

RAM Data Initialization:

1. DDRAM

   All addresses are initialized to 20H by the clear display instruction after the reset is canceled.
2. CGRAM/SEGRAM

   This is not automatically initialized by reset input but must be initialized by software while display is off (D = 0).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Booster output pins (VLOUT): Outputs GND level
3. Oscillator output pin (OSC2): Outputs oscillation signal
4. Key strobe pins (KST0 to KST3): Output strobe signals at specified time intervals
5. Key scan interrupt pin (IRQ*): Outputs V_{CC} level
6. General output ports (PORT0–PORT2): Output GND level

Serial Data Transfer

Setting the IM1 and IM2 pins (interface mode pins) to the GND level allows standard clock-synchronized serial data transfer, using the chip select line (CS*), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the IM0/ID pin function uses an ID pin.

The HD66728 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66728 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66728. The HD66728, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66728 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an instruction can be issued or key scan data can be read, and when RS = 1, data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit) as shown in table 26.

After receiving the start byte, the HD66728 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. To transfer data consecutively, note that only the display-clear instruction requires a longer execution time than the others (see table 24, Instruction List).

Two bytes of RAM read data after the start byte are invalid. The HD66728 starts to read correct RAM data from the third byte.

Write a dummy instruction (00H) before the key scan data is read.

Table 25 Start Byte Format

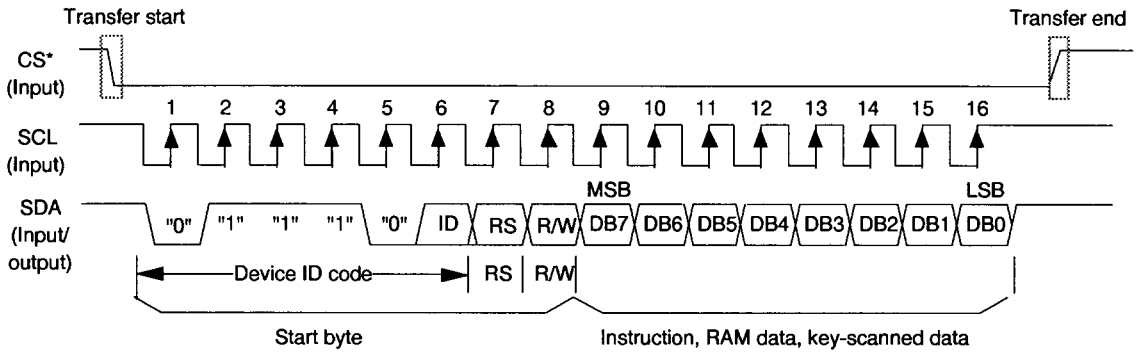
Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

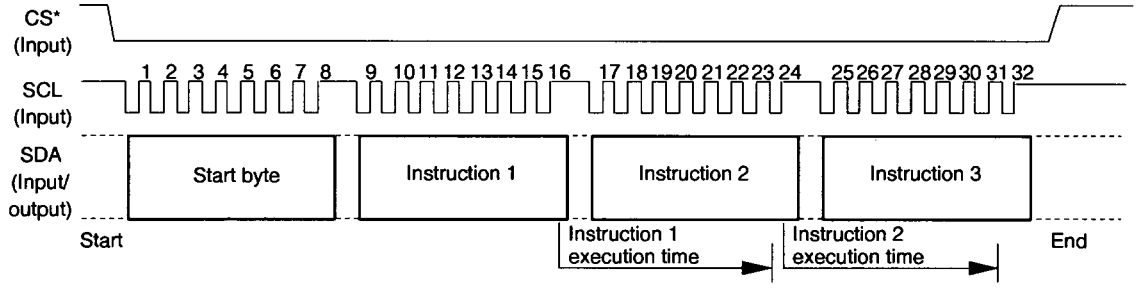
Table 26 RS and R/W Bit Function

RS	R/W	Function
0	0	Writes instruction
0	1	Reads key scan data
1	0	Writes RAM data
1	1	Reads RAM data

a) Basic Data-transfer Timing through Clock-synchronized Serial Bus Interface

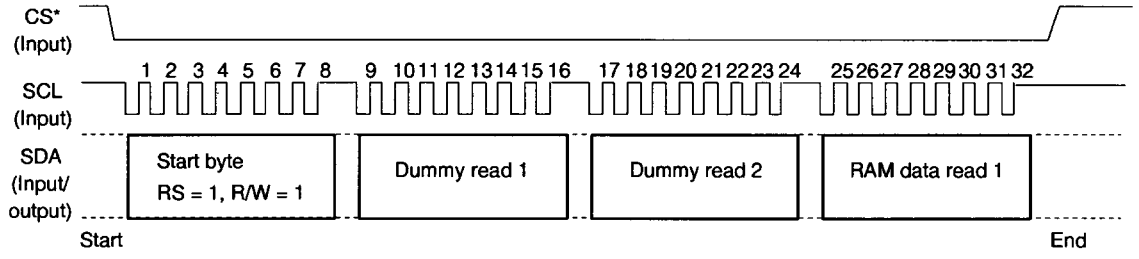


b) Consecutive Data-transfer Timing through Clock-synchronized Serial Bus Interface



Note: When instruciton 1 is a clear display instruction, adjust the transfer rate so that the 8th bit of instruction 2 is transferred after execution of the clear display instruction.

c) RAM Data Read-transfer Timing



Note: Two bytes of the RAM read data after the start byte are invalid. The HD66728 starts to read the correct RAM data from the third byte.

Figure 29 Clock-synchronized Serial Interface Timing Sequence

Key Scan Control

The key matrix scanner senses and holds the key states at each rising edge of key strobe signals (KST) that are output by the HD66728. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key state of eight inputs KIN0 to KIN7, enabling up to 32 keys to be scanned.

The states of inputs KIN0 to KIN7 are sampled by key strobe signal KST0 and latched into the SCAN0 register. Similarly, the data sampled by strobe signals KST1 to KST3 is latched into the SCAN1 to SCAN3 registers, respectively. Key pressing is stored as 1 in these registers.

The generation cycle and pulse width of the key strobe signals depend on the operating frequency (oscillation frequency) of the HD66728 and the key scan cycle determined by the KF0 and KF1 bits. For example, when the operational frequency is 80 kHz and KF0 and KF1 are both 10, the generation cycle is 3.2 ms and the pulse width is 0.8 ms. When the operating frequency (oscillation frequency) is changed, the above generation cycle and the pulse width are changed in inverse proportion.

In order to compensate for the mechanical features of the keys, such as chattering and noise and for the key-strobe generation cycle and the pulse width of the HD66728, software should read the scanned data two to three times in succession to obtain valid data. Multiple keypress combinations should also be processed in the software.

Up to three keys can be pressed simultaneously. Note, however, that if the third key is pressed on the intersection between the rows and columns of the first two keys pressed, incorrect data will be sampled. For three-key input, the third key must be on a separate column or row.

Additionally, the HD66728 supports the key standby mode in which only the key scan circuit enters the standby state. When 1 is set to the key standby mode setting bit (KSB), only key scanning is stopped. In this case, as well as in the normal standby mode, the key scan interrupt function can be used. For example, this function is used when only key scanning is stopped to improve the sensitivity of the wave received by a radio system during calling.

The input pins KIN0 to KIN7 are pulled up to V_{CC} with internal MOS transistors (see the Electrical Characteristics section). External resistors may also be required to further pull the voltages up when the internal pull-ups are insufficient for the desired noise margins or for a large key matrix.

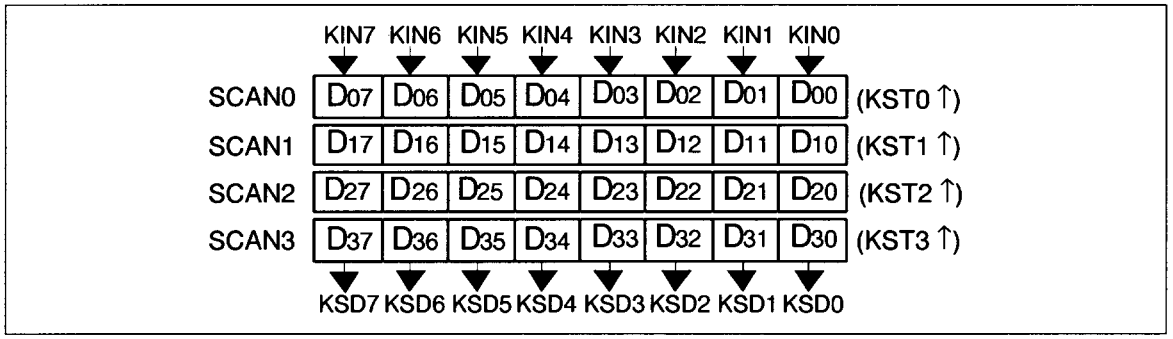


Figure 30 Key Scan Register Configuration

Table 27 Key Scan Cycles for Each Operating Frequency

KF1	KF0	Key Scan Pulse Width	Key Scan Cycle
0	0	0.2 ms	0.8 ms (64 clock cycles)
0	1	0.4 ms	1.6 ms (128 clock cycles)
1	0	0.8 ms	3.2 ms (256 clock cycles)
1	1	1.6 ms	6.4 ms (512 clock cycles)

Note: The data is a value obtained when the oscillation frequency (fosc) is 80 kHz. The value depends on the oscillation frequency.

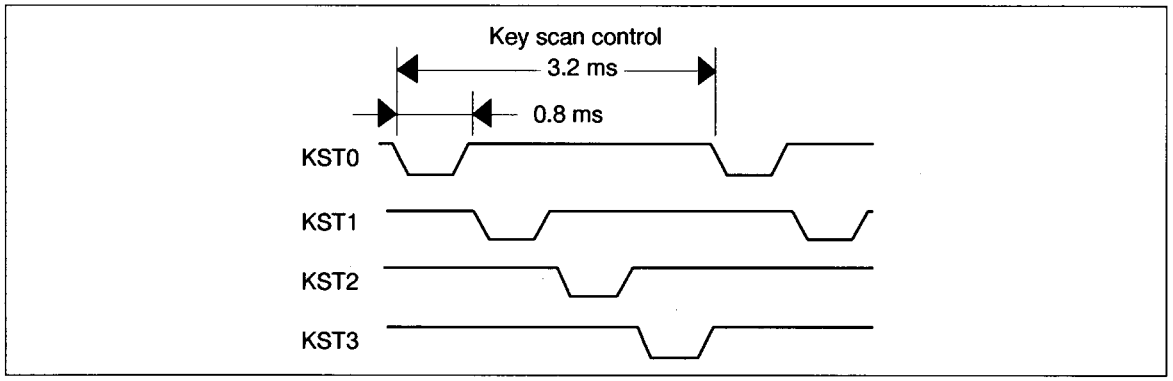


Figure 31 Key Strobe Output Timing (KF1/0 = 10, fcp/fosc = 80 kHz)

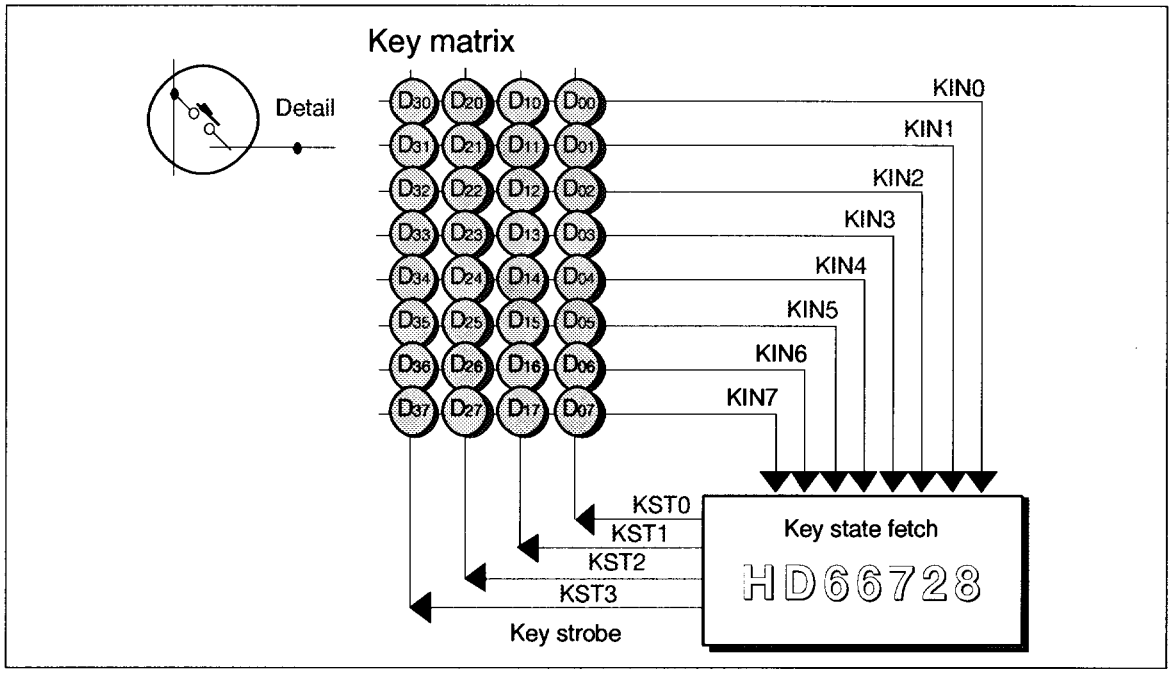


Figure 32 Key Scan Configuration

The key-scanned data can be read by an MPU via a serial interface. First, a start byte should be transferred. After the HD66728 has received the start byte, the MPU reads scan data KSD7 to KSD0 from the SCAN0 register starting from the MSB. Similarly, the MPU reads data from SCAN1, SCAN2 and SCAN3 in that order. After reading SCAN3, the MPU starts at SCAN0 again.

The HD66728 may be read out while it is latching scan data and is thus unstable. Consequently, it should also be reconfirmed with software if required.

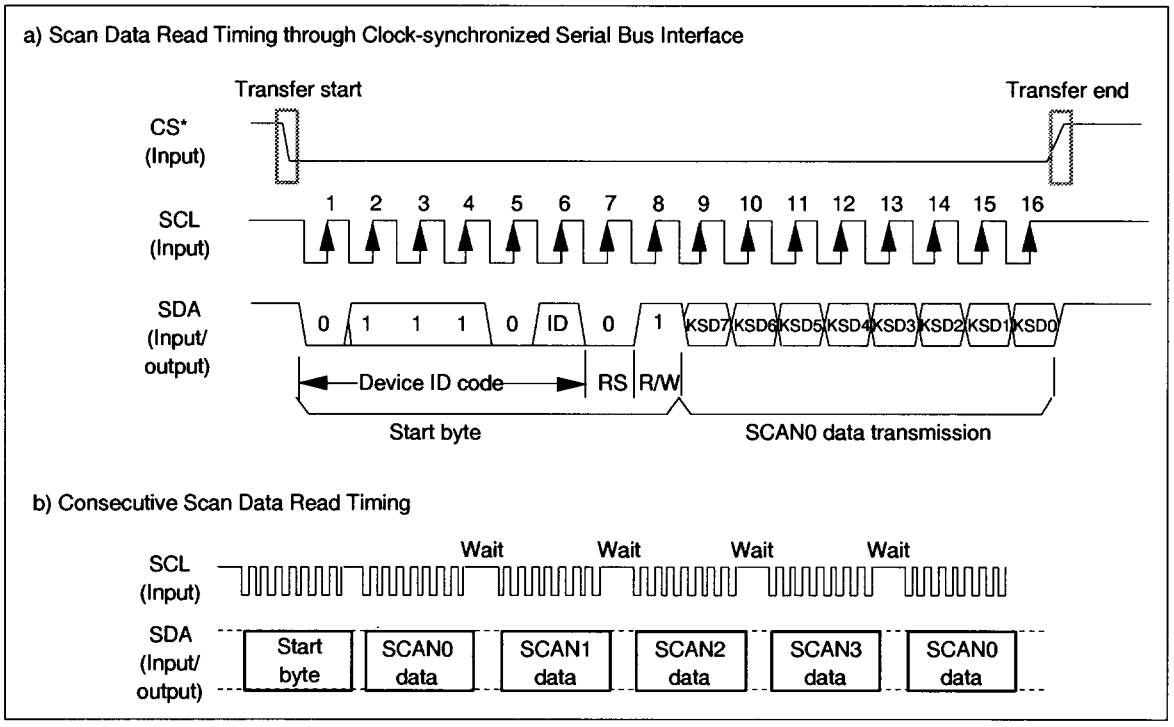


Figure 33 Scan Data Serial Transfer Timing

Key Scan Interrupt (Wake-up Function)

If the interrupt enable bit (IRE) is set to 1, the HD66728 sends an interrupt signal to the MPU on detecting that a key has been pressed in the key scan circuit by setting the IRQ* output pin to a low level. An interrupt signal can be generated by pressing any key in a 32-key matrix. The interrupt level continues to be output during the key scan cycle while the key is being pressed.

Normal key scanning is performed and interrupts can occur in the HD66728 sleep mode (SLP = 1). Accordingly, power consumption can be minimized in the sleep mode, by triggering the MPU to read key states via the interrupt which is generated only when the HD66728 detects a key input. For details, see the Sleep Mode section.

On the other hand, normal key scanning and the internal operating clock stop in the standby mode (STB = 1) or in the key standby mode (KSB = 1). During this period, the KST0 output is kept low, so the HD66728 can always monitor eight key inputs (KIN0-KIN7) connected to KST0 when RS = GND. Therefore, if any of the eight keys is pressed, an interrupt occurs. When RS = Vcc, all outputs KST0 to KST3 are kept low, so the HD66728 can always monitor 32 key inputs. If any of 32 keys is pressed, an interrupt occurs. Accordingly, power consumption or noise generation can further be minimized in the standby mode, where the whole system is inactive, by triggering the MPU via the interrupt which is generated only when the HD66728 detects a key input from the above keys. For details, see the Standby Mode section.

The IRQ* output pin is pulled up to V_{CC} with an internal MOS resistor of approximately 50 kΩ. Additional external resistors may be required to obtain stronger pull-ups. Interrupts may occur if noise occurs in KIN0-KIN7 input during key scanning. Interrupts must be inhibited if not needed by setting the interrupt enable bit (IRE) to 0.

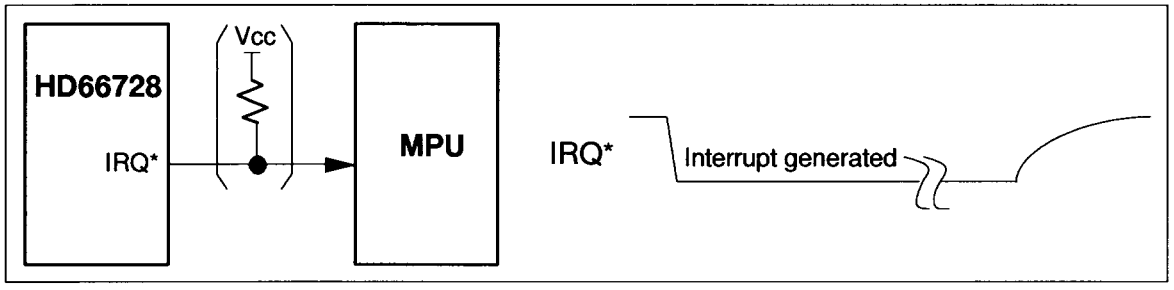


Figure 34 Interrupt Generator

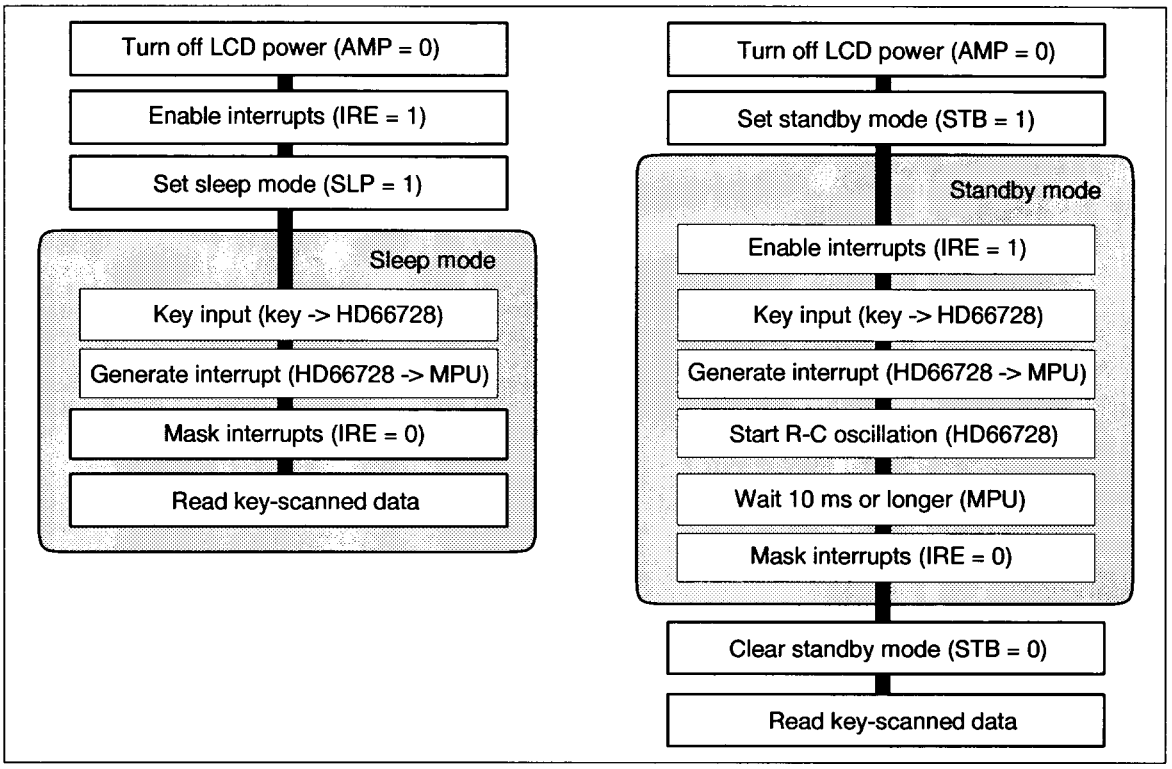


Figure 35 Key Scan Interrupt Processing Flow in Sleep and Standby Modes

Parallel Data Transfer

8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/Vcc/GND level allows E-clock-synchronized 8-bit parallel data transfer. Setting the IM2/1/0 (interface mode) to the Vcc/Vcc/GND level allows 80-system 8-bit parallel data transfer. When the number of buses or the mounting area is limited, use a 4-bit bus interface or serial data transfer.

Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

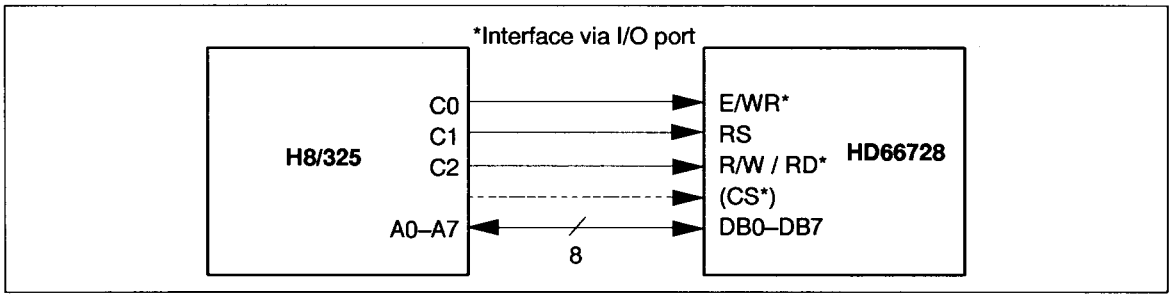


Figure 36 Interface to 8-bit Microcomputer

4-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/Vcc/Vcc level allows E-clock-synchronized 4-bit parallel data transfer using pins DB7/KIN7-DB4/KIN4. Setting the IM2/1/0 (interface mode) to the Vcc/Vcc/Vcc level allows 80-system 4-bit parallel data transfer. The 8-bit instructions and RAM data are divided into four upper/lower bits and the transfer starts from the upper four bits.

Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

Note: Transfer synchronization function for a 4-bit bus interface
The HD66728 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 4-bit data transfer in the 4-bit bus interface. Noise causing transfer mismatch between the four upper and lower bits can be corrected by a reset triggered by consecutively writing a 0000 instruction four times. The next transfer starts from the upper four bits. Executing synchronization function periodically can recover any runaway in the display system.

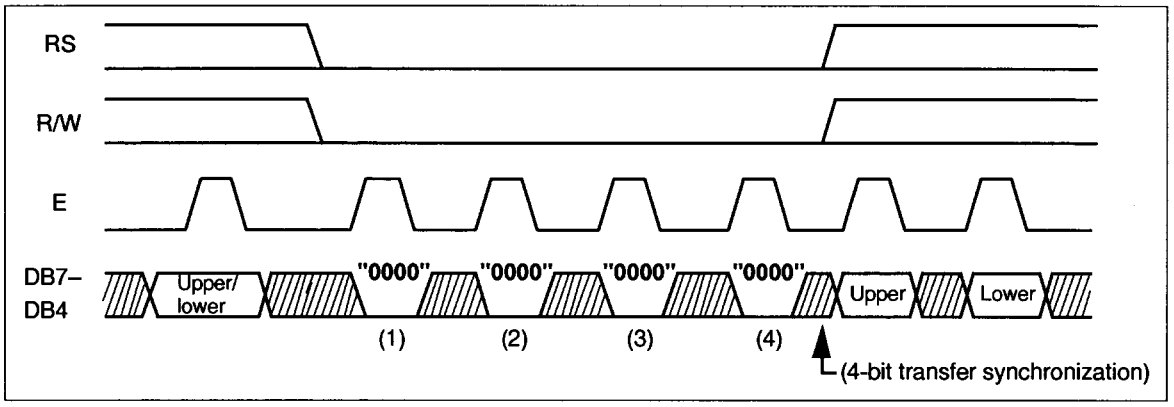


Figure 37 4-bit Transfer Synchronization

Oscillation Circuit

The HD66728 can either be supplied with operating pulses externally (external clock mode) or oscillate using an internal R-C oscillator with an external oscillator-resistor (external resistor oscillation mode). Note that in R-C oscillation, the oscillation frequency is changed according to the internal capacitance value, the external resistance value, or operating power-supply voltage. Consumption current can be lowered by 10 µA in the external clock mode.

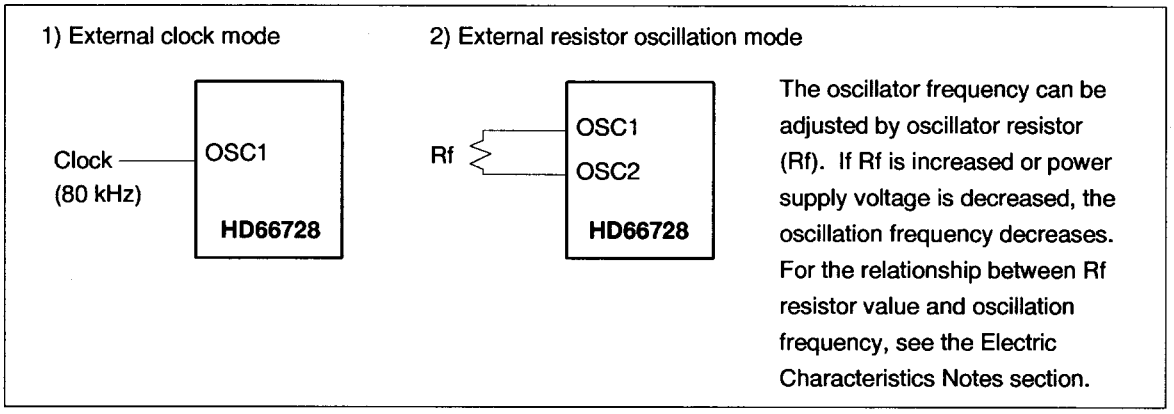


Figure 38 Oscillation Circuits

Table 28 Relationship between Drive Duty Ratio and Frame Frequency (fosc = 75 kHz)

	Display mode									
	1-line Display	2-line Display	3-line Display	4-line Display	5-line Display	6-line Display	7-line Display	8-line Display	9-line Display	10-line Display
	Set value for NL3–0									
LCD Drive	**0000**	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1000**	**1001**
Multiplexing duty ratio	1/8	1/16	1/24	1/32	1/40	1/48	1/56	1/64	1/72	1/80
Drive bias (recommend-ed value)	1/4	1/5	1/6	1/6	1/7	1/8	1/8	1/9	1/9.5	1/10
Frame frequency	73 Hz	73 Hz	73 Hz	73 Hz	72 Hz	74 Hz	74 Hz	73 Hz	65 Hz	59 Hz
One-frame frequency	1,024	1,024	1,032	1,024	1,040	1,008	1,008	1,024	1,152	1,280

Note: If the frame frequency is low and the display flickers, increase the oscillation frequency (fosc). Particularly in the 9-line display and 10-line display modes, note that the frame frequency is lowered.

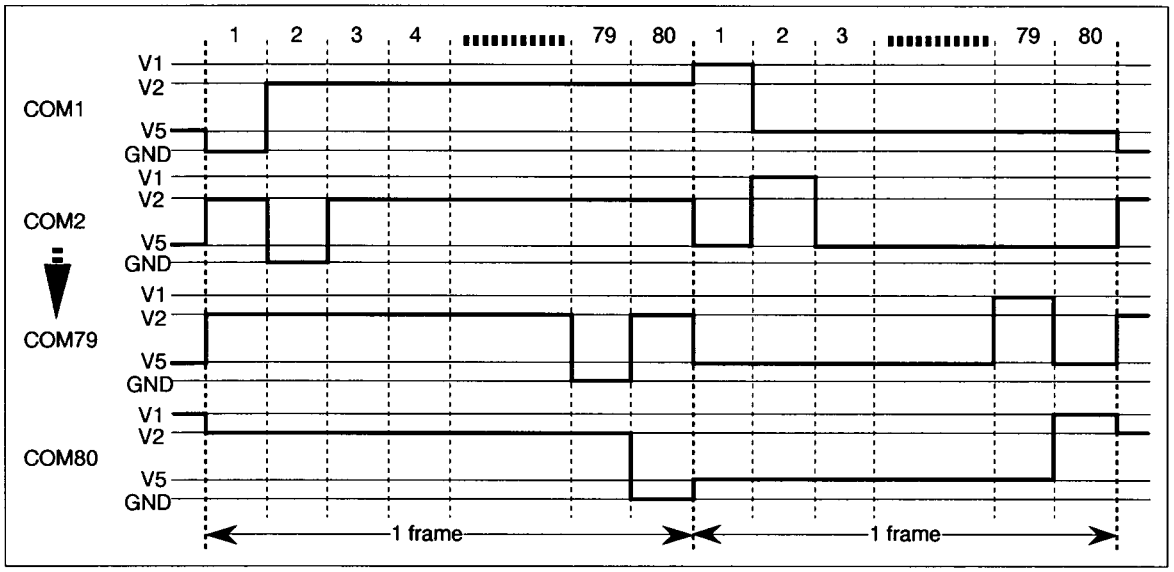
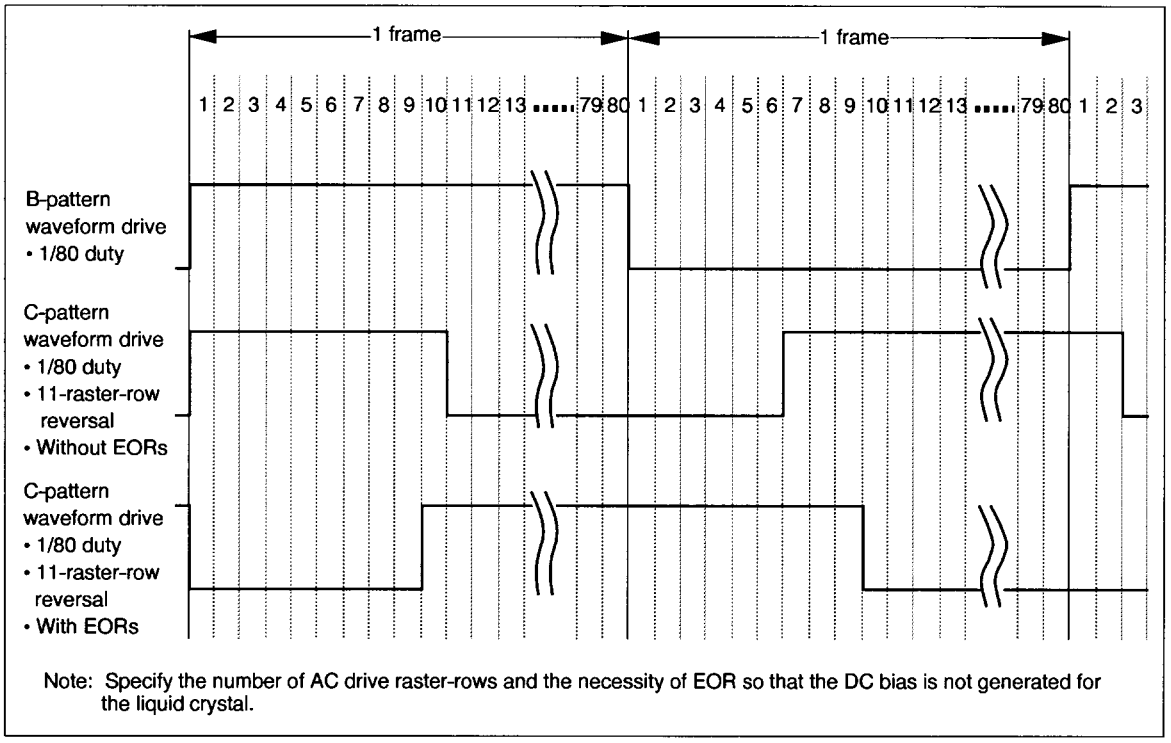


Figure 39 LCD Drive Output Waveform (B-pattern AC Drive with 1/80 Multiplexing Duty Ratio)

n-raster-row Reversed AC Drive

The HD66728 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 32 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than five lines (1/40 duty), the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality. Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Note: Specify the number of AC drive raster-rows and the necessity of EOR so that the DC bias is not generated for the liquid crystal.

Figure 40 Example of an AC Signal under n-raster-row Reversed AC Drive

Liquid Crystal Display Voltage Generator

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal booster, circuits should be connected as shown in figure 41. Here, contrast can be adjusted by software through the CT bits of the contrast adjustment register.

The HD66728 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential differences between V_{LCD} and V1 and between V5 and GND must be 0.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.

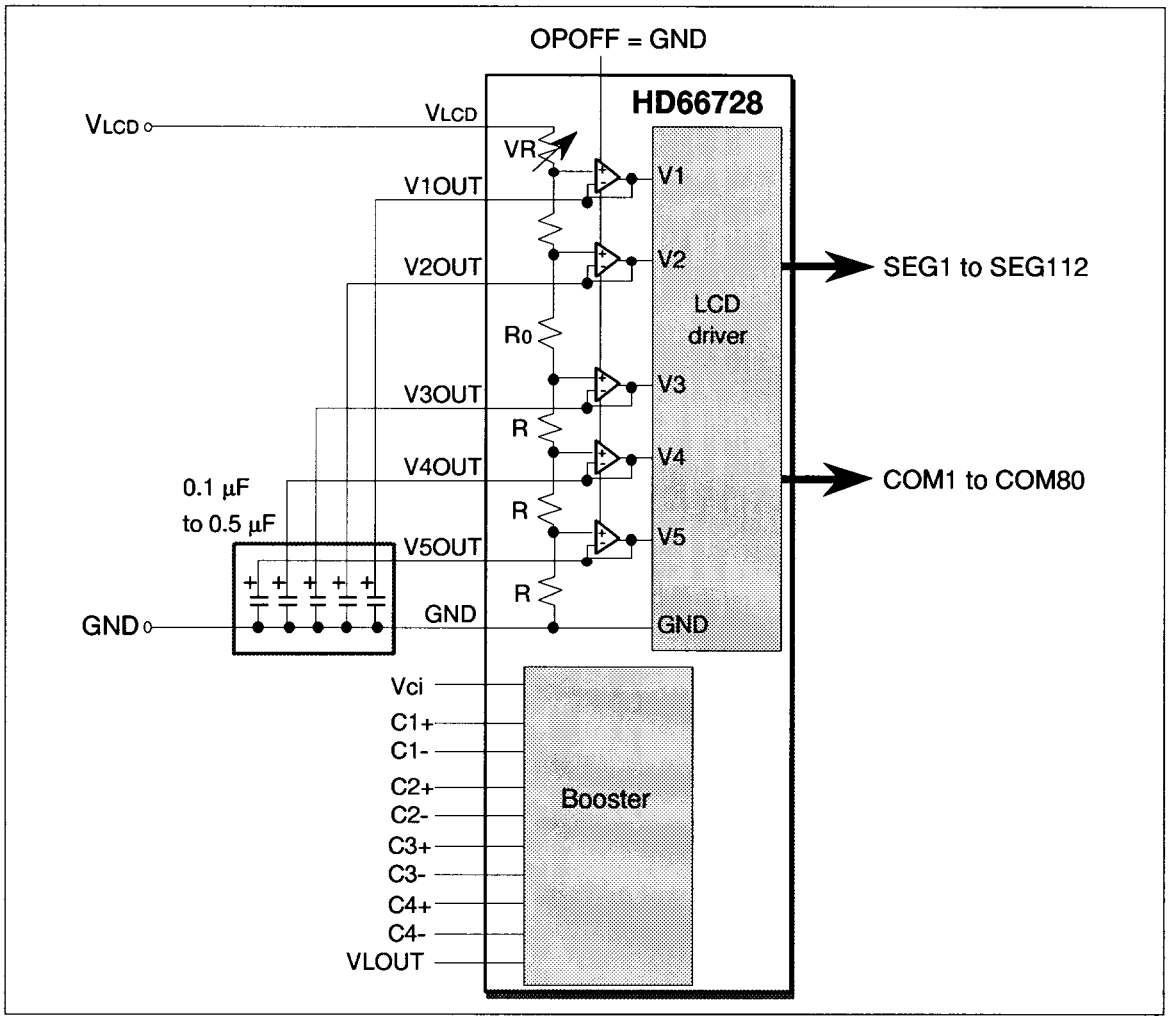


Figure 41 External Power Supply Circuit for LCD Drive Voltage Generation

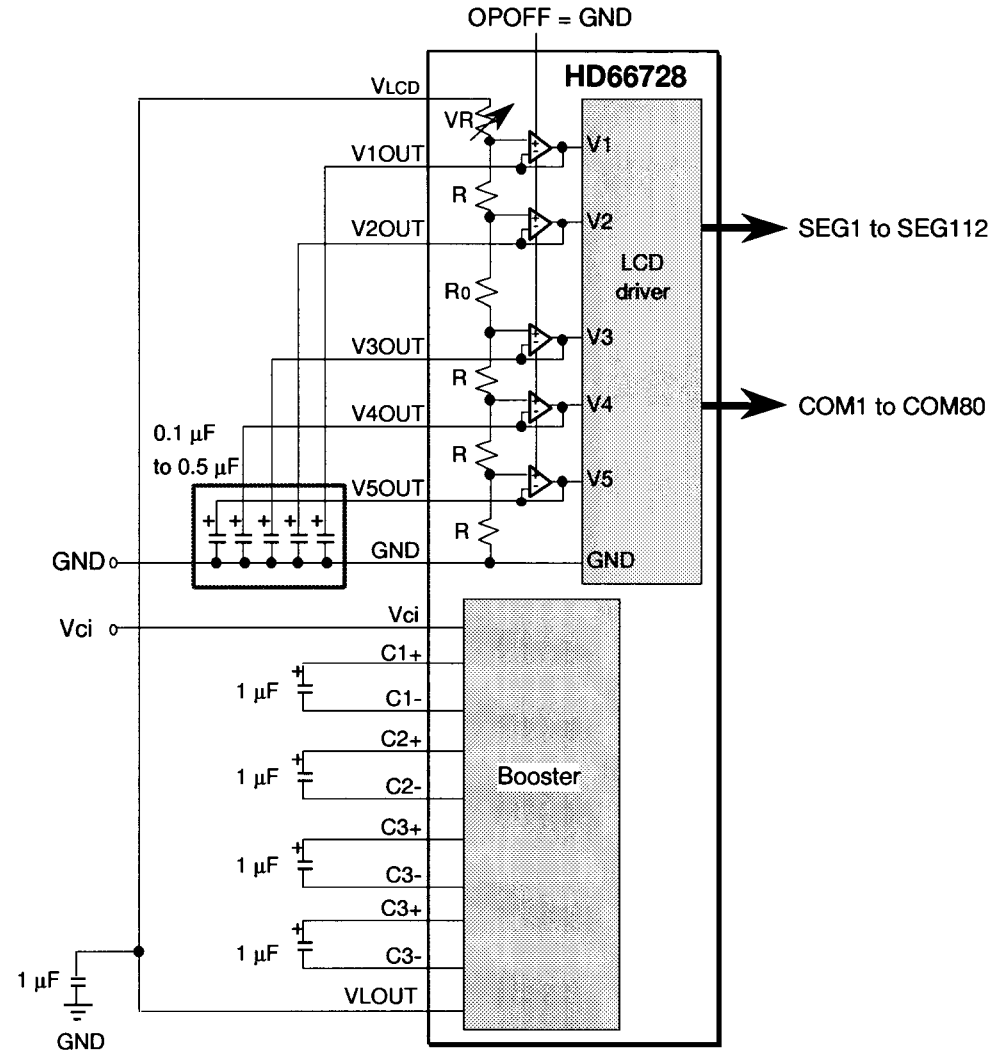
When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal booster, circuits should be connected as shown in figure 42. Here, contrast can be adjusted through the CT bits of the contrast control instruction. Temperature can be compensated either through the CT bits or by controlling the reference voltage for the booster (Vci pin) using a thermistor.

Note that Vci is both a reference voltage and power supply for the booster. The reference voltage must therefore be adjusted using an emitter-follower or a similar element so that sufficient current can be supplied. In this case, Vci must be equal to or smaller than the V_{CC} level.

The HD66728 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, the potential differences between V_{LCD} and V1 and between V5 and GND must be 0.4 V or higher.

Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.



Notes: 1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the liquid-crystal power supply voltage (17 V). Particularly, Vci must be 3.3 V or less for five-times boosting.
2. Vci is both a reference voltage and power supply for the booster; connect it to Vcc directly or combine it with a transistor so that sufficient current can be obtained.
3. Polarized capacitors must be connected correctly.
4. Circuits for temperature compensation should be based on the sample circuit in figure 43.

Figure 42 Internal Booster for LCD Drive Voltage Generation

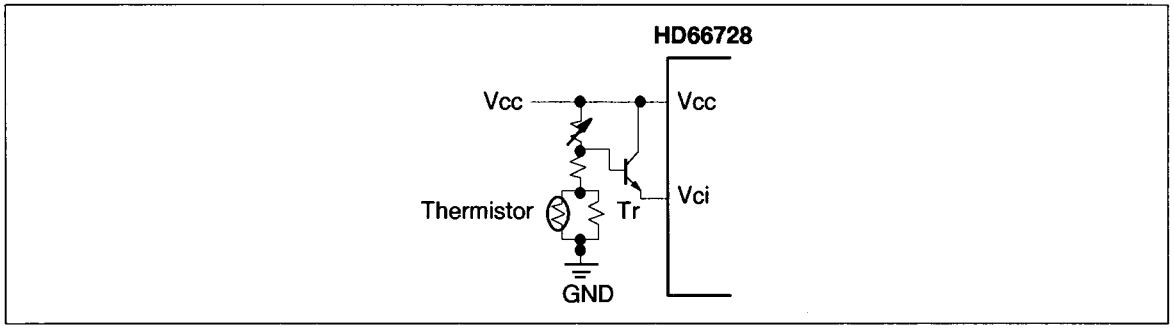


Figure 43 Temperature Compensation Circuit

Switching the Boosting Multiplying Factor

Instruction bits (BT1/0 bits) can optionally select the boosting multiplying factor of the internal booster. According to the display status, power consumption can be reduced by changing the LCD drive duty and the LCD drive bias, and by controlling the boosting multiplying factor for the minimum requirements. For details, see the Partial-display-on Function section.

Due to the maximum boosting multiplying factor, the following external capacitor needs to be connected. For example, when the maximum boosting is quadrupled, the capacitors between C4+ and C4– for five-times boosting are not needed, so these pins must be open.

Table 29 VLOUT Output Status

BT1	BT0	VLOUT Output Status
0	0	Triple boosting output
0	1	Quadruple boosting output
1	0	Five-times boosting output
1	1	Setting inhibited

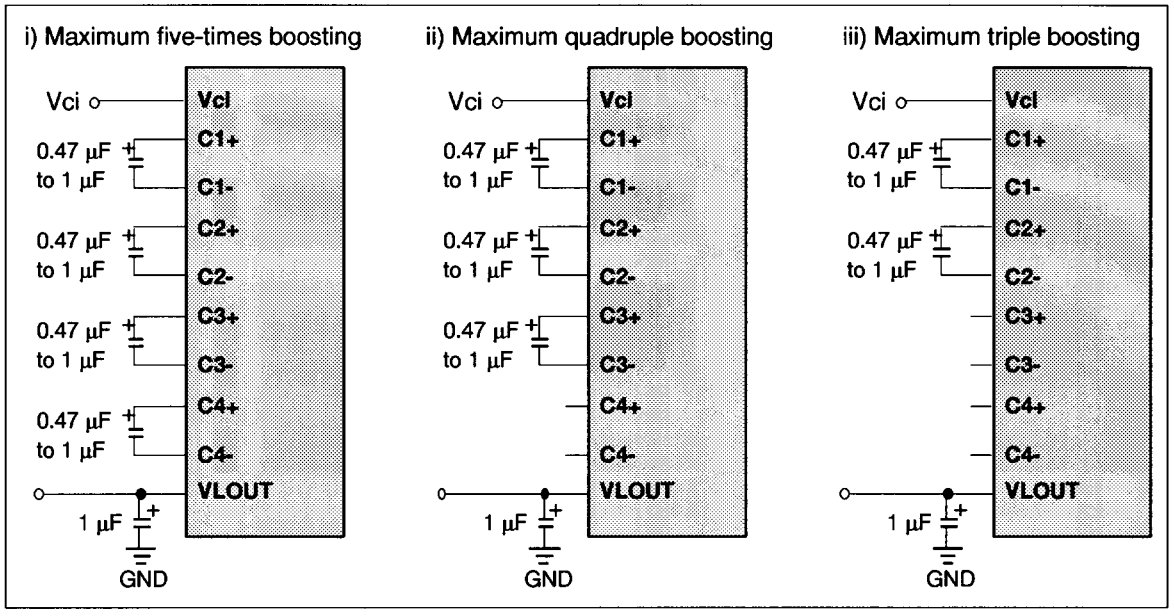


Figure 44 Booster Output Multiplying Factor Switching

Example of Power-supply Voltage Generator for More Than Five-times Boosting Output

The HD66728 incorporates the booster for up to five-times boosting. However, the LCD drive voltage (VLCD) will not be enough for five-times boosting from Vcc when the power-supply voltage of Vcc is low or when the LCD drive voltage is high for the high-contrast LCD display. In this case, the reference voltage (Vci) for boosting can be set higher than the power-supply voltage of Vcc.

Set the Vci input voltage for the booster to 5.5 V or less within the range of Vcc + 1.0 V. Control the Vci voltage so that the boosting output voltage (VLOUT) should be less than the absolute maximum ratings (17 V).

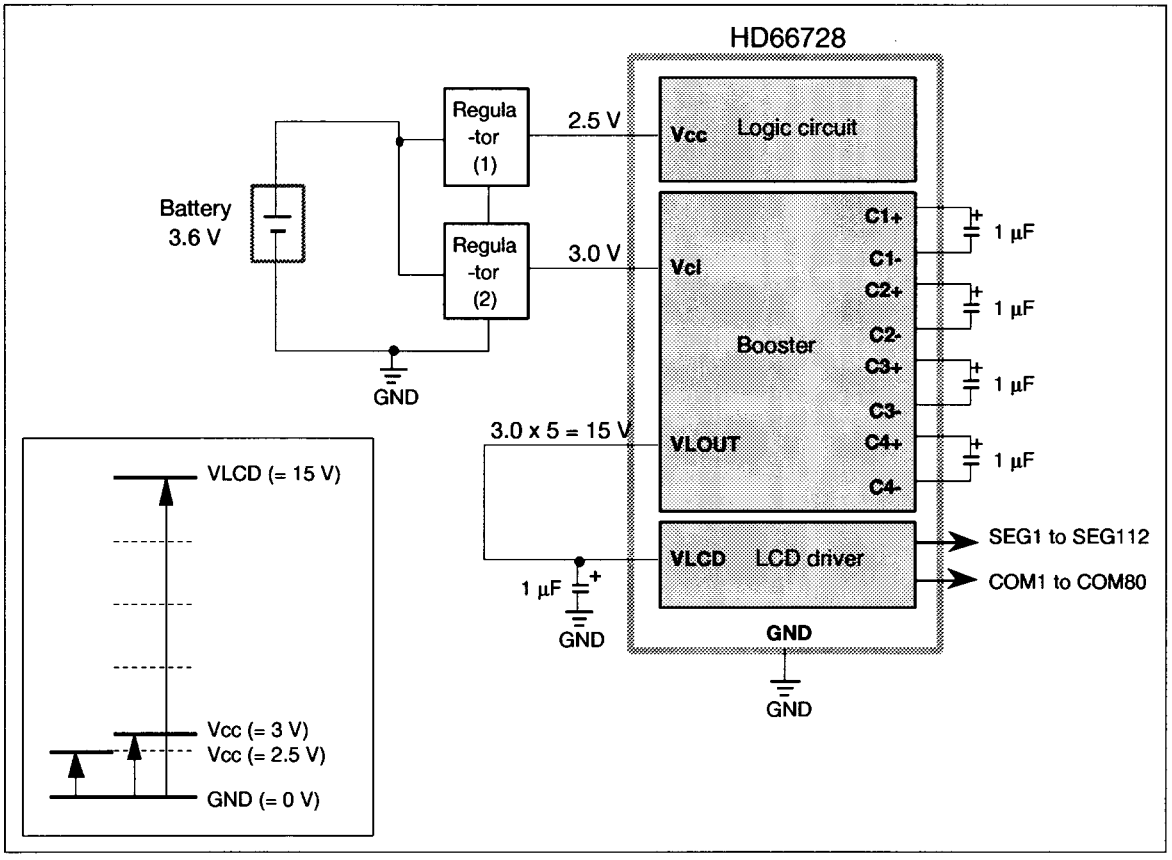
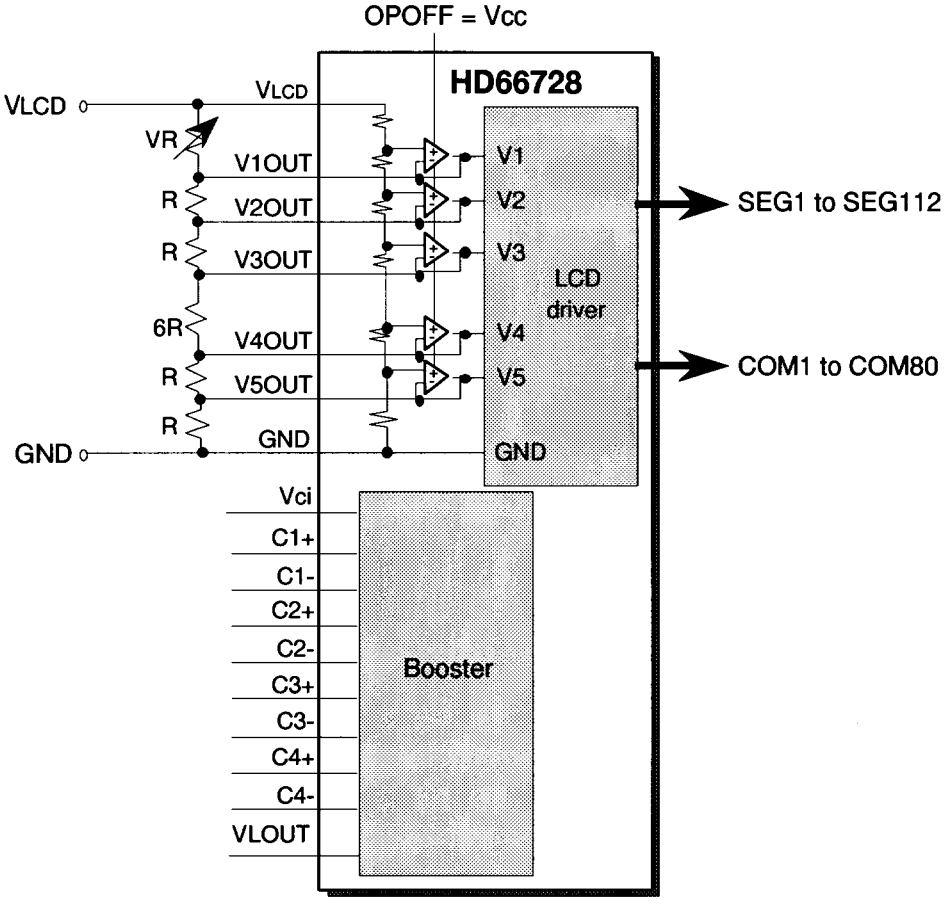


Figure 45 Usage Example of Booster at Vci > Vcc

When External Bleeder Resistors are Used

When internal operational amplifiers cannot fully drive the LCD panel used, V1 to V5 voltages can be supplied through external bleeder resistors or external voltage follower operational amplifier (figure 46). Here, the OPOFF pin must be set to the V_{CC} level to turn off the internal operational amplifiers. Since the internal contrast adjuster is disabled, contrast must be adjusted externally. Connection of external bleeder-resistors can specify a given bias value from 1/4 to 1/10. Figure 46 shows connection for 1/10-bias drive voltage generation. Internal boosters can be used as they are. However, use the external power supply since the through current in bleeder resistors becomes large, loads in the internal booster are heavy, and the boosting output voltage drops.



Notes:
1. Resistance of each external bleeder resistor should be 2 kΩ to 10 kΩ.
2. When 0.1 µF to0.5 µF capacitors are added in parallel with each external bleeder resistor, resistance can be increased, and the through current in the bleeder resistors can be reduced (see figure 47).
3. The bias current value for driving LCDs can be varied by adjusting the resistance (6R) between the V3OUT and V4OUT pins.
4. The internal contrast adjuster is disabled; contrast must be adjusted either by controlling the external variable resistor between VLCD and V1 for the booster.
5. Vci is both a reference voltage and power supply for the booster; connect it to Vcc directly or combine it with a transistor so that sufficient current can be obtained.

Figure 46 Circuit Using External Bleeder Resistors

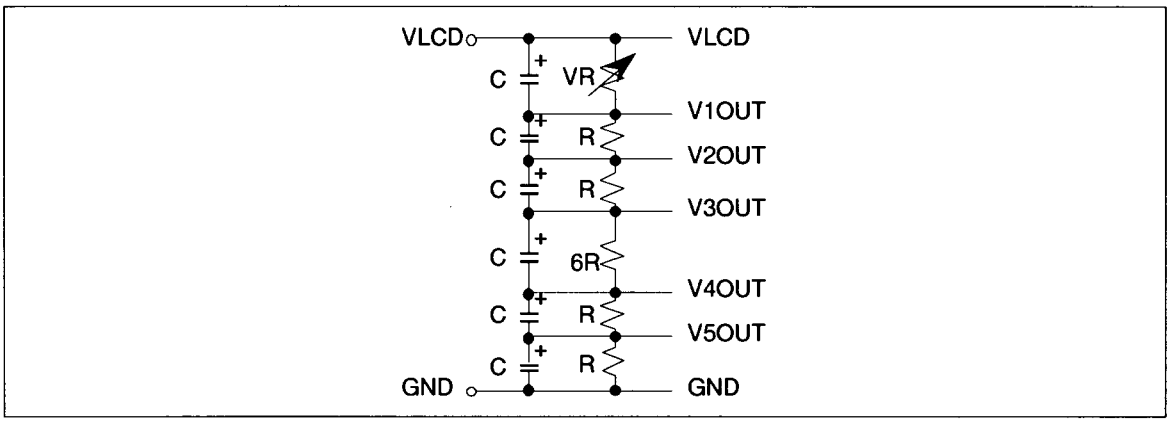


Figure 47 Low-current Consumption Bleeder Resistor

Contrast Adjuster

Software can adjust 64-step contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between V_{LCD} and V1) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor between V_{LCD} and V1 (VR) can be precisely adjusted in a 0.05 x R unit within a range from 0.05 x R through 3.20 x R, where R is a reference resistance obtained by dividing the total resistance.

The HD66728 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages. Thus, CT5-0 bits must be adjusted so that the potential differences between V_{LCD} and V1 and between V5 and GND are 0.4 V or higher when liquid-crystal drives, particularly when the VR is small.

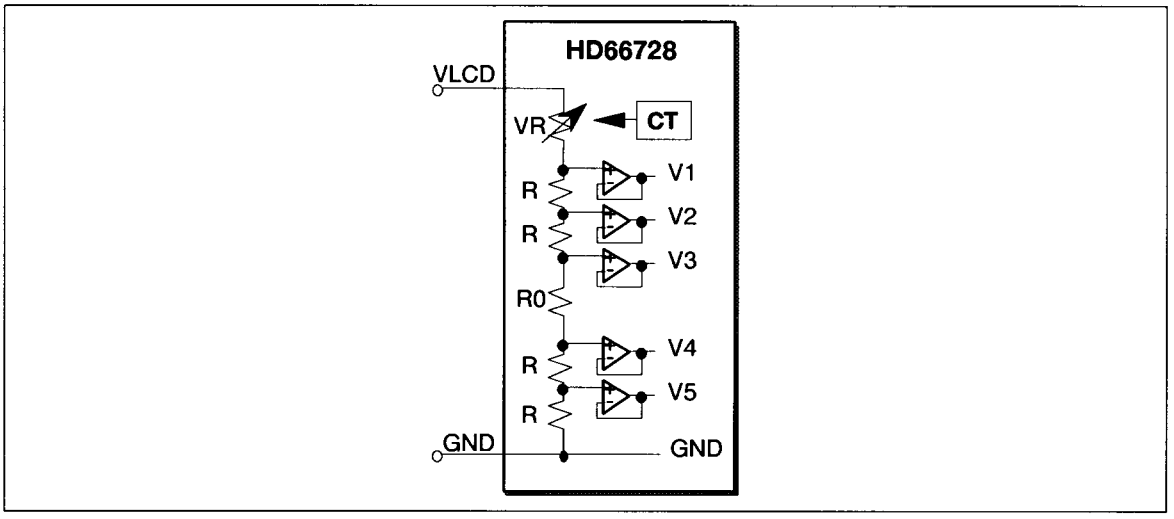


Figure 48 Contrast Adjuster

Table 30 Contrast Adjustment Bits (CT) and Variable Resistor Values

CT Set Value						Variable Resistor Value (VR)	Potential Difference between V1 and GND	Display Color
CT5	CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	0	3.20 x R	(Small)	(Light)
0	0	0	0	0	1	3.15 x R		
0	0	0	0	1	0	3.10 x R		
0	0	0	0	1	1	3.05 x R		
0	0	0	1	0	0	3.00 x R		
0	0	0	1	0	1	2.95 x R		
0	0	0	1	1	0	2.90 x R		
0	0	0	1	1	1	2.85 x R		
0	0	1	0	0	0	2.80 x R		
0	0	1	0	0	1	2.75 x R		
0	0	1	0	1	0	2.70 x R		
0	0	1	0	1	1	2.65 x R		
0	0	1	1	0	0	2.60 x R		
0	1	1	1	1	1	1.65 x R		
1	0	0	0	0	0	1.60 x R		
1	0	0	0	0	1	1.55 x R		
1	0	0	0	1	0	1.50 x R		
1	0	0	0	1	1	1.45 x R		
1	0	0	1	0	0	1.40 x R		
1	0	0	1	0	1	1.35 x R		
1	0	0	1	1	0	1.30 x R		
1	0	0	1	1	1	1.25 x R		
1	0	1	0	0	0	1.20 x R		
1	1	1	0	0	1	1.15x R		
1	1	1	1	0	0	0.20 x R		
1	1	1	1	0	1	0.15 x R		
1	1	1	1	1	0	0.10 x R		
1	1	1	1	1	1	0.05 x R	(Large)	(Deep)

Table 31 Contrast Adjustment per Bias Drive Voltage

Bias	LCD drive voltage: V_{DR}	Contrast adjustment range
1/10 bias drive	$\frac{10 \times R}{10 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.757 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.995 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{10 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{10 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/9.5 bias drive	$\frac{9.5 \times R}{9.5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.748 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.994 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{9.5 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{9.5 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/9 bias drive	$\frac{9 \times R}{9 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.737 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.994 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{9 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{9 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/8 bias drive	$\frac{8 \times R}{8 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.714 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.993 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{8 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{8 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/7 bias drive	$\frac{7 \times R}{7 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.686 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.993 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{7 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{7 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/6 bias drive	$\frac{6 \times R}{6 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.652 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.992 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{6 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{6 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/5 bias drive	$\frac{5 \times R}{5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.610 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.990 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{5 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{5 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/4 bias drive	$\frac{4 \times R}{4 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.556 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.988 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{4 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{4 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]

Liquid Crystal Display Drive Bias Selector

An optimum liquid crystal display bias value can be selected using BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL3-0 bits). Liquid crystal display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is an ideal value where the optimum contrast is obtained. Driving by using a lower value than the optimum bias value provides lower contrast and lower liquid crystal display voltage (potential difference between V1 and GND). When the liquid crystal display voltage is insufficient even if a five-times booster is used or output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid crystal bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT4-0 bits) and selecting the booster output level (BT1/0 bits).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N}+1}$$

Table 32 Optimum Drive Bias Values

LCD drive duty ratio	1/80	1/72	1/64	1/56	1/48	1/40	1/32	1/24	1/16	1/8
(NL3-0 set value)	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
Optimum drive bias value	1/10	1/9.5	1/9	1/8	1/8	1/7	1/6	1/6	1/5	1/4
(BS2-0 set value)	000	001	010	011	011	100	101	101	110	111

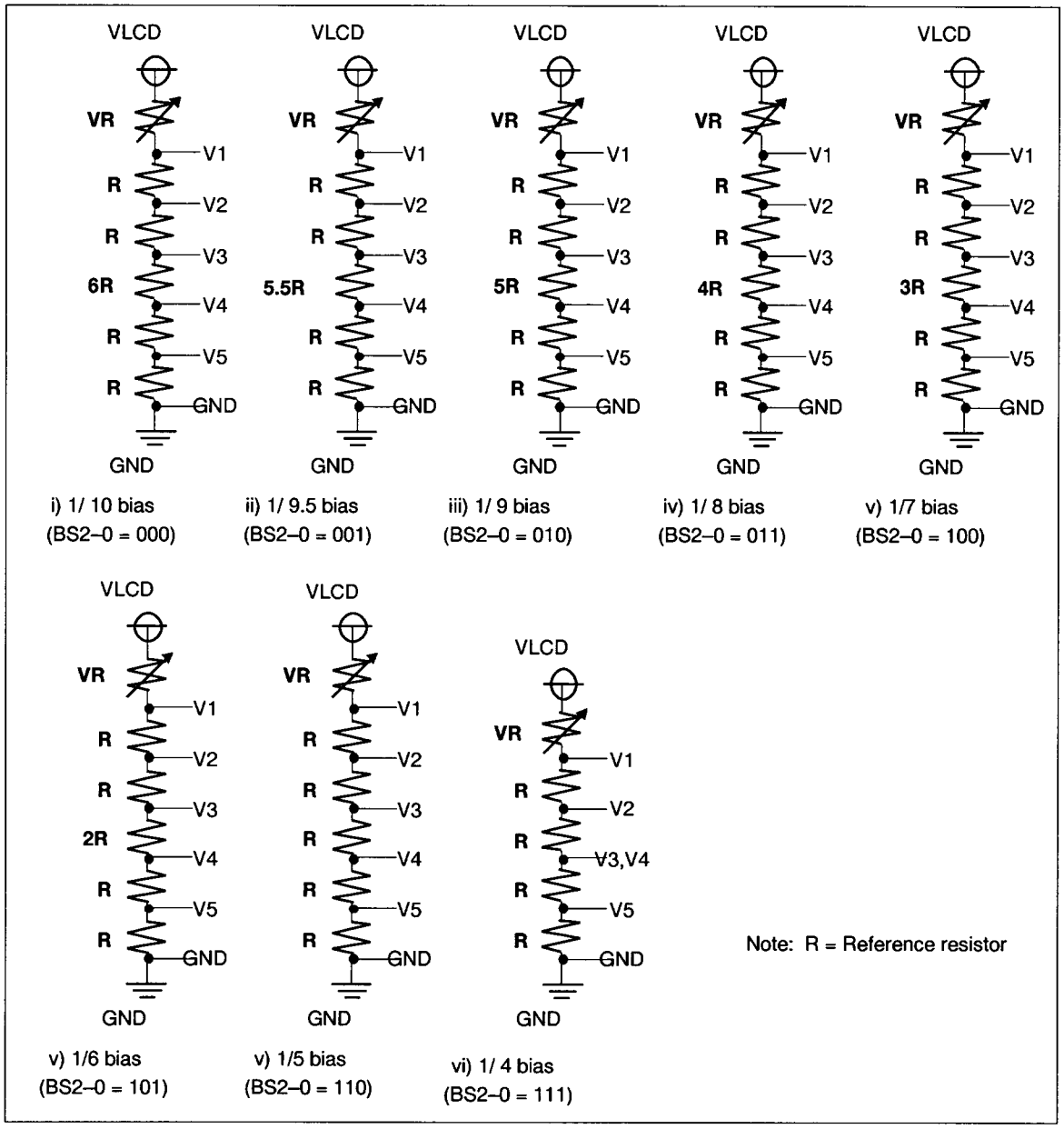


Figure 49 Liquid Crystal Display Drive Bias Circuit

LCD Panel Interface

The HD66728 has a function for changing the common driver/segment driver output shift direction using the CMS bit and SGS bit to meet the chip mounting positions of the HD66728. This is to facilitate the interface wiring to the LCD panel with COG or TCP installed.

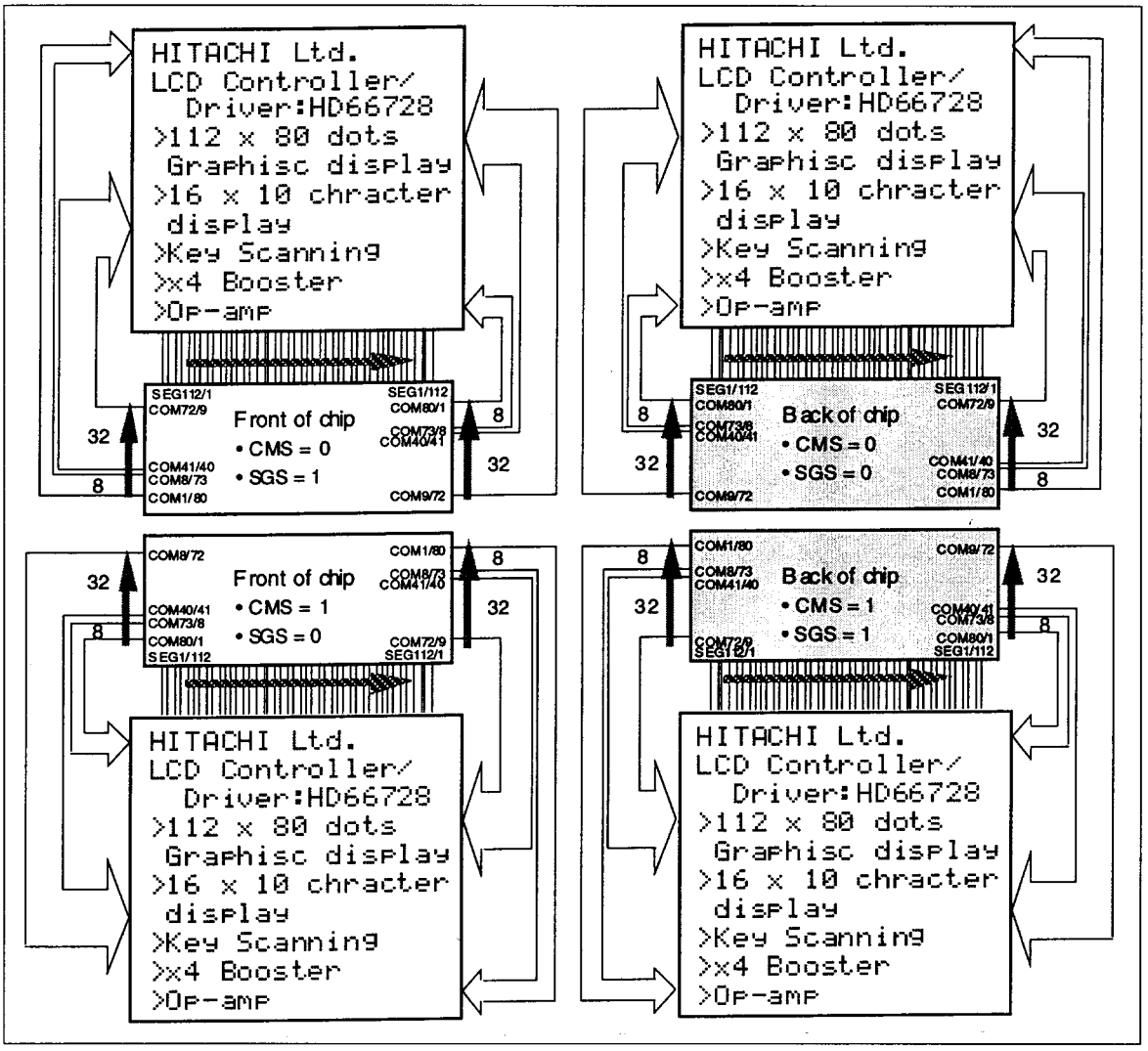


Figure 50 1/80 Duty Drive Pattern Wiring

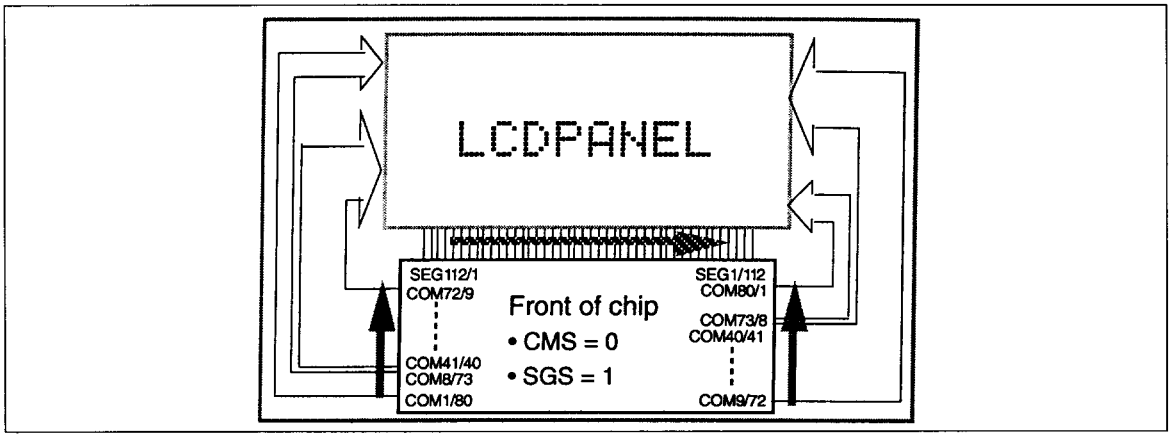


Figure 51 1-line Display Pattern Wiring

Table 33 Number of Left and Right Extension Lines of Common Driver

Drive Duty Ratio	Left Edge of Screen	Right Edge of Screen
1/48	16 (COM1–8, 41–48)	32 (COM9–40)
1/56	24 (COM1–8, 41–56)	32 (COM9–40)
1/64	32 (COM1–8, 41–64)	32 (COM9–40)
1/72	40 (COM1–8, 41–72)	32 (COM9–40)
1/80	40 (COM1–8, 41–72)	40 (COM9–40, 73–80)

CGROM Bank Switching Function

The HD66728 incorporates two pages of CGROM. Switching the memory bank in a display line unit using the CGROM bank switching bits (RL1 to RL10) can display a total of 432 font patterns. Since each display line switches memory bank 0/1, the number of fonts which can be displayed in the same display line is 240 CGROMs + 16 CGRAMs when memory bank 0 is selected, and 192 CGROMs + 64 CGRAMs when memory bank 1 is selected. Font displays for CGRAMs (1) to (16) are used in common with memory bank 0 and memory bank 1.

With the number of fonts is extended, multinational fonts, special symbols, and icons can be displayed. In addition, the character display mode can simply implement multiple displays: graphic pictograms or graphic mark displays that use a one-line display, and menu bar displays by using the black-and-white reversed fonts that are supported by the graphics display.

Table 34 RL Bit Setting

Bit Set Value	Set RLn = 0	Set RLn = 1
RL1 bit	The first line is displayed by memory bank 0.	The first line is displayed by memory bank 1.
RL2 bit	The second line is displayed by memory bank 0.	The second line is displayed by memory bank 1.
RL3 bit	The third line is displayed by memory bank 0.	The third line is displayed by memory bank 1.
RL4 bit	The fourth line is displayed by memory bank 0.	The fourth line is displayed by memory bank 1.
RL5 bit	The fifth line is displayed by memory bank 0.	The fifth line is displayed by memory bank 1.
RL6 bit	The sixth line is displayed by memory bank 0.	The sixth line is displayed by memory bank 1.
RL7 bit	The seventh line is displayed by memory bank 0.	The seventh line is displayed by memory bank 1.
RL8 bit	The eighth line is displayed by memory bank 0.	The eighth line is displayed by memory bank 1.
RL9 bit	The ninth line is displayed by memory bank 0.	The ninth line is displayed by memory bank 1.
RL10 bit	The 10th line is displayed by memory bank 0.	The 10th line is displayed by memory bank 1.

Table 35 Relationship between Character Code and Memory Bank

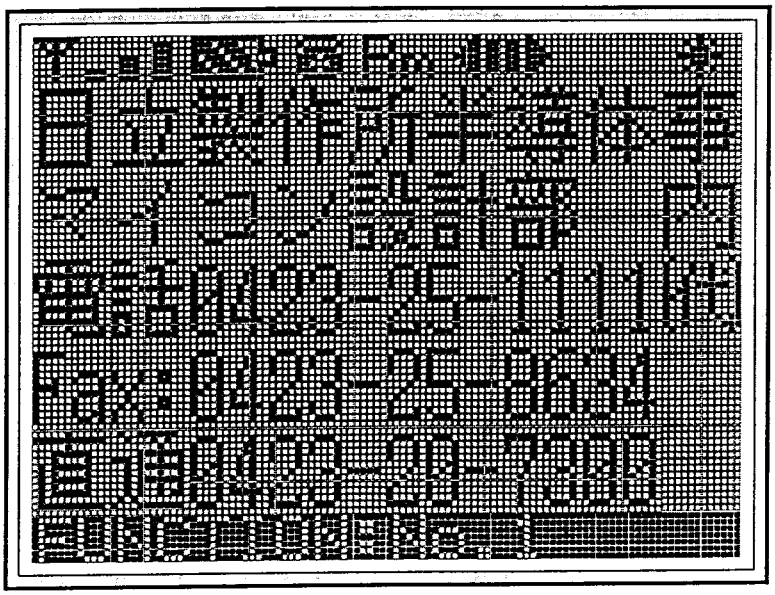
Character Code	Memory Bank 0 (RL1–10 = 0)	Memory Bank 1 (RL1–10 = 1)
"00"H to "0F"H	*CGRAM (1) to (16)*	*CGRAM (1) to (16)*
"10"H to "1F"H	CGROM (1) to (16)	*CGRAM (17) to (32)*
"20"H to "2F"H	CGROM (17) to (32)	CGROM (241) to (256)
"30"H to "3F"H	CGROM (33) to (48)	CGROM (257) to (272)
"40"H to "4F"H	CGROM (49) to (64)	CGROM (273) to (288)
"50"H to "5F"H	CGROM (65) to (80)	CGROM (289) to (304)
"60"H to "6F"H	CGROM (81) to (96)	CGROM (305) to (320)
"70"H to "7F"H	CGROM (97) to (112)	CGROM (321) to (336)
"80"H to "8F"H	CGROM (113) to (128)	*CGRAM (33) to (48)*
"90"H to "9F"H	CGROM (129) to (144)	*CGRAM (49) to (64)*
"A0"H to "AF"H	CGROM (145) to (160)	CGROM (337) to (352)
"B0"H to "BF"H	CGROM (161) to (176)	CGROM (353) to (368)
"C0"H to "CF"H	CGROM (177) to (192)	CGROM (369) to (384)
"D0"H to "DF"H	CGROM (193) to (208)	CGROM (385) to (400)
"E0"H to "EF"H	CGROM (209) to (224)	CGROM (401) to (416)
"F0"H to "FF"H	CGROM (225) to (240)	CGROM (417) to (432)

Graphics Display Function

The HD66728 has a character display mode (SPR = 0 and GR = 0) where the CGRAM or CGROM is used to display font patterns, a graphics display mode (SPR = 0 and GR = 1) where the bit pattern data is set to the CGRAM to display given patterns, and a superimposed display mode (SPR = 1) which displays both display modes combined. In the character display mode, characters can easily be provided by sending one-byte-per-character character codes to the DDRAM, but any pattern cannot be displayed. In the graphics display mode or superimposed mode, all bit pattern data to be displayed must be sent although any pattern can be displayed. The HD66728 supports these three modes which can easily be switched using the GR bit and SPR bit.

In the graphics display mode, kanji characters, special symbols, and graphics icons can be displayed. Up to 112 x 80-dot display is allowed using the CGRAM. Thus, for a 12 x 13-dot kanji font, up to a 6-line x 9-character kanji display, and for a 14 x 15-dot kanji font, up to a 6-line x 8-character kanji display, and for a 16 x 16-dot kanji font, up to a 5-line x 6-character kanji display are allowed.

i) 12 x 13-dot kanji display example
(6-line x 9-character display)



ii) 112 x 80-dot game display example

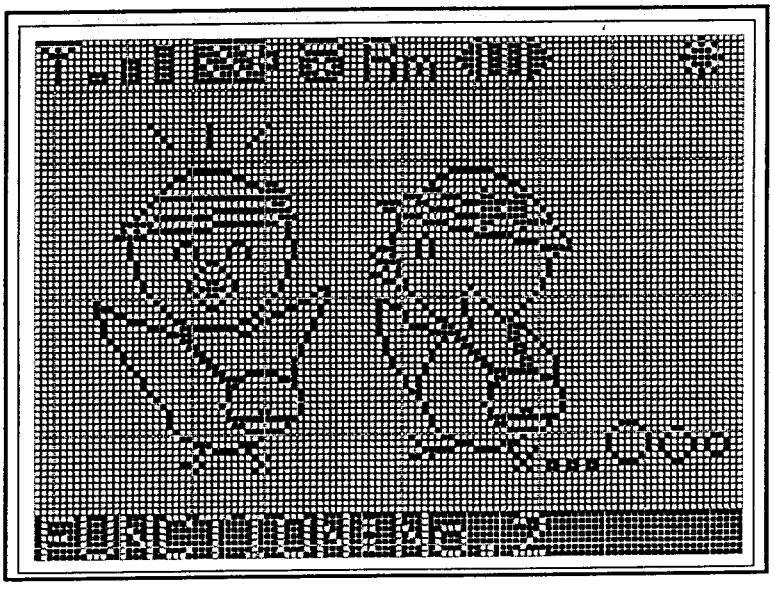


Figure 52 Display Example in Graphics Display Mode

Superimposed Display Function

The HD66728 has a superimposed display mode (SPR = 1) which displays two modes combined: the character display mode where the character code in the CGROM is used to display font patterns, and the graphics display mode where the bit pattern data is set to the CGRAM to display given patterns. The superimposed mode can be supplied with an easy character display mode and various graphics display modes, enabling a flexible high-quality display. For example, this mode is available to insert graphics such as maps or facial images in an address book which otherwise only uses characters.

When characters are displayed in this mode, user fonts cannot be displayed by using the CGRAM. The CGRAM is used as the RAM for the graphics display.

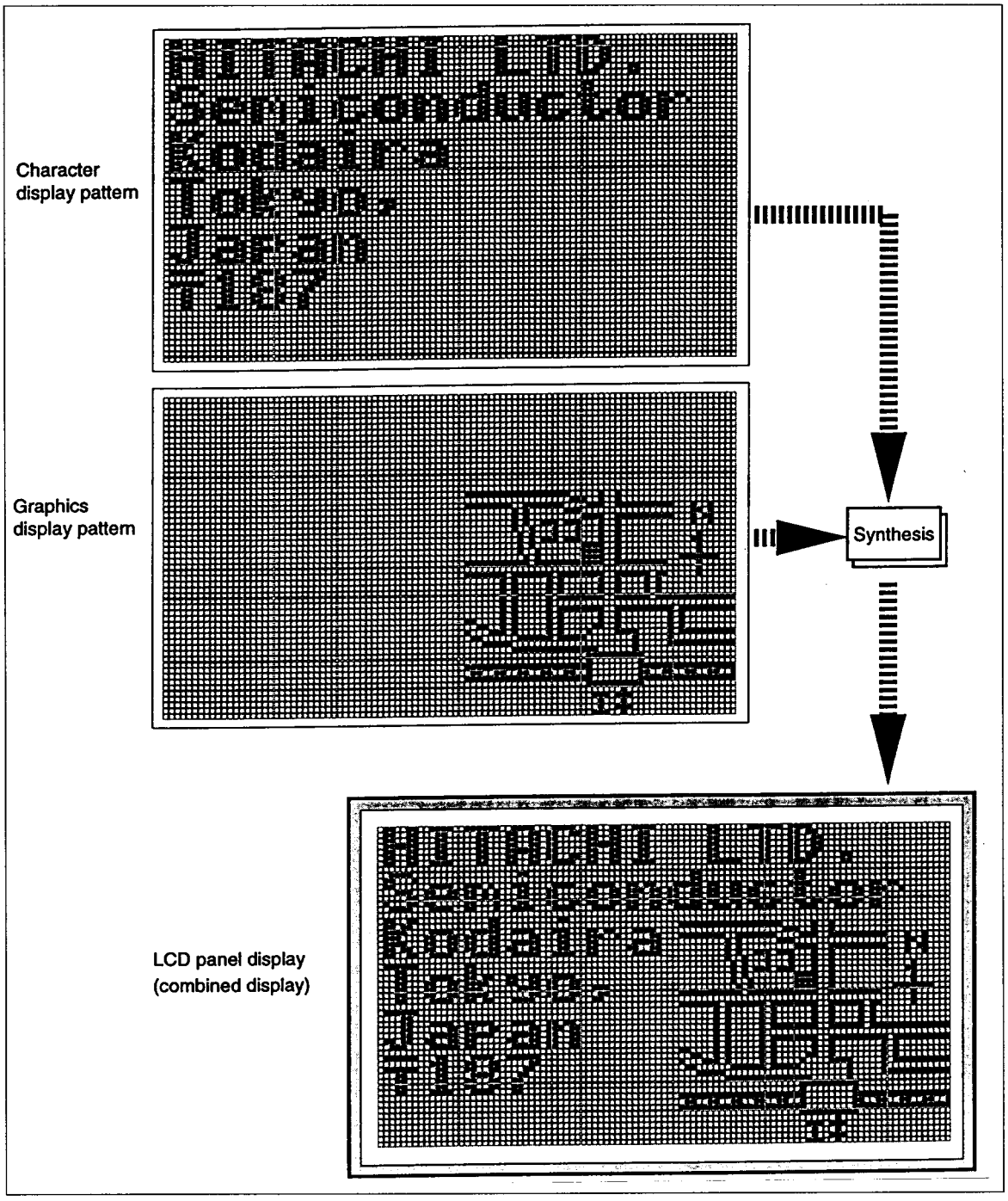


Figure 53 Example of Superimposed Display

Vertical Smooth Scroll Display

The HD66728 can scroll character and graphics display vertically in units of raster-rows. This is achieved by writing display data into a one-line area that is not being used for display. In other words, one line can be used to achieve continuous smooth vertical scroll even in a 9-line or less display. Here, after the 10th line is displayed, the first line is displayed again. When the 10th line is fully displayed, all one-line display data must be rewritten immediately after scrolling because there is no non-displayed area. Additionally, when display areas of a graphics icon such as a pictogram or a menu bar are partially fixed-displayed, the remaining areas can be displayed. For details, see the Partial Smooth Scroll Display Function section.

Specifically, this function is controlled by incrementing or decrementing the value in the display-start line bits (SL2 to SL0) and display-start raster-row bits (SN3 to SN0) by 1. For example, to smoothly scroll up, first set line bits SN3 to SN0 to 0000, and increment SL2 to SL0 by 1 from 000 to 111 to scroll seven raster-rows. Then increment line bits SN3 to SN0 to 0001, and again increment SL2 to SL0 by 1 from 000 to 111. If the vertical double-height display is at the top of the line, scrolling is done by each two raster-row.

When the response speed of the liquid crystal is low or when high-speed scrolling is needed, two- to four-raster-row scrolling is recommended.

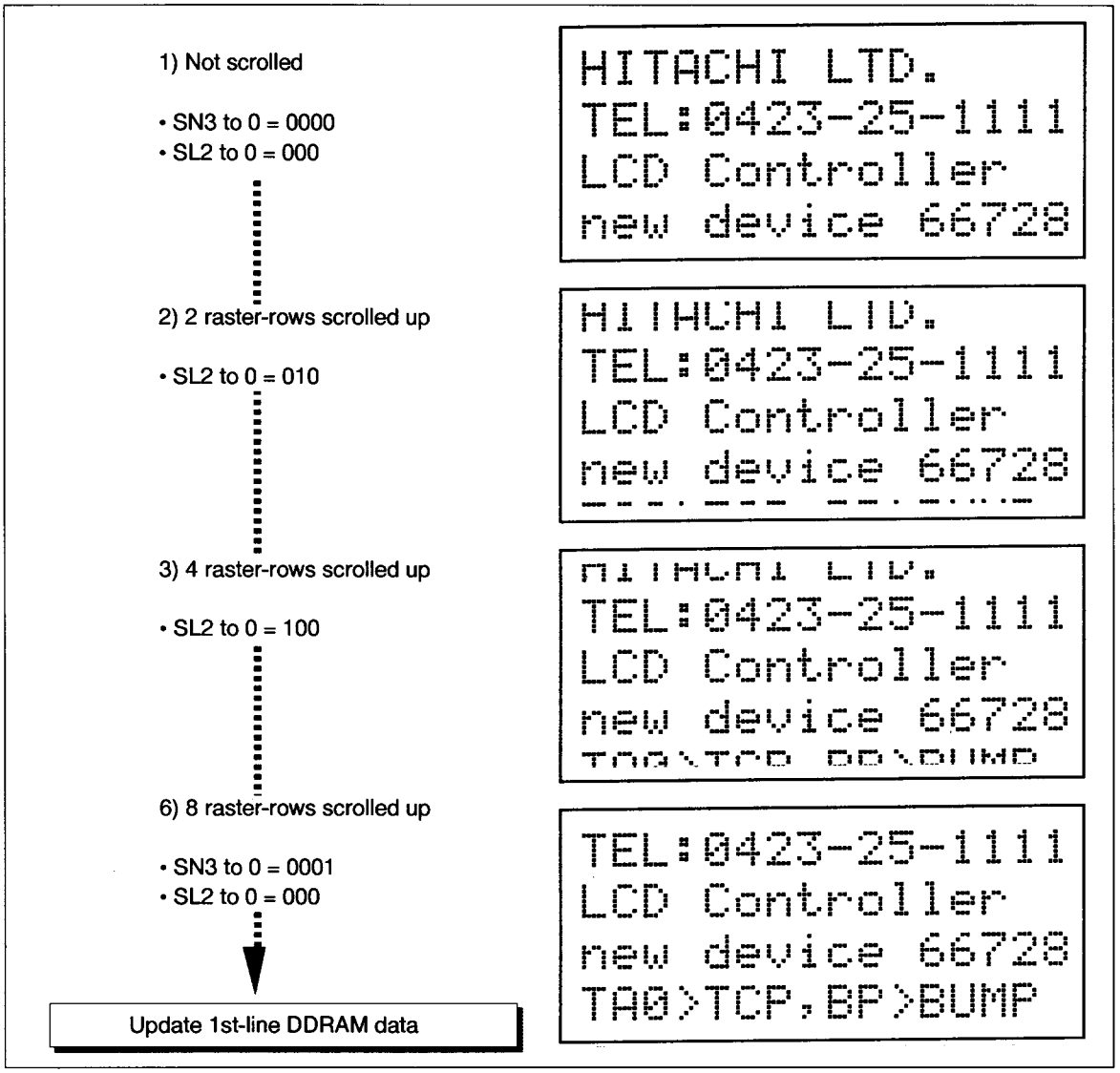


Figure 54 Vertical Smooth Scroll (4-line Display)

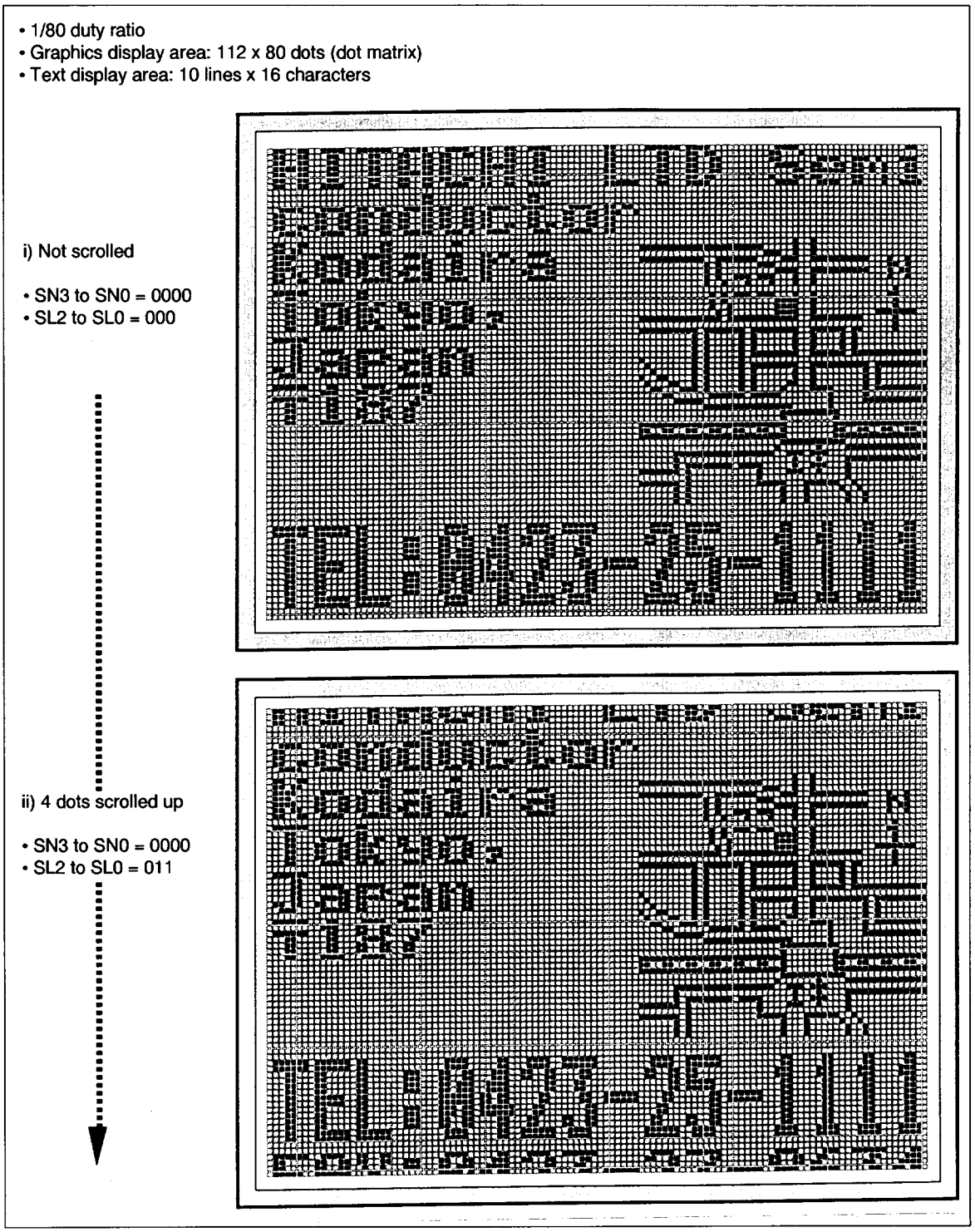
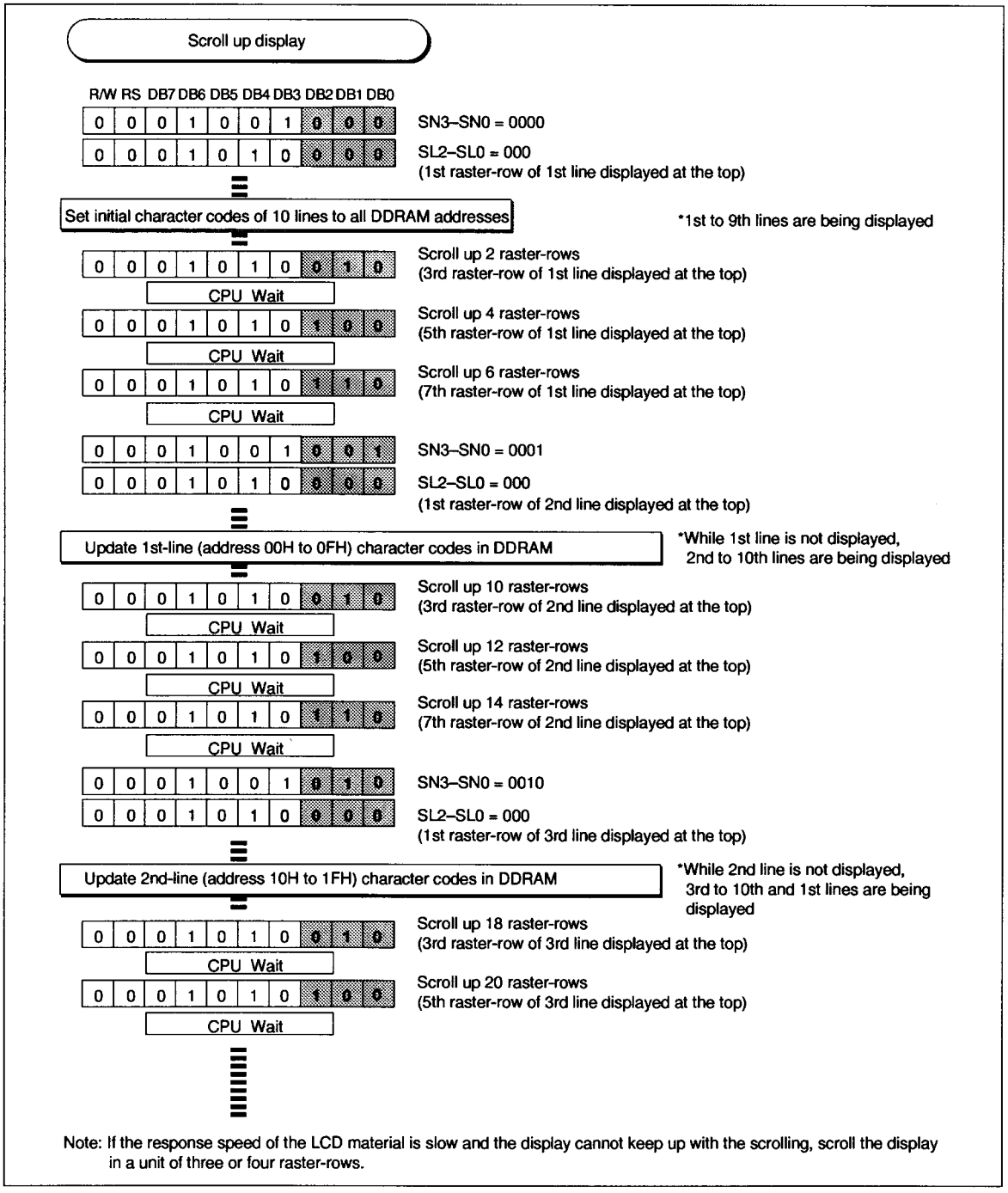


Figure 55 Example of Vertical Scroll in Superimposed Mode

Setting Instructions (Character Display Mode: GR = 0, 9-line Display: NL2-0 = 1000)



Note: If the response speed of the LCD material is slow and the display cannot keep up with the scrolling, scroll the display in a unit of three or four raster-rows.

Figure 56 Setting Instructions for Vertical Smooth Scroll (Character Display Mode)

Setting Instructions (Graphics Display Mode: GR = 1, 10-line Display: NL3-0 = 1001)

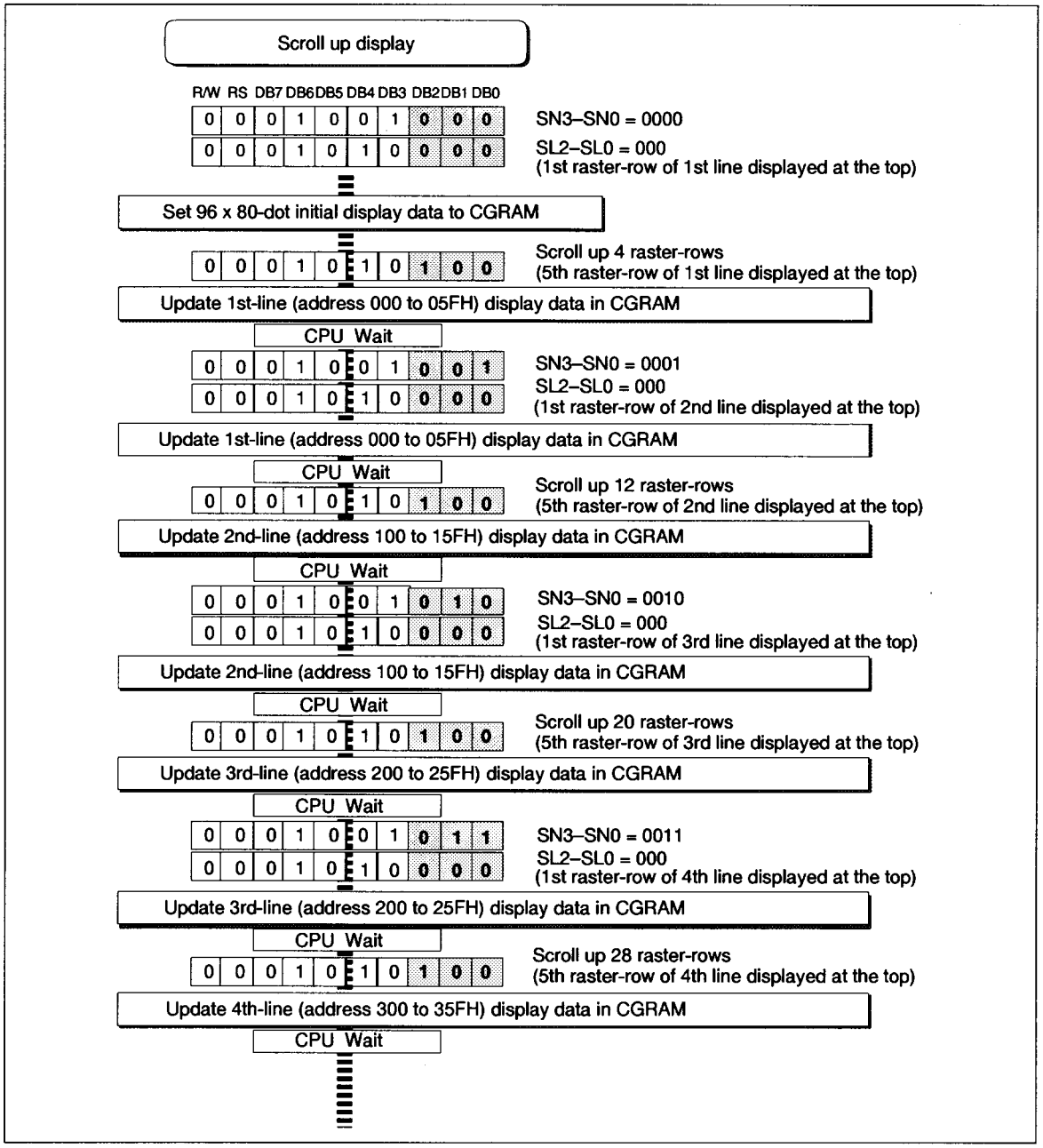


Figure 57 Setting Instructions for Vertical Smooth Scroll (Graphics Display Mode)

Partial Smooth Scroll Display Function

The HD66728 can partially fixed-display the areas of a graphics icon, such as a pictogram or a menu bar, and perform vertical smooth scrolling of the remaining bit-map areas. Since the PS1 to PS0 bits do not perform smooth scrolling of the upper first to third display lines but does fixed-display, pictograms can be placed. When CN1 to CN0 bits are set to 10, the first line is displayed at the bottom edge of the LCD screen, and the menu bar can be fixed-displayed at the bottom. This function can largely control the bit-map rewrite frequencies and reduce software loads.

Table 36 Bit Setting and Display Lines

Bit Setting	COM Position	CN1–0 = 00					CN1–0 = 10				
		SN3–0 = 0000	SN3–0 = 0001	SN3–0 = 0010	SN3–0 = 0011	SN3–0 = 0011	SN3–0 = 0000	SN3–0 = 0001	SN3–0 = 0010	SN3–0 = 0011	SN3–0 = 0100
PS1–0 = 00	COM1	1st line	2nd line	3rd line	4th line	5th line	2nd line	3rd line	4th line	5th line	6th line
		2nd line	3rd line	4th line	5th line	6th line	3rd line	4th line	5th line	6th line	7th line
		3rd line	4th line	5th line	6th line	7th line	4th line	5th line	6th line	7th line	8th line
		4th line	5th line	6th line	7th line	8th line	5th line	6th line	7th line	8th line	9th line
		5th line	6th line	7th line	8th line	9th line	6th line	7th line	8th line	9th line	10th line
		6th line	7th line	8th line	9th line	10th line	7th line	8th line	9th line	10th line	1st line
		7th line	8th line	9th line	10th line	1st line	8th line	9th line	10th line	1st line	2nd line
		8th line	9th line	10th line	1st line	2nd line	9th line	10th line	1st line	2nd line	3rd line
		9th line	10th line	1st line	2nd line	3rd line	10th line	1st line	2nd line	3rd line	4th line
	COM80	10th line	1st line	2nd line	3rd line	4th line	1st line	2nd line	3rd line	4th line	5th line
PS1–0 = 01	COM1	1st line	1st line	1st line	1st line	1st line	1st line	2nd line	3rd line	4th line	5th line
		1st line	2nd line	3rd line	4th line	5th line	2nd line	3rd line	4th line	5th line	6th line
		2nd line	3rd line	4th line	5th line	6th line	3rd line	4th line	5th line	6th line	7th line
		3rd line	4th line	5th line	6th line	7th line	4th line	5th line	6th line	7th line	8th line
		4th line	5th line	6th line	7th line	8th line	5th line	6th line	7th line	8th line	9th line
		5th line	6th line	7th line	8th line	9th line	6th line	7th line	8th line	9th line	10th line
		6th line	7th line	8th line	9th line	10th line	7th line	8th line	9th line	10th line	2nd line
		7th line	8th line	9th line	10th line	2nd line	8th line	9th line	10th line	2nd line	3rd line
		8th line	9th line	10th line	2nd line	3rd line	9th line	10th line	2nd line	3rd line	4th line
	COM80	9th line	10th line	2nd line	3rd line	4th line	1st line	1st line	1st line	1st line	1st line
PS1–0 = 10	COM1	1st line	1st line	1st line	1st line	1st line	2nd line	2nd line	2nd line	2nd line	2nd line
		2nd line	2nd line	2nd line	2nd line	2nd line	1st line	2nd line	3rd line	4th line	5th line
		1st line	2nd line	3rd line	4th line	5th line	2nd line	3rd line	4th line	5th line	6th line
		2nd line	3rd line	4th line	5th line	6th line	3rd line	4th line	5th line	6th line	7th line
		3rd line	4th line	5th line	6th line	7th line	4th line	5th line	6th line	7th line	8th line
		4th line	5th line	6th line	7th line	8th line	5th line	6th line	7th line	8th line	9th line
		5th line	6th line	7th line	8th line	9th line	6th line	7th line	8th line	9th line	10th line
		6th line	7th line	8th line	9th line	10th line	7th line	8th line	9th line	10th line	3rd line
		7th line	8th line	9th line	10th line	3rd line	8th line	9th line	10th line	3rd line	4th line
	COM80	8th line	9th line	10th line	3rd line	4th line	1st line	1st line	1st line	1st line	1st line
PS1–0 = 11	COM1	1st line	1st line	1st line	1st line	1st line	2nd line	2nd line	2nd line	2nd line	2nd line
		2nd line	2nd line	2nd line	2nd line	2nd line	3rd line	3rd line	3rd line	3rd line	3rd line
		3rd line	3rd line	3rd line	3rd line	3rd line	1st line	2nd line	3rd line	4th line	5th line
		1st line	2nd line	3rd line	4th line	5th line	2nd line	3rd line	4th line	5th line	6th line
		2nd line	3rd line	4th line	5th line	6th line	3rd line	4th line	5th line	6th line	7th line
		3rd line	4th line	5th line	6th line	7th line	4th line	5th line	6th line	7th line	8th line
		4th line	5th line	6th line	7th line	8th line	5th line	6th line	7th line	8th line	9th line
		5th line	6th line	7th line	8th line	9th line	6th line	7th line	8th line	9th line	10th line
		6th line	7th line	8th line	9th line	10th line	7th line	8th line	9th line	10th line	4th line
	COM80	7th line	8th line	9th line	10th line	4th line	1st line	1st line	1st line	1st line	1st line

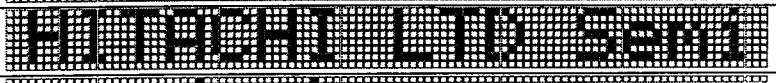
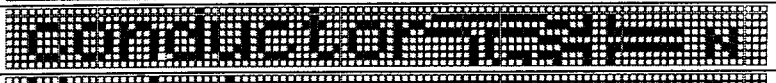
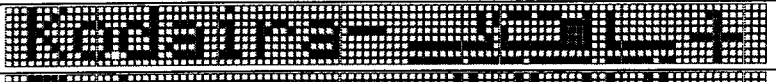
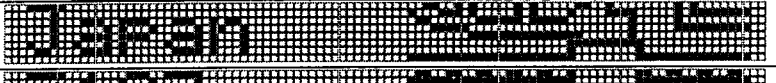
Notes: 1. The shadow lines above are fixed-displayed. They do not depend on the setting values of the SN3–0 or SL3–0 bits.

2. The SN3–0 and SL3–0 bits specify the next first scroll display line of the fixed-displayed lines.

3. When the drive duty ratio is nine lines (1/72 duty ratio) or less and CN1–0 is 10, the first line shifts to the last displayed line.

Partial Smooth Scroll Display Examples

Table 37 Data Setting to the CGRAMPartial Smooth Scroll Display Examples

CGRAM Address	CGRAM Data
000 to 06F	
080 to 0EF	
100 to 16F	
180 to 1EF	
200 to 26F	
280 to 2EF	
300 to 36F	
380 to 3EF	
400 to 46F	
480 to 4EF	

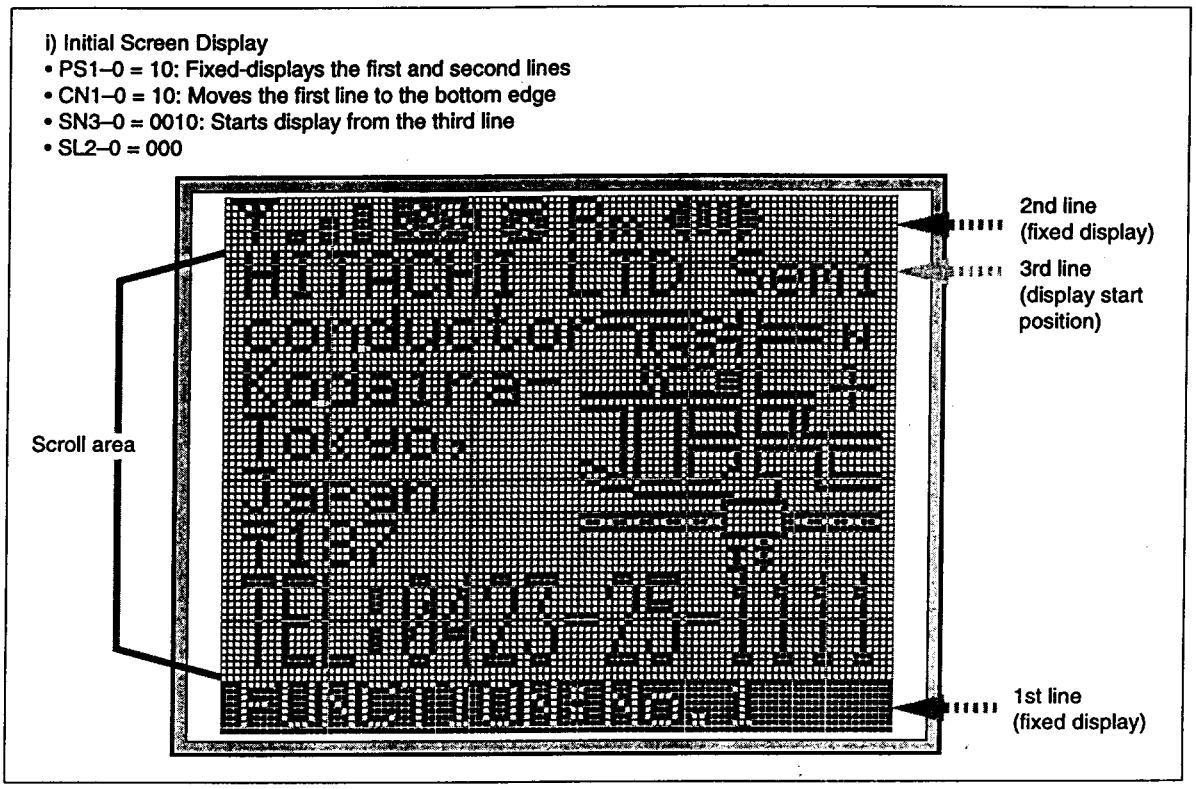


Figure 58 Example of Initial Screen in the Partial Smooth Scroll Mode

ii) 4-dot Partial Scroll Up
- PS1–0 = 10: Fixed-displays the first and second lines
- CN1–0 = 10: Moves the first line to the bottom edge
- SN3–0 = 0010: Starts display from the third line
- SL2–0 = 100: Shifts up by 4 dots

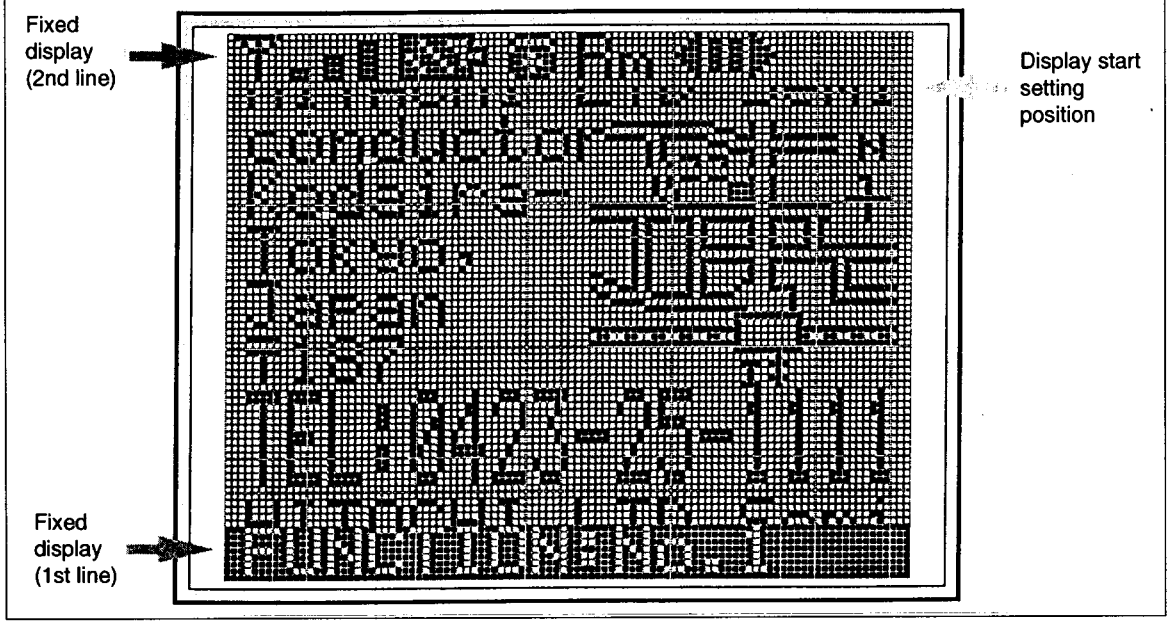


Figure 59 Example of Display Screen in the Partial Smooth Scroll Mode (1)

iii) 8-dot Partial Scroll Up
- PS1–0 = 10: Fixed-displays the first and second lines
- CN1–0 = 10: Moves the first line to the bottom edge
- SN3–0 = 0011: Starts display from the fourth line
- SL2–0 = 000

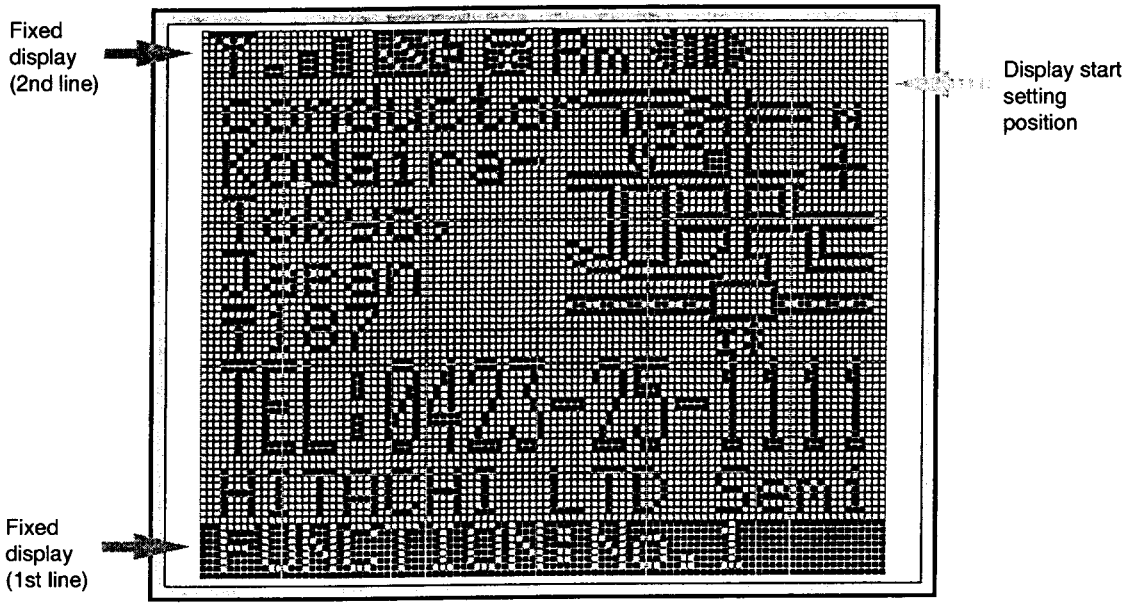


Figure 60 Example of Display Screen in the Partial Smooth Scroll Mode (2)

Double-height Display

The HD66728 can double the height of any desired line from the first to 10th lines. A line can be selected by the DL1 to DL10 bits as listed in table 38. All the font characters or graphics display patterns stored in the CGROM and CGRAM can be doubled in height, allowing easy recognition. Note that there should be no space between the lines for double-height display (figure 61).

In vertical smooth scrolling, when the display-start setting line is displaying at double height, scrolling can be done by each two-line (dot).

Table 38 Double-height Display Specifications

Bit Setting	Display Position
DL1 = 1	1st line: double-height
DL2 = 1	2nd line: double-height
DL3 = 1	3rd line: double-height
DL4 = 1	4th line: double-height
DL5 = 1	5th line: double-height
DL6 = 1	6th line: double-height
DL7 = 1	7th line: double-height
DL8 = 1	8th line: double-height
DL9 = 1	9th line: double-height
DL10 = 1	10th line: double-height

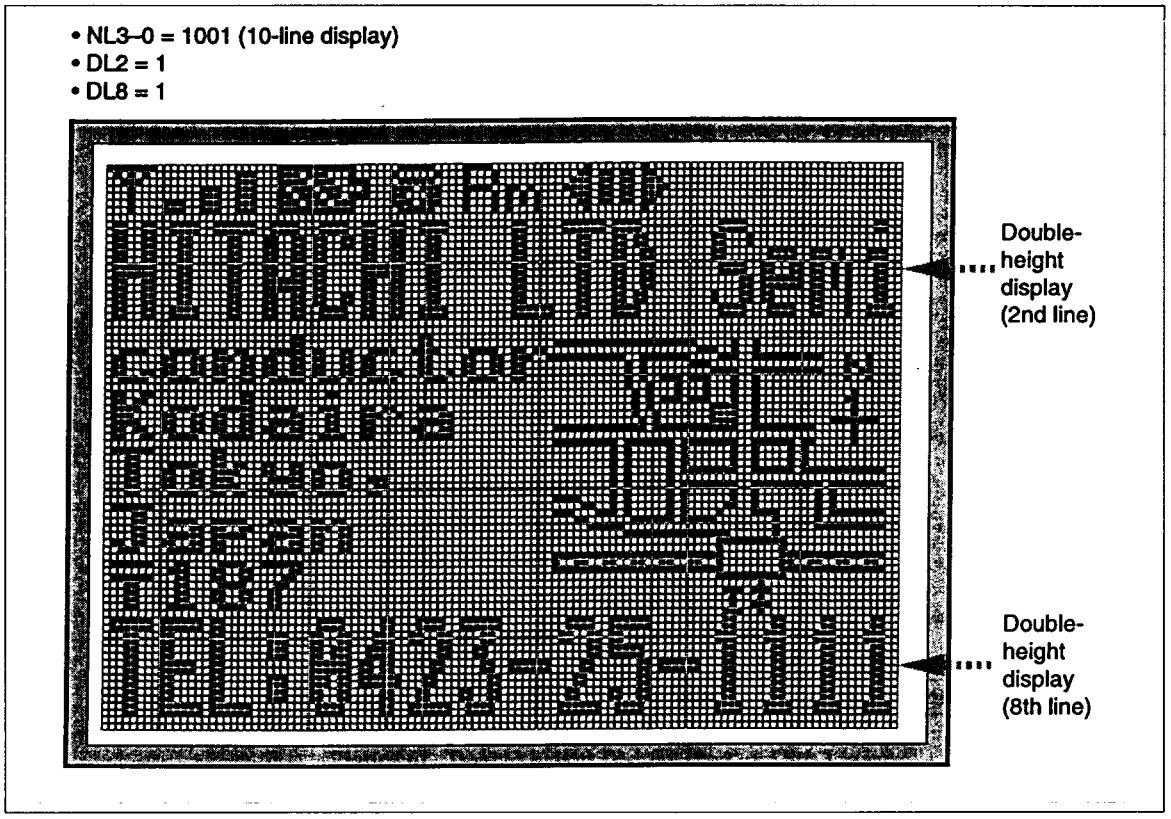


Figure 61 Double-height Display (2nd and 8th Lines)

Reversed Display Function

The HD66728 can display character/graphics display sections by black-and-white reversal. Black-and-white reversal can be easily displayed when REV is set to 1.

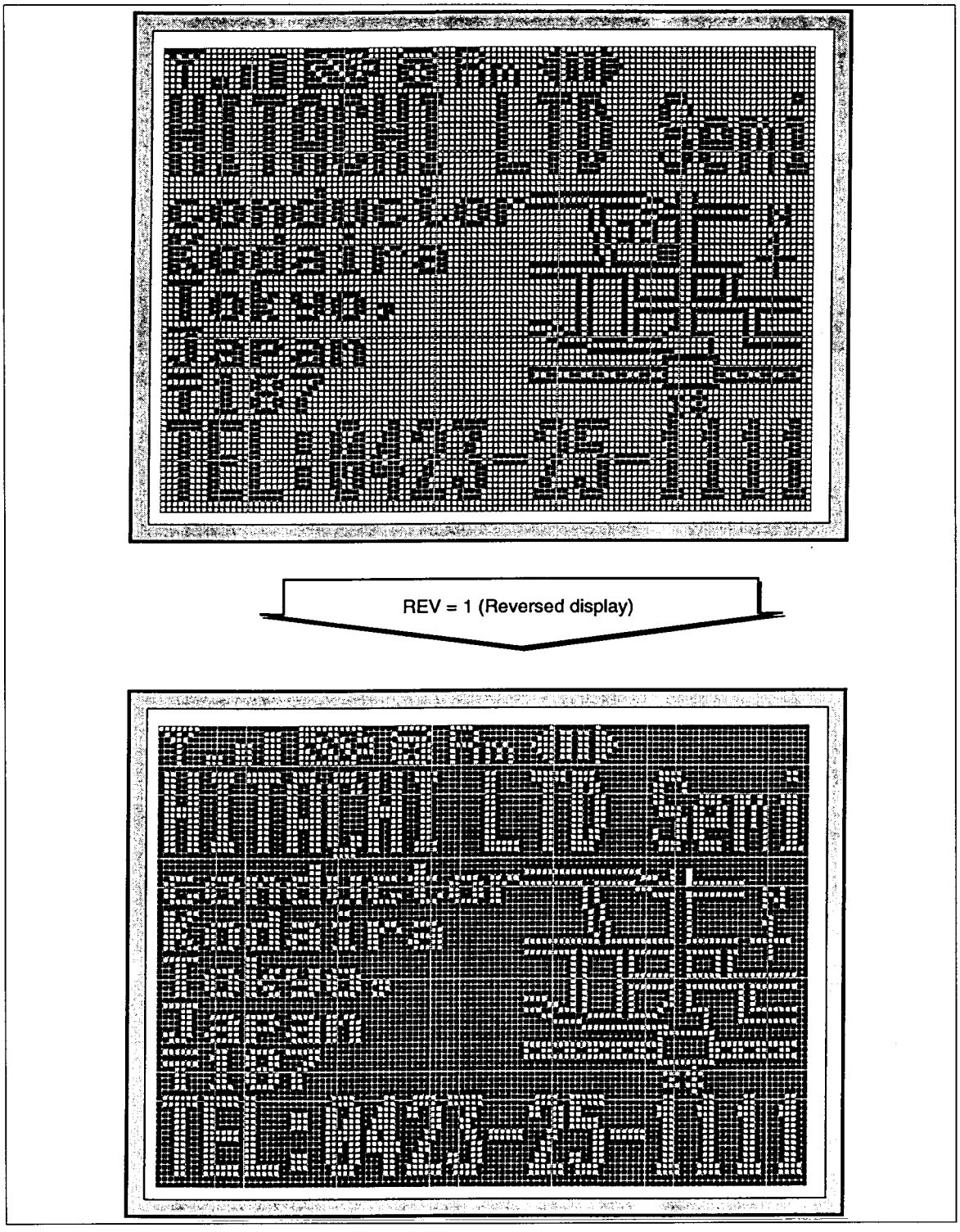


Figure 62 Reversed Display

Line-cursor Display

The HD66728 can assign a cursor attribute to an entire line corresponding to lower eight bits of the address counter value by setting the LC bit to 1. One of three line-cursor modes can be selected: a black-and-white reversed cursor (B/W = 1), an underline cursor (C = 1), and a blink cursor (B = 1). The cycle for a blink cursor is 32 frames. These line-cursors are suitable for highlighting an index and/or marker, or for indicating an item in a menu with a cursor or an underline.

However, the black-and-white reversed display described above does not perform black-and-white blink. When SCE = 0, the CGRAM area which is output from the ISEG1 to ISEG6 pins does not produce line-cursor display.

Table 39 Address Counter Value and Line Cursor

Address Counter Value (AC)	Selected Line for Line Cursor
00H to 0FH	Entire 1st line (16 characters)
10H to 1FH	Entire 2nd line (16 characters)
20H to 2FH	Entire 3rd line (16 characters)
30H to 3FH	Entire 4th line (16 characters)
40H to 4FH	Entire 5th line (16 characters)
50H to 5FH	Entire 6th line (16 characters)
60H to 6FH	Entire 7th line (16 characters)
70H to 7FH	Entire 8th line (16 characters)
80H to 8FH	Entire 9th line (16 characters)
90H to 9FH	Entire 10th line (16 characters)

Black-white Reversed Cursor (LC = 1, B/W = 1)

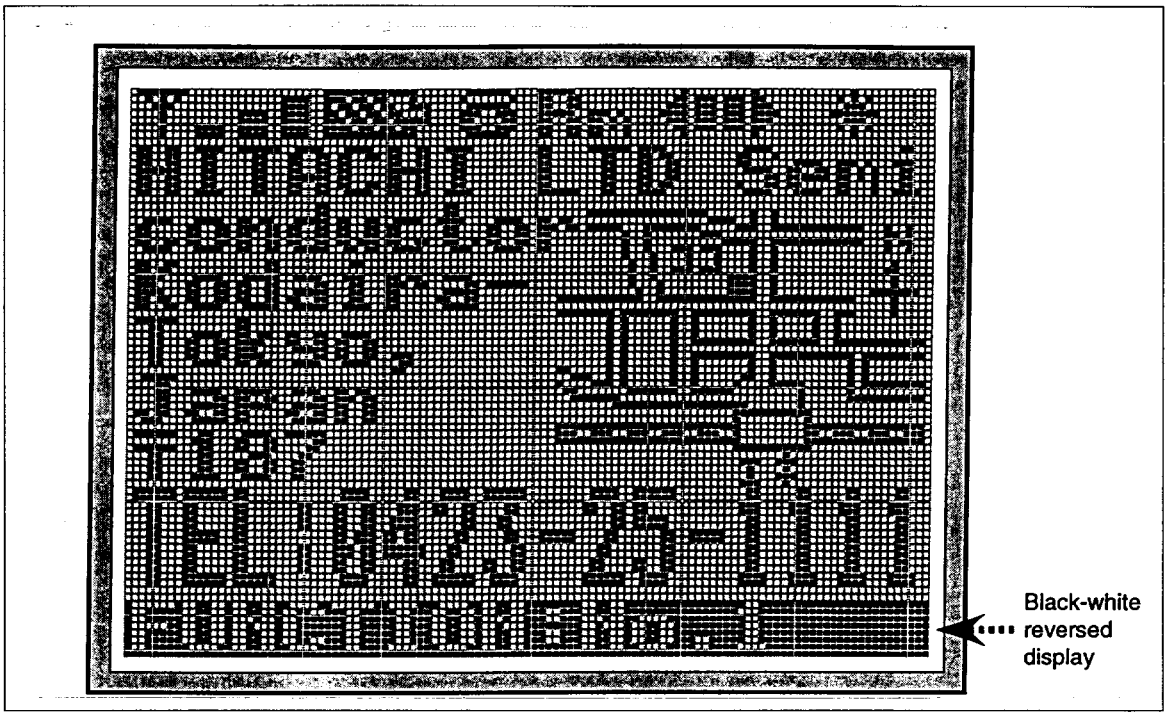


Figure 63 Black-white Reversed Cursor

Underline Cursor (LC = 1, C = 1)

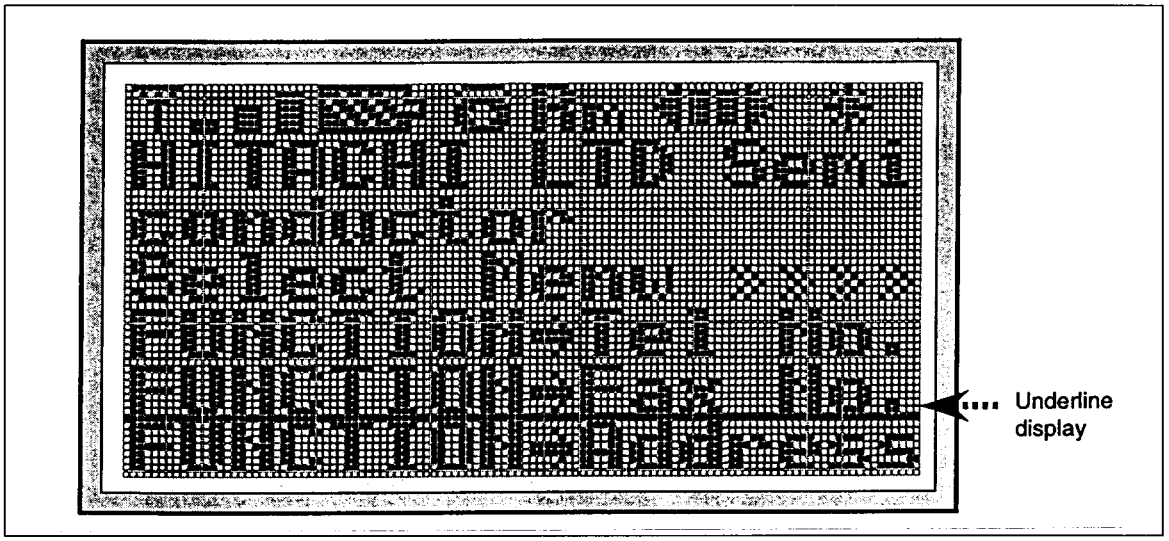


Figure 64 Underline Cursor

Blink Cursor (LC = 1, B = 1)

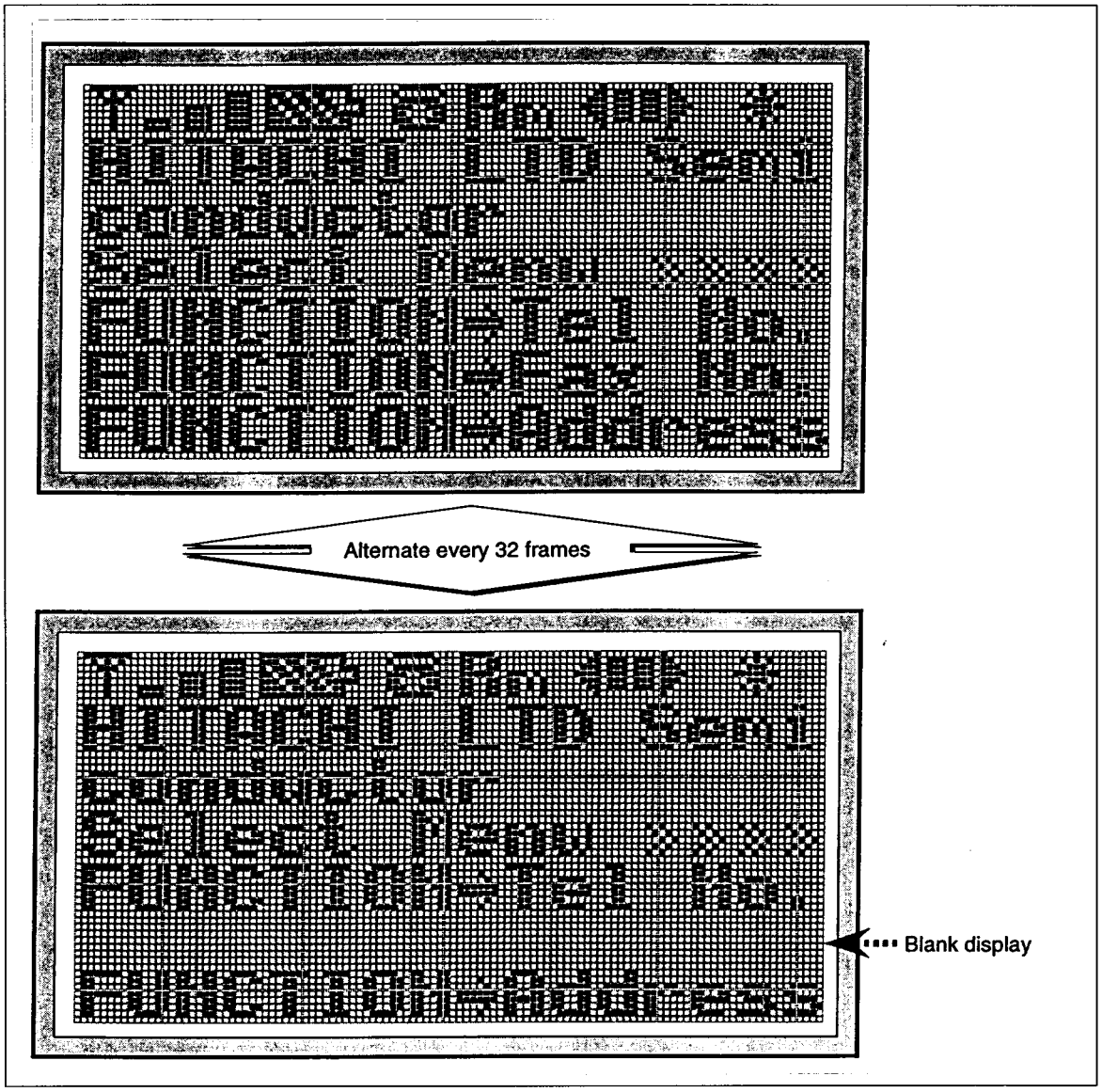


Figure 65 Blink Cursor

Partial-display-on Function

The HD66728 can program the liquid crystal display drive duty ratio setting (NL3-0 bits), liquid crystal display drive bias value selection (BS2-0 bits), boost output level selection (BT1/0 bit) and contrast adjustment (CT5-0 bits). For example, in the 10-line display mode (1/80 duty ratio), the HD66728 can selectively drive only the center of the screen or only the top or bottom of the screen by combining these register functions and the centering display (CN1–0 bit) function. This is called partial-display-on. Lowering the liquid crystal display drive duty ratio as required saves the liquid crystal display drive voltage, thus reducing internal current consumption. This is suitable for four-line display of a calendar or time, or the display of only graphics icons (pictograms) at the top or bottom of the screen, which needs to be continuous in the system standby state with minimal current consumption. Here, the non-displayed lines are constantly driven by the unselected level voltage, thus turning off the LCD for the lines.

In general, lowering the liquid crystal display drive duty ratio decreases the optimum liquid crystal display drive voltage and liquid crystal display drive bias value. This reduces output multiplying factors in the booster and greatly controls consumption current.

Table 40 Partial-display-on Function (10-line Display)

Item	Normal 10-line Display	Partial-on Display (Limited 4-line Display)	
LCD screen	10th line displayed	Only four lines on the center of the screen (from the 3rd to 6th lines)	Only four lines at the top and bottom of the screen (from the 1st to 3rd and 10th lines)
LCD drive position shift	Not necessary (CN1–0 = 00)	Necessary (CN1–0 = 01)	Necessary (CN1–0 = 01)
LCD drive duty ratio	1/80 (NL3–0 = 1001)	1/32 (NL3–0 = 0011)	1/32 (NL3–0 = 0011)
LCD drive bias value (optimum)	1/10 (BS2-0 = 000)	1/6 (BS2-0 = 101)	1/6 (BS2-0 = 101)
LCD drive voltage*	12 V to 15 V (adjustable using CT5–0)	6 V to 8 V (adjustable using CT5–0)	6 V to 8 V (adjustable using CT5–0)
Boosting output multiplying factor	Five times (BT1–0 = 10)	Triple (BT1–0 = 00)	Triple (BT1–0 = 00)
Frame frequency (fosc = 90 kHz)	70 Hz	88 Hz	88 Hz

Note: The LCD drive voltage depends on the LCD materials which are actually used. Since the LCD drive voltage is high when the LCD drive duty ratio is high, a low duty ratio is suitable for low-power consumption.

- **1/32-duty Drive at the Top and Bottom of the Screen**

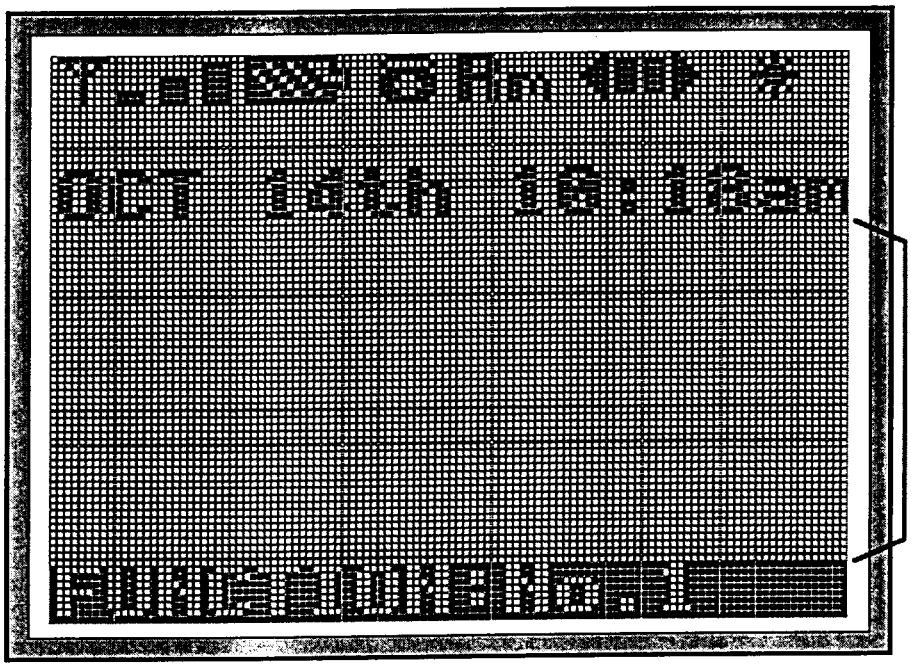


Figure 66 Partial-on Display (Date and Time Indicated) (1)

• 1/32-duty Drive on the Center of the Screen

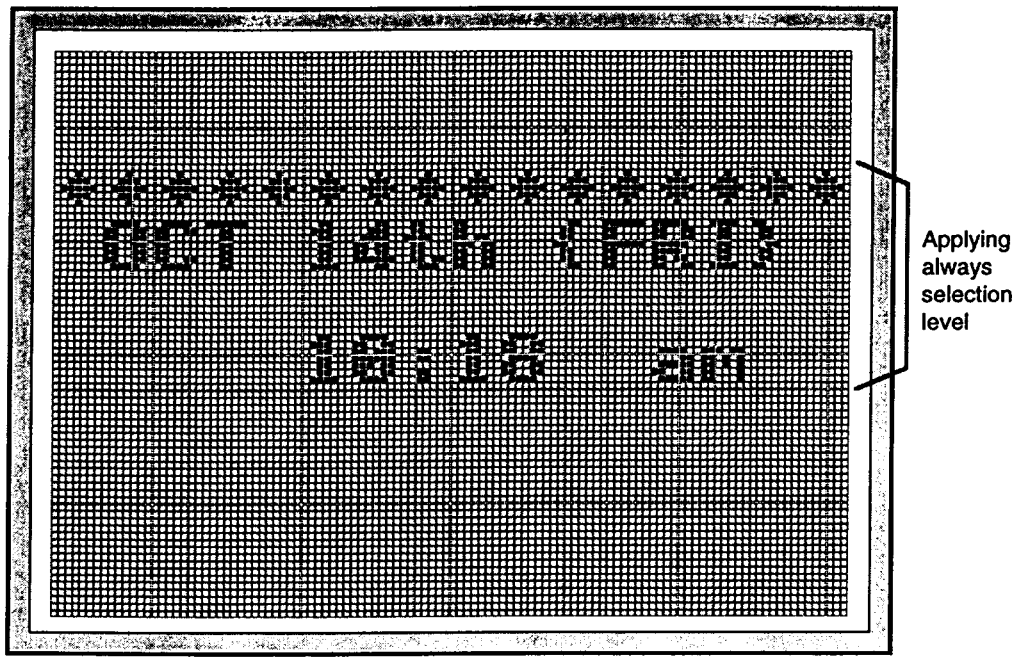


Figure 67 Partial-on Display (Date and Time Indicated) (2)

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66728 in the sleep mode, where the device stops all internal display operations except for key scan operations, thus reducing current consumption. Specifically, LCD drive is completely halted. Here, all the SEG (SEG1 to SEG112) and COM (COM1 to COM80) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

The key scan circuit operates normally in the sleep mode, thus allowing normal key scan and key scan interrupt generation. For details, see the Key Scan Control section and Key Scan Interrupt (Wake-up Function) section.

Table 41 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)	Key Standby Mode (KSB = 1)
LCD control	Turned off	Turned off	Normally turned on
R-C oscillation circuit	Operates normally	Halted	Normally turned on
Key scan circuit	Can operate normally	Halted but IRQ* can be generated	

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66728 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, character and segment displays, which are controlled by the multiplexing drive method, are completely halted. Here, all the SEG (SEG1 to SEG112) and COM (COM1 to COM80) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction and the key scan interrupt generation enable instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

Although key scan is halted in the standby mode, the HD66728 can detect key inputs, thus generating key scan interrupt (IRQ*). This means, the system can be activated from a completely inactive state. For details, see the Key Scan Interrupt (Wake-up Function) section.

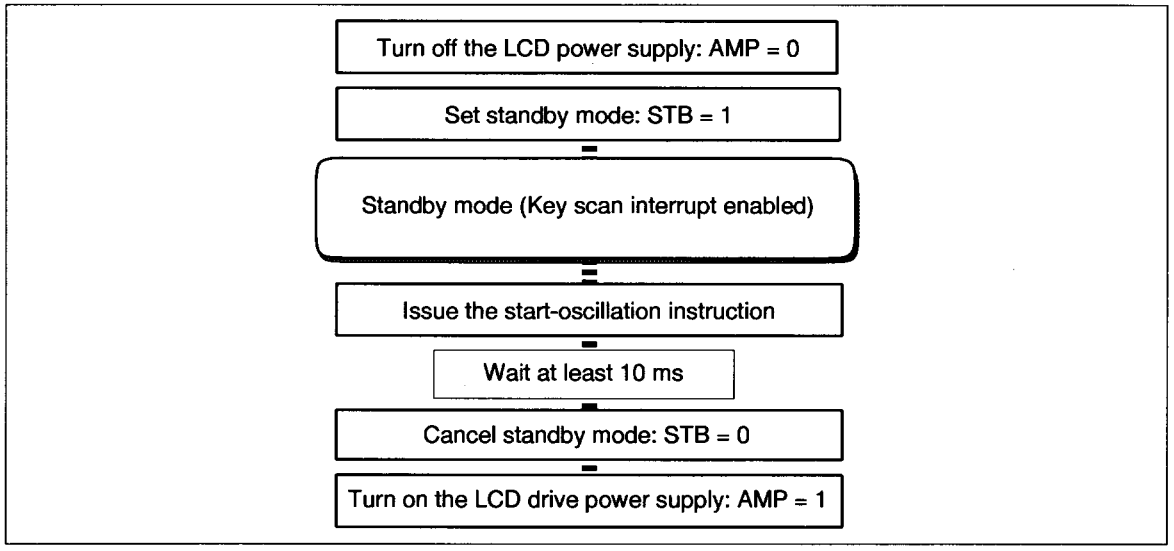


Figure 68 Procedure for Setting and Canceling Standby Mode

Key Standby Mode

When the key standby mode (KSB bit = 1) is set, only key-scan operations are selectively stopped. In this case, however, the display operation, including the internal CR oscillation circuit operation, continues as usual. Since noise generation can be suppressed by stopping unnecessary key-scan operations, the receiving sensitivity for such a wireless system can be improved.

In this case, although key-scan operations are stopped during the key standby mode, a key scan interrupt (IRQ*) can be generated by detecting the key being pressed, as can be done during the standby mode described above. For details, refer to the Key Scan Interrupt (Wake-up Function) section.

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1, 2
Power supply voltage (2)	V_{LCD} – GND	V	–0.3 to +16.0	1, 3
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	–40 to +85	1, 4
Storage temperature	Tstg	°C	–55 to +110	1, 5

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.
2. VCC > GND must be maintained.
3. VLCD > GND must be maintained.
4. For bare die and wafer products, specified up to 85°C.
5. This temperature specifications apply to the TCP package.

DC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[1])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V		2, 3
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 1.8 to 2.7 V	2, 3
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V	2, 3
Output high voltage (1) (SDA, DB0-7 pins)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	2, 4
Output low voltage (1) (SDA, DB0-7 pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 1.8 to 2.7 V, I_{OL} = 0.1 mA	2
Output low voltage (1) (SDA, DB0-7 pins)	V_{OL1}	—	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V, I_{OL} = 0.1 mA	2
Output high voltage (2) (KST0-7, IRQ* pins)	V_{OH2}	0.7 V_{CC}	—	—	V	$-I_{OH}$ = 0.5 µA, V_{CC} = 3 V	2
Output low voltage (2) (KST0-7, IRQ* pins)	V_{OL2}	—	—	0.2 V_{CC}	V	I_{OL} = 0.1 mA	2
Output high voltage (3) (PORT0-2 pins)	V_{OH3}	0.75 V_{CC}	—	—	V	$-I_{OH}$ = 0.1mA	2
Output low voltage (3) (PORT0-2 pins)	V_{OL3}	—	—	0.2 V_{CC}	V	I_{OL} = 0.1mA	2
Driver ON resistance (COM pins)	R_{COM}	—	3	20	kΩ	±Id = 0.05 mA, V_{LCD} = 10 V	5
Driver ON resistance (SEG pins)	R_{SEG}	—	3	30	kΩ	±Id = 0.05 mA, V_{LCD} = 10 V	5
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	6
Pull-up MOS current (KIN0-7, DB0-7, SDA pins)	$-I_p$	1	10	40	µA	V_{CC} = 3 V, Vin = 0 V	2
Current consumption during normal operation (V_{CC}–GND)	I_{OP}	—	32 (T.B.D.)	55 (T.B.D.)	µA	R-C oscillation, V_{CC} = 3 V, Ta = 25 °C, f_{OSC} = 80 kHz (1/72 duty)	7, 8
Current consumption during sleep mode (V_{CC}–GND)	I_{SL}	—	25 (T.B.D.)	—	µA	R-C oscillation, V_{CC} = 3 V, Ta = 25 °C, f_{OSC} = 80 kHz (1/72 duty)	7, 8
Current consumption during standby mode (V_{CC}–GND)	I_{ST}	—	0.1	5	µA	V_{CC} = 3 V, Ta = 25°C	7, 8
LCD drive power supply current (V_{LCD}–GND)	I_{LCD}	—	18 (T.B.D.)	35 (T.B.D.)	µA	V_{LCD} – GND = 5.5 V, Ta = 25 °C, f_{OSC} = 80 kHz, 1/9.5 bias	8
LCD drive voltage (V_{LCD} – GND)	V_{LCD}	4.5	—	15	V		9

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Triple-boost output voltage (VLOUT pin)	V_{UP3}	8.5	8.9	9.0	V	V_{CC} = Vci = 3.0 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 80 kHz, Ta = 25°C	12
Quadruple-boost output voltage (VLOUT pin)	V_{UP4}	11.5 (T.B.D.)	11.8 (T.B.D.)	12.0	V	V_{CC} = Vci = 3.0 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 80 kHz, Ta = 25°C	12
Five-times-boost output voltage (VLOUT pin)	V_{UP5}	14.5 (T.B.D.)	14.8 (T.B.D.)	15.0	V	V_{CC} = Vci = 3.0 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 80 kHz, Ta = 25°C	12
Input voltage	V_{Ci}	1.0	—	4.0	V	Quadruple boost	12
	V_{Ci}	1.0	—	3.2	V	Five-times boost	12

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	15	32	100	kHz		10
External clock duty ratio	Duty	45	50	55	%		10
External clock rise time	trcp	—	—	0.2	µs		10
External clock fall time	tfcp	—	—	0.2	µs		10
R-C oscillation clock	f_{osc}	64 (T.B.D.)	80 (T.B.D.)	96 (T.B.D.)	kHz	Rf = 220 kΩ, V_{CC} = 3 V	11

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	500 (T.B.D.)	—	—	ns	Figure 75
	Read	t_{CYCE}	800 (T.B.D.)	—	—		
Enable high-level pulse width	Write	PW_{EH}	120 (T.B.D.)	—	—	ns	Figure 75
	Read	PW_{EH}	350 (T.B.D.)	—	—		
Enable low-level pulse width	Write	PW_{EL}	300 (T.B.D.)	—	—	ns	Figure 75
	Read	PW_{EL}	300 (T.B.D.)	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 75
Setup time (RS, R/W to E, CS*)		t_{ASE}	60	—	—	ns	Figure 75
Address hold time		t_{AHE}	20	—	—	ns	Figure 75
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 75
Write data hold time		t_{HE}	20	—	—	ns	Figure 75
Read data delay time		t_{DDRE}	—	—	350	ns	Figure 75
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 75

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	330 (T.B.D.)	—	—	ns	Figure 75
	Read	t_{CYCE}	500 (T.B.D.)	—	—		
Enable high-level pulse width	Write	PW_{EH}	70 (T.B.D.)	—	—	ns	Figure 75
	Read	PW_{EH}	250 (T.B.D.)	—	—		
Enable low-level pulse width	Write	PW_{EL}	200 (T.B.D.)	—	—	ns	Figure 75
	Read	PW_{EL}	200 (T.B.D.)	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 75
Setup time (RS, R/W to E, CS*)		t_{ASE}	60	—	—	ns	Figure 75
Address hold time		t_{AHE}	20	—	—	ns	Figure 75
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 75
Write data hold time		t_{HE}	20	—	—	ns	Figure 75
Read data delay time		t_{DDRE}	—	—	250	ns	Figure 75
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 75

80-system Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	500 (T.B.D.)	—	—	ns	Figure 76
	Read	t_{CYCR}	800 (T.B.D.)	—	—	ns	Figure 76
Write low-level pulse width		PW_{LW}	120 (T.B.D.)	—	—	ns	Figure 76
Read low-level pulse width		PW_{LR}	350 (T.B.D.)	—	—	ns	Figure 76
Write high-level pulse width		PW_{HW}	300 (T.B.D.)	—	—	ns	Figure 76
Read high-level pulse width		PW_{HR}	300 (T.B.D.)	—	—	ns	Figure 76
Write/Read rise/fall time		t_{WRr} , $_{WRf}$	—	—	25	ns	Figure 76
Setup time (RS to CS*, WR*, RD*)		t_{AS}	60	—	—	ns	Figure 76
Address hold time		t_{AH}	20	—	—	ns	Figure 76
Write data setup time		t_{DSW}	60	—	—	ns	Figure 76
Write data hold time		t_{H}	20	—	—	ns	Figure 76
Read data delay time		t_{DDR}	—	—	350	ns	Figure 76
Read data hold time		t_{DHR}	5	—	—	ns	Figure 76

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	330 (T.B.D.)	—	—	ns	Figure 76
	Read	t_{CYCR}	500 (T.B.D.)	—	—	ns	Figure 76
Write low-level pulse width		PW_{LW}	70 (T.B.D.)	—	—	ns	Figure 76
Read low-level pulse width		PW_{LR}	250 (T.B.D.)	—	—	ns	Figure 76
Write high-level pulse width		PW_{HW}	200 (T.B.D.)	—	—	ns	Figure 76
Read high-level pulse width		PW_{HR}	200 (T.B.D.)	—	—	ns	Figure 76
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 76
Setup time (RS to CS*, WR*, RD*)		t_{AS}	60	—	—	ns	Figure 76
Address hold time		t_{AH}	20	—	—	ns	Figure 76
Write data setup time		t_{DSW}	60	—	—	ns	Figure 76
Write data hold time		t_{H}	20	—	—	ns	Figure 76
Read data delay time		t_{DDR}	—	—	250	ns	Figure 76
Read data hold time		t_{DHR}	5	—	—	ns	Figure 76

Clock-synchronized Serial Interface Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

(V_{CC} = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	At write (receive)	t_{SCYC}	0.5	—	20	µs	Figure 77
	At read (send)	t_{SCYC}	1	—	20	µs	Figure 77
Serial clock high-level width	At write (receive)	t_{SCH}	230	—	—	ns	Figure 77
	At read (send)	t_{SCH}	480	—	—	ns	Figure 77
Serial clock low-level width	At write (receive)	t_{SCL}	230	—	—	ns	Figure 77
	At read (send)	t_{SCL}	480	—	—	ns	Figure 77
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	20	ns	Figure 77
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 77
Chip select hold time		t_{CH}	200	—	—	ns	Figure 77
Serial input data setup time		t_{SISU}	100	—	—	ns	Figure 77
Serial input data hold time		t_{SIH}	100	—	—	ns	Figure 77
Serial output data delay time		t_{SOD}	—	—	400	ns	Figure 77
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 77

(V_{CC} = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	At write (receive)	t_{SCYC}	0.2	—	20	µs	Figure 77
	At read (send)	t_{SCYC}	0.5	—	20	µs	Figure 77
Serial clock high-level width	At write (receive)	t_{SCH}	80	—	—	ns	Figure 77
	At read (send)	t_{SCH}	230	—	—	ns	Figure 77
Serial clock low-level width	At write (receive)	t_{SCL}	80	—	—	ns	Figure 77
	At read (send)	t_{SCL}	230	—	—	ns	Figure 77
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	20	ns	Figure 77
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 77
Chip select hold time		t_{CH}	200	—	—	ns	Figure 77
Serial input data setup time		t_{SISU}	40	—	—	ns	Figure 77
Serial input data hold time		t_{SIH}	40	—	—	ns	Figure 77
Serial output data delay time		t_{SOD}	—	—	200	ns	Figure 77
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 77

Reset Timing Characteristics (V_{CC} = 2.2 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 78

Electrical Characteristics Notes

1. For bare die products, specified up to 85°C.
2. The following three circuits are I/O pin configurations (figure 69).

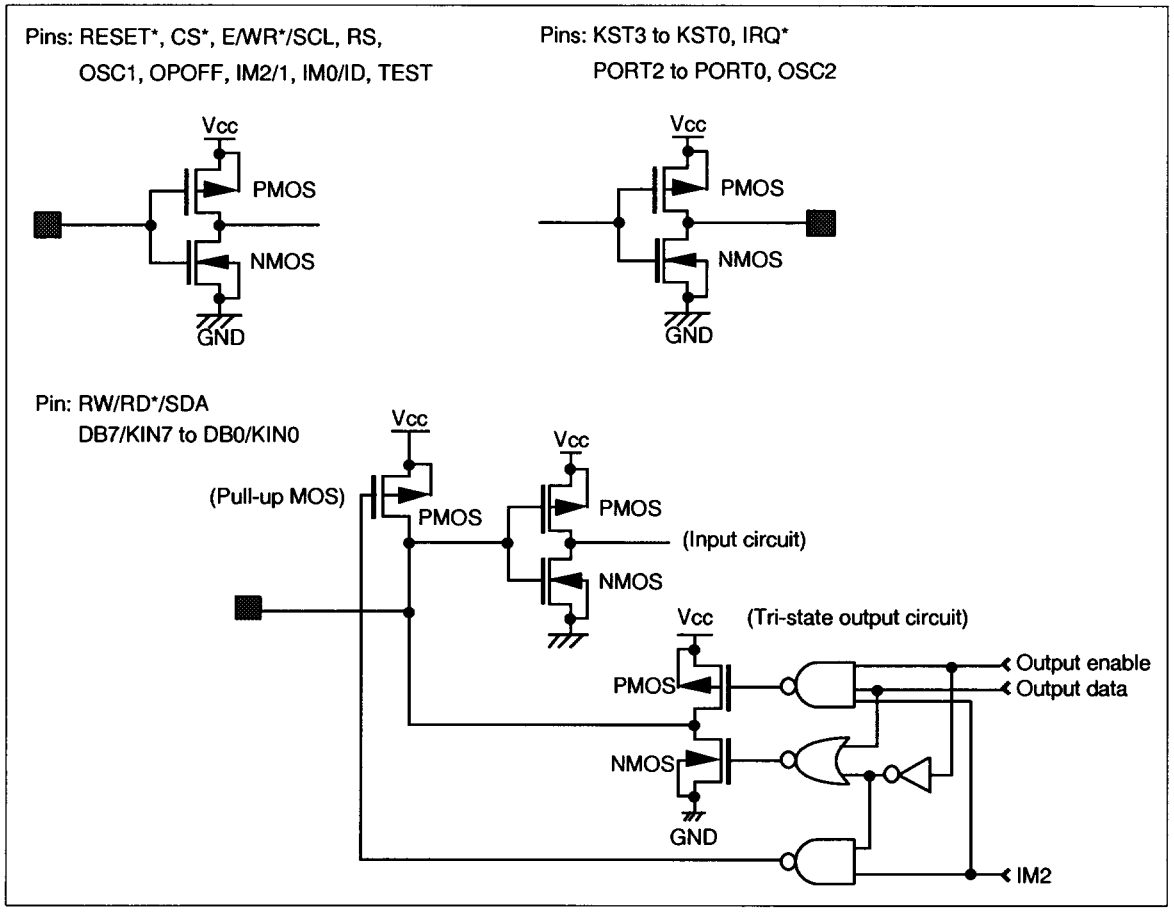


Figure 69 I/O Pin Configuration

3. The TEST pin must be grounded and the IM2/1, IM0/ID, and OPOFF pins must be grounded or connected to Vcc.
4. Corresponds to the high output for clock-synchronized serial interface.
5. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins, and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins, when current Id is flown through all driver output pins.
6. This excludes the current flowing through pull-up MOSs and output drive MOSs.
7. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
8. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 70).

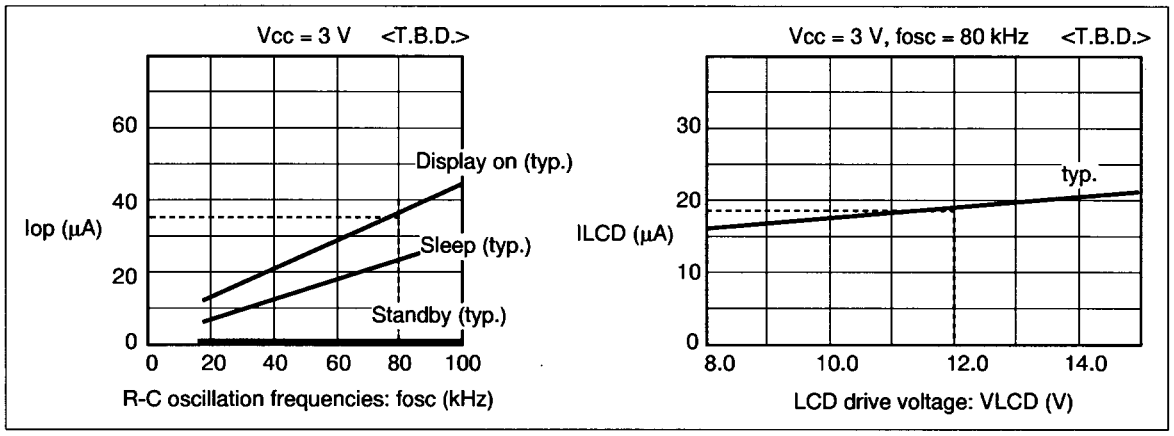


Figure 70 Relationship between the Operation Frequency and Current Consumption

9. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (Vcc, V1, V2, V3, V4, V5) when there is no load.
10. Applies to the external clock input (figure 71).

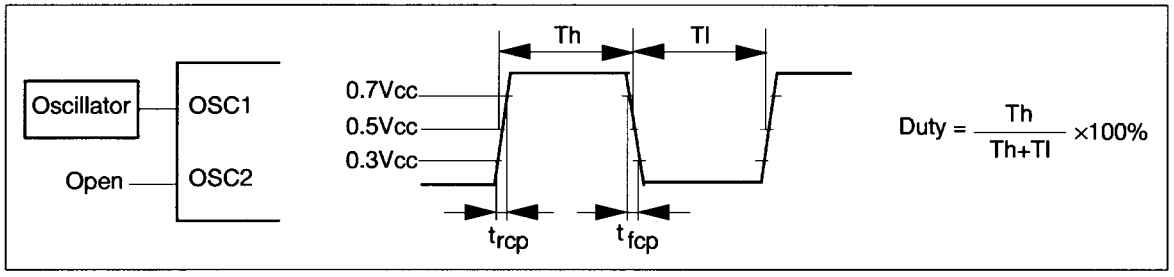


Figure 71 External Clock Supply

11. Applies to the internal oscillator operations using external oscillation resistor Rf (figure 72 and table 42).

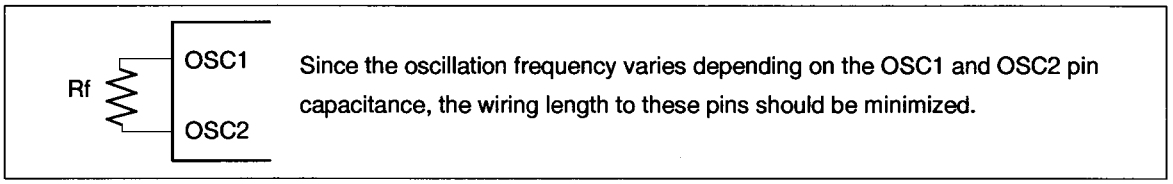


Figure 72 Internal Oscillation

Table 42 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (Rf)	R-C Oscillation Frequency: fosc <T.B.D.>				
	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 4.0 V	Vcc = 5.0 V
180 kΩ			92 kHz		
200 kΩ			87 kHz		
220 kΩ			80 kHz		
240 kΩ			73 kHz		
270 kΩ			65 kHz		
300 kΩ			61 kHz		

12. Booster characteristics test circuits are shown in figure 73.

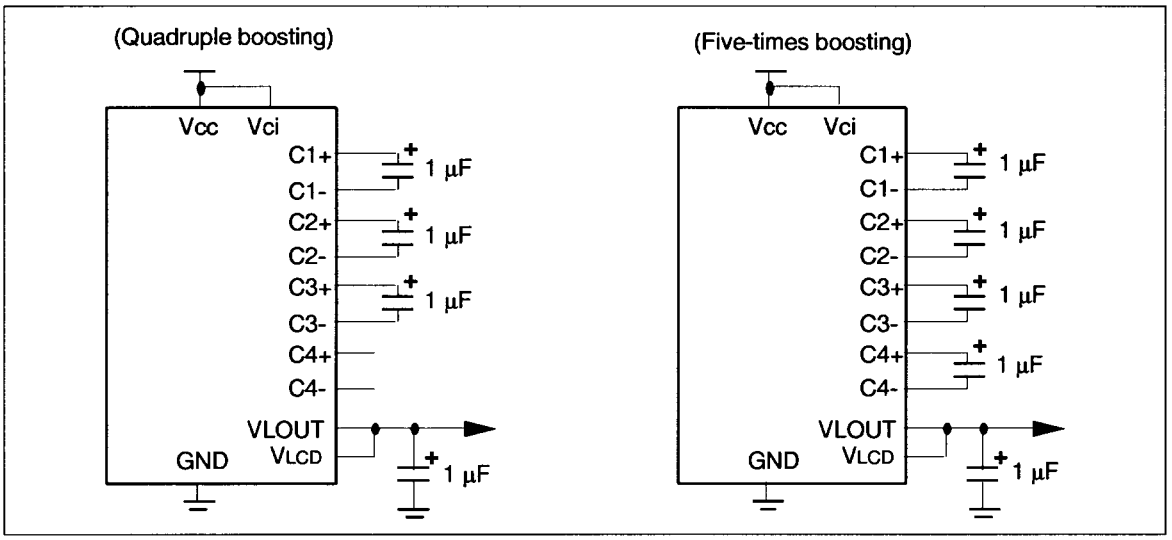
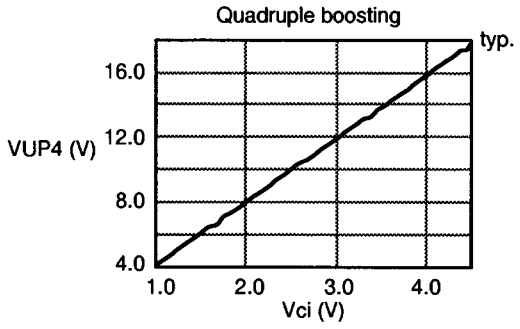


Figure 73 Booster

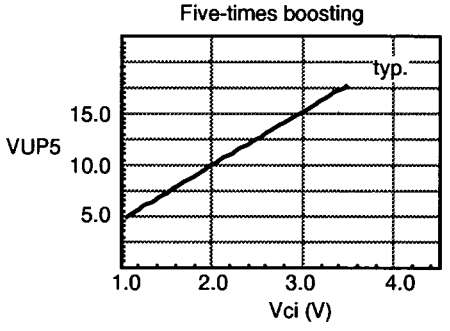
Referential data

VUP4 = VLCD – GND; VUP5 = VLCD – GND

(i) Relation between the obtained voltage and input voltage

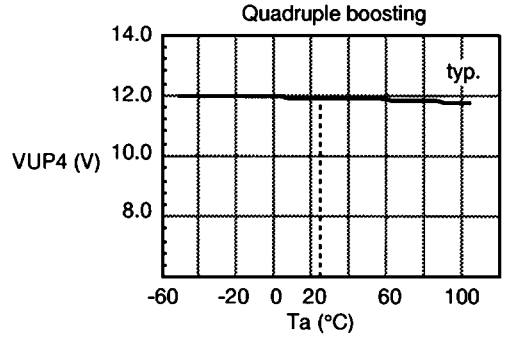


Vci = Vcc, fosc = 80 kHz, Ta = 25°C

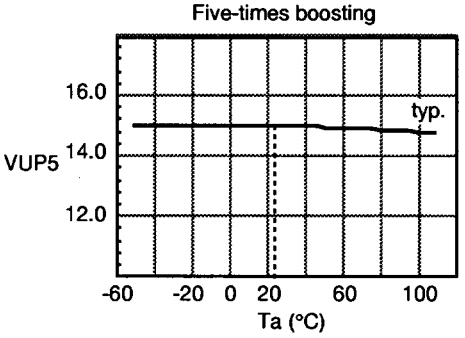


Vci = Vcc, fosc = 80 kHz, Ta = 25°C

(ii) Relation between the obtained voltage and temperature

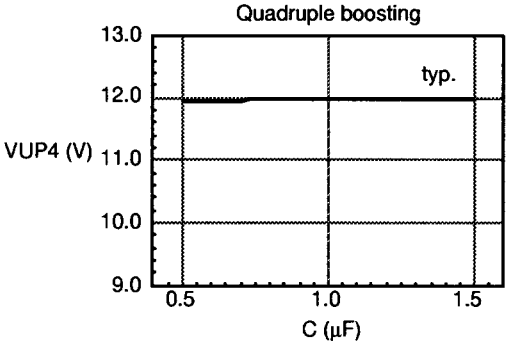


Vci = Vcc = 3 V, fosc = 80 kHz, Io = 30μA

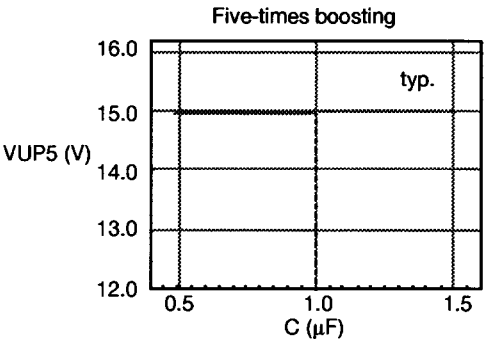


Vci = Vcc = 3 V, fosc = 80 kHz, Io = 30μA

(iii) Relation between the obtained voltage and capacity



Vci = Vcc = 3.0 V, fosc = 80 kHz, Io = 30 μA



Vci = Vcc = 3.0 V, fosc = 80 kHz, Io = 30 μA

Figure 73 Booster (cont)

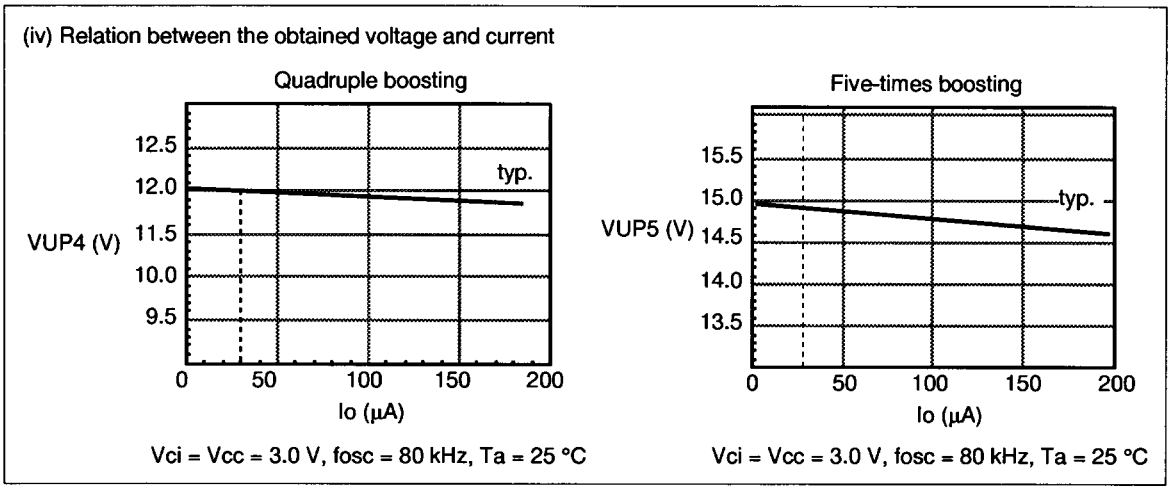


Figure 73 Booster (cont)

Load Circuits

AC Characteristics Test Load Circuits

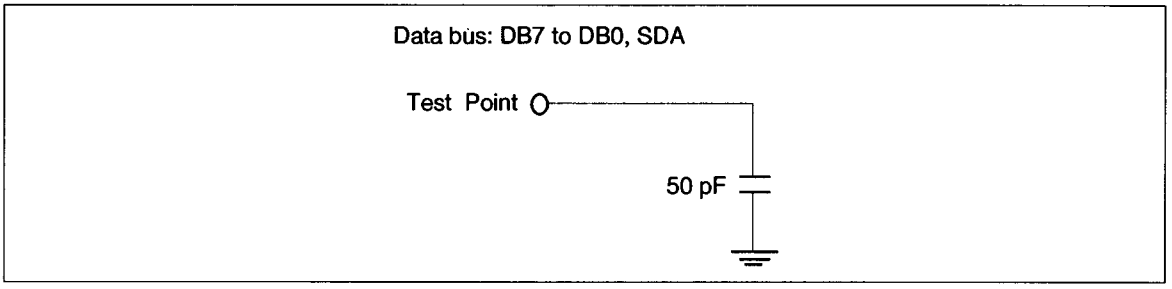
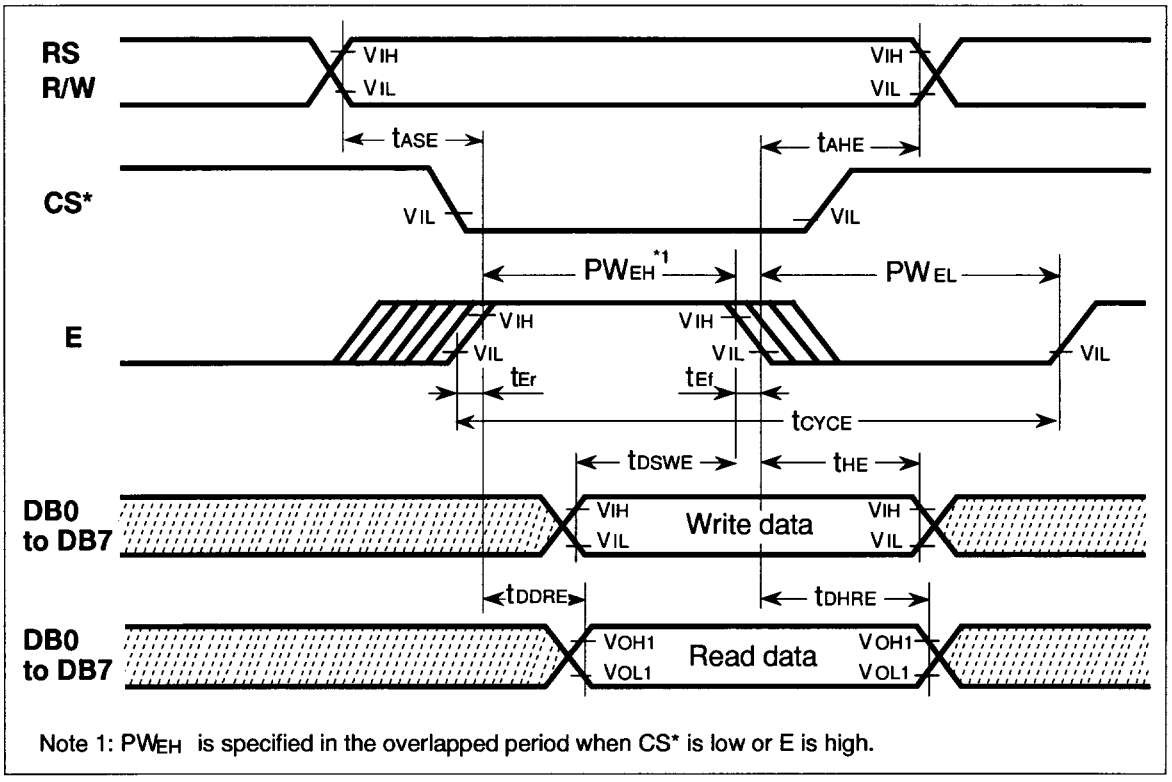


Figure 74 Load Circuit

Timing Characteristics

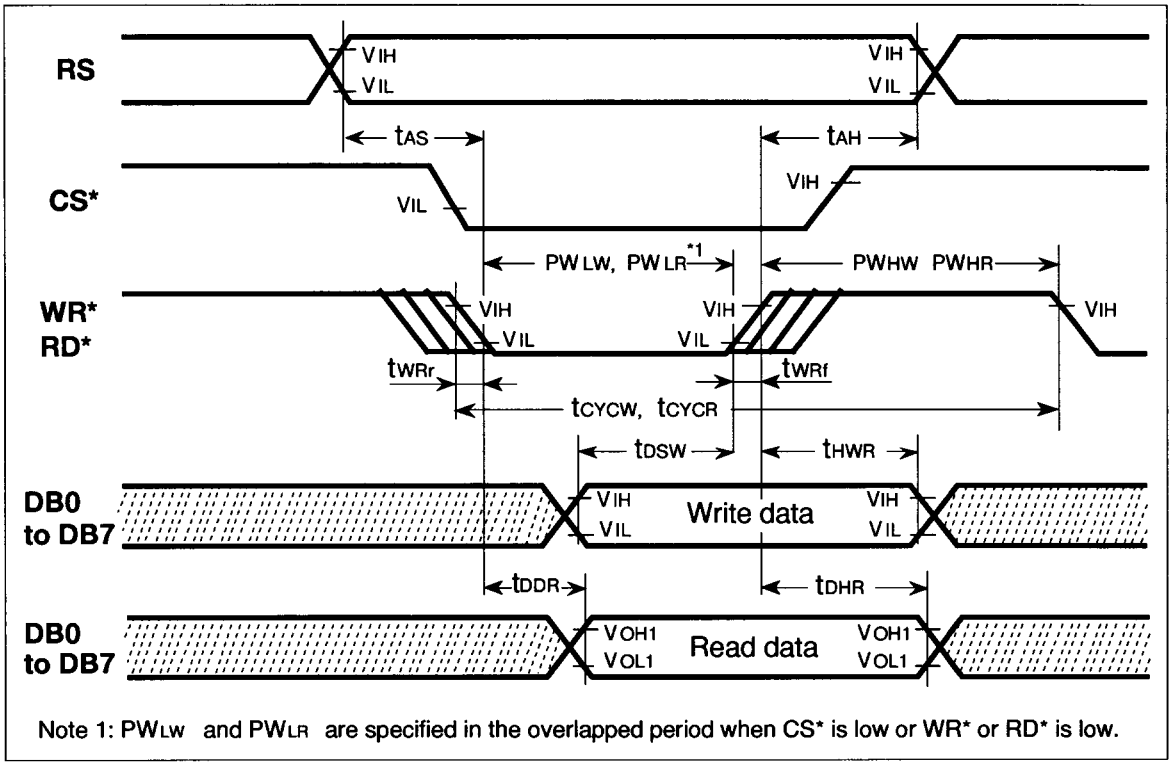
68-system Bus Operation



Note 1: PW_{EH} is specified in the overlapped period when CS* is low or E is high.

Figure 75 68-system Bus Timing

80-system Bus Operation



Note 1: PW_{LW} and PW_{LR} are specified in the overlapped period when CS* is low or WR* or RD* is low.

Figure 76 80-system Bus Timing

Clock-synchronized Serial Operation

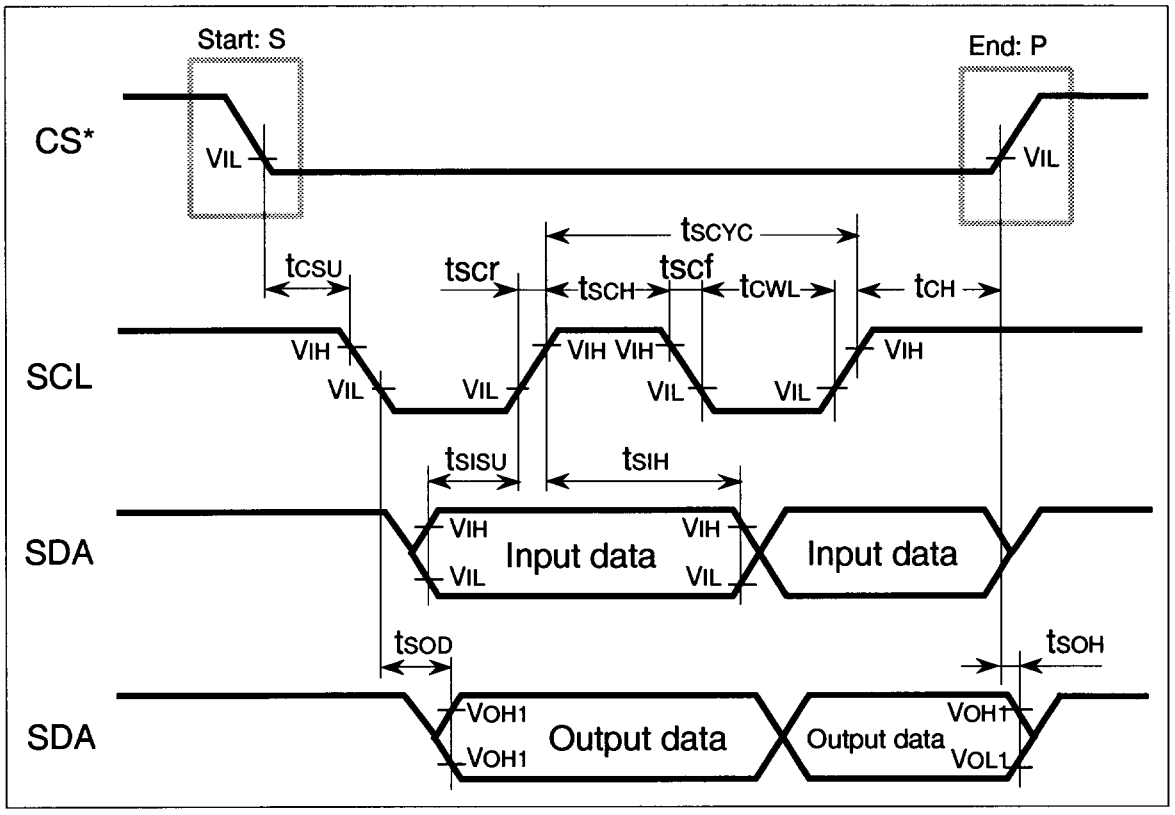


Figure 77 Clock-synchronized Serial Interface Timing

Reset Operation

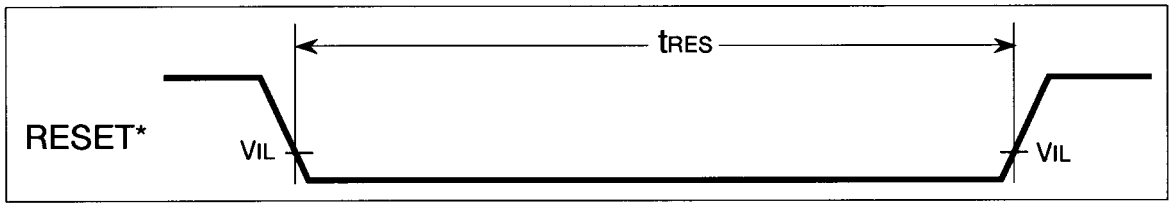


Figure 78 Reset Timing