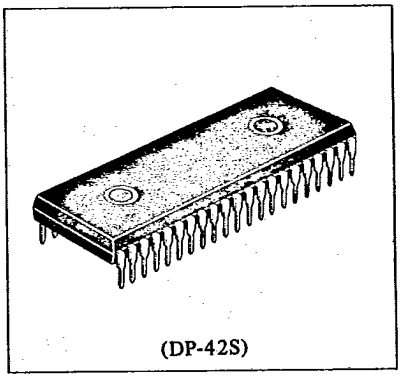
HA16640NT

Preliminary
February 1985

HITACHI

Write/Mechanism Controller for Floppy Disk Drive

This IC can provide WRITE + MECHANISM CONTROL function is one chip for FLOPPY DISK DRIVE

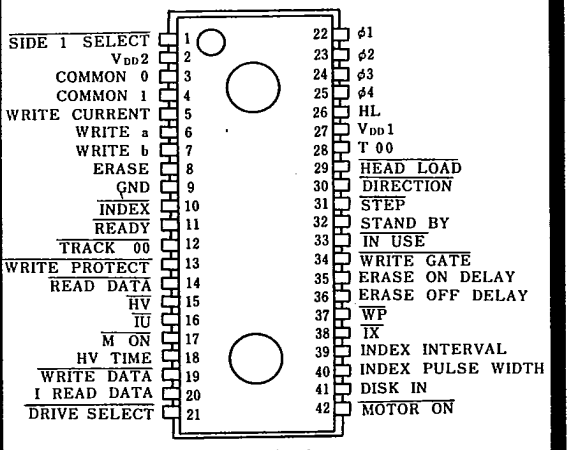


(DP-42S)

■ FEATURES

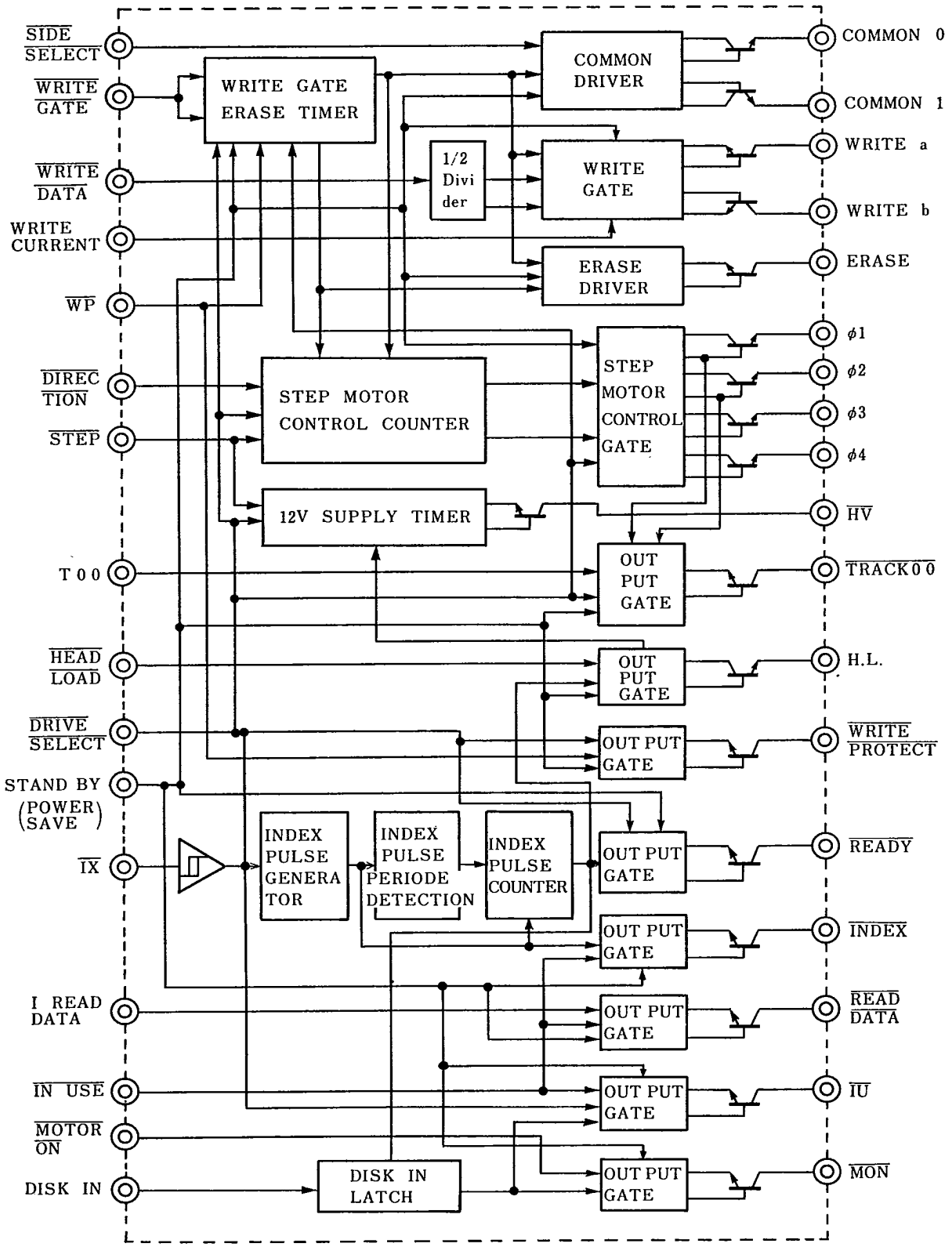
- WRITE Circuit includes COMMON, WRITE, ERASE drivers, and has capability of application for many kind of FDD.
- WRITE Circuit also includes tripple power supply monitor circuits, so can protect the Disk from abnormal writing or erasing at ON, OFF of supply voltage.
- The delay time between write gate and erase gate timing is generated by internal MONO MULTI Circuit, so this IC is able to apply for many kind of FDD and HEAD component.
- The function of MECHANISM CONTROL circuit conforms to the standard FDD's interface.
- MECHANISM CONTROL Circuit has a power save function, and at the stand-by mode in operation, power save circuit protects the equipment from internal temperature increasing by inhibiting the load current in external components, and also reduces the power dissipation in IC chip.
- The output interface has capability of large drive current, and internal logic circuit has low power consumption by means of Bi-CMOS technology. Especialy, in the output interface circuit, it is not necessary to have any external TTL ICs because of including line drivers into IC chip.
- With this device, it is able to design the print circuit board without TTL ICs, and to reduce many external components, also to shrink an area of print circuit board.
- Signal processing and control circuit in FDD are able to be constructed with only two ICs and some external discrete devices by connecting with FDD READ IC, HA16631P/MP.

■ PIN CONFIGURATION



(Top View)

■ BLOCK DIAGRAM



* In the WRITE CIRCUIT, power supply monitor circuits are included to watch the Line Voltage of 5V and 12V. When the line voltage goes down to abnormal value, the COMMON, WRITE, ERASE drivers are all inhibited rapidly.

■ ABSOLUTE MAXIMUM RATING (T_a=25°C)

Item	Symbol	Ratings	Unit	Applicable Terminal
Supply Voltage	V_{DD1}	−0.3 to +7.0	V	V_{DD1}
Supply Voltage	V_{DD2}	−0.3 to +14.0	V	V_{DD2}
Interface Input Voltage	V_{IN1}	−0.3 to V_{DD1}	V	Note 1
Interface Input Voltage	V_{IN2}	−0.3 to V_{DD2}	V	Note 2
Interface Output Current	I_{OL1}	50	mA	Note 3
$\overline{IU}$ Terminal Output Current	I_{OL2}	20	mA	IU
$\overline{HV}$ Terminal Output Current	I_{OL3}	15	mA	HV
$\overline{MON}$ Terminal Output Current	I_{OL4}	5	mA	MON
HL Terminal Output Current	I_{OH5}	10	mA	HL
STEP Terminal Output Current	I_{OH6}	5	mA	$\phi1$ $\phi2$ $\phi3$ $\phi4$
COMMON Drive Current (WRITE MODE)	I_{OCW}	100	mA	COMMON ϕ.1.
COMMON Drive Current (READ MODE)	I_{OCR}	5	mA	COMMON ϕ.1.
WRITE Drive Current	I_{OWW}	15	mA	WRITE a,b
ERASE Drive Current	I_{OEW}	85	mA	ERASE
Input Current on the WRITE Current Set Terminal	I_{WC}	3.75	mA	WRITE CURRENT
Power Dissipation	P_D	850 (0 to 50°C)	mW	
Operating Temperature Range	T_{OP}	0 to +70	°C	
Storage Temperature Range	T_{stg}	−55 to +125	°C	

Notes 1. Applicable Terminal: $\overline{\text{SIDE SELECT}}$, $\overline{\text{WRITE DATA}}$, $\overline{\text{STEP}}$, $\overline{\text{DIRECTION}}$, $\overline{\text{IN USE}}$, $\overline{\text{MOTOR ON}}$, $\overline{\text{HEAD LOAD}}$, STAND BY, $\overline{\text{WRITE GATE}}$, $\overline{\text{DRIVE SELECT}}$, IREAD DATA

2. Applicable Terminal: T00, DISK IN, $\overline{WP}$, $\overline{IX}$ and also Terminals from MM Circuit connecting with the external C,R time constant.

3. Except for $\overline{IU}$, $\overline{HV}$, $\overline{MON}$, HL, $\phi1$ $\phi2$ $\phi3$ $\phi4$.

■ ELECTRICAL CHARACTERISTICS (T_a = 25°C)

	Circuit Block	Item	Test Condition	Symbol	min	typ	max	Unit
WRITE Circuit	Supply Voltage	Supply Voltage Range		V_{DD1}	4.5	5.0	5.5	V
		Supply Voltage Range		V_{DD2}	10.8	12.0	13.2	V
	COMMON Driver	Output Voltage at Selected WRITE Mode	V_{DD2} = 12V I_{OCW} = −100mA	V_{OCW}	−	10.7	−	V
		Output Voltage at Unselected WRITE Mode	V_{DD2} = 12V Unselected	V_{OCWU}	−	−	0.7	V
		Output Voltage at Selected READ Mode	V_{DD2} = 12V I_{COR} = −5mA	V_{OCR}	−	4.7	−	V
		Output Voltage at Unselected READ Mode	V_{DD2} = 12V Unselected	V_{OCRU}	−	−	0.7	V
		Output Current Range		I_{COM}	−	−	100	mA
	WRITE Driver	Input Current Range on the WRITE Current set Terminal		I_{WC}	0	−	2.5	mA
		WRITE Current Accuracy	WRITE Driver output Voltage = 10V I_{WC} = 1mA	I_{OWW}	3.6	4.0	4.4	mA
		WRITE Current Temperature Coefficient	I_{WC} = 1mA T_a = 0 to 70°C	TCI_{OW}	−	±0.05	−	%/°C
		WRITE Current Symmetry	V_{DD1} = 5V, V_{DD2} = 12V I_{owa}-I_{owb}	ΔI_{OW}	−1	−	+1	%
		Leak Current	V_{DD1} = 5V, V_{DD2} = 12V V_{OW} = 20V	I_{LKW}	−	−	100	μA
	ERASE Driver	Output Low Voltage	V_{DD1} = 4.5V I_{OE} = 80mA	V_{OLER}	−	−	0.6	V
		Output Leak Current	V_{DD1} = 5.5V V_{OER} = 20V	I_{LKER}	−	−	200	μA
	Lower Line Voltage Protector	12V Detection Voltage		V_{PRV12}	−	8.1	−	V
		5V Detection Voltage		V_{PRV5}	−	3.8	−	V

	Circuit Block	Item	Test Condition	Symbol	min	typ	max	Unit
WRITE Circuit	Signal Interface (Note 1)	High Level Input Voltage	V_{DD1} = 5.0V	V_{IHI}	2.4	–	–	V
		Low Level Input Voltage	V_{DD1} = 5.0V	V_{ILI}	–	–	0.8	V
	Signal Interface (Note 1)	High Level Input Current	V_{DD1} = 5.5V V_{IH} = 5.5V	I_{HI}	–	–	10	μA
		Low Level Input Current	V_{DD1} = 5.5V V_{IL} = 0V	I_{ILI}	–10	–	–	μA
	Sensor Interface (Note 2)	High Level Input Voltage	V_{DD1} = 5.0V	V_{IHS}	3.3	–	–	V
		Low Level Input Voltage	V_{DD1} = 5.0V	V_{ILS}	–	–	1.7	V
		High Level Input Current	V_{DD1} = 5.5V V_{IH} = 5.5V	I_{IHS}	–	–	10	μA
		Low Level Input Current	V_{DD1} = 5.5V V_{IL} =0V	I_{ILS}	–10	–	–	μA
	Index Input Interface	Higher Threshold Voltage	V_{DD1} = 5V	V_{THIX}	–	3.5	–	V
		Lower Threshold Voltage	V_{DD1} = 5V	V_{THIX}	–	2.0	–	V
		Hysterisis	V_{DD1} = 5V	V_{HYS}	–	1.5	–	V
		Input Current	V_{DD1} = 4.5V V_{IH} = 2.6V	I_{IHIX}	–80	–	100	μA
Mechanism Control Circuit	Signal Output Interface	Low Level Output Voltage	V_{DD1} = 4.5V I_{OL} = 48mA	V_{OLI}	–	-	0.4	V
		High Level Output Current	V_{DD1} = 5.5V V_{OH} = 5.5V	I_{OHI}	–	–	250	μA
	IU Output	Low Level Output Voltage	V_{DD1} = 4.5V I_{OL} = 10mA	V_{OLIU}	–	–	0.5	V
		High Level Output Current	V_{DD1} = 5.5V V_{OH} = 5.5V	I_{OHIU}	–	–	100	μA
	HV Output	Low Level Output Voltage	V_{DD1} = 4.5V I_{OL} = 15mA	V_{OLHV}	–	–	0.5	V
		High Level Output Current	V_{DD1} = 5.5V V_{OH} = 13.2V	I_{OHHV}	–	–	100	μA
	MON Output	Low Level Output Voltage	V_{DD1} = 4.5V I_{OL} = 5mA	V_{OLMN}	–	–	0.4	V
		High Level Output Current	V_{DD1} = 5.5V V_{OH} = 5.5V	I_{OHMN}	–	–	50	μA
	HL Output	High Level Output Voltage	V_{DD1} = 5V I_{OH} = –10mA	V_{OHHL}	3.6	–	–	V
		Low Level Output Current	V_{DD1} = 5.5V V_{OL} = 0V	I_{OLHL}	–20	–	–	μA
	STEP Output	High Level Output Voltage	V_{DD1} = 5V I_{OH} = –5mA	V_{OHSTP}	3.6	–	–	V
		Low Level Output Current	V_{DD1} = 5.5V V_{OL} =0V	I_{OLSTP}	–20	–	–	μA
	ERASE Timer	ERASE ON DELAY	Cex = 0.034μF Rex = 33kΩ	t_{EN}	0.42	0.50	0.58	ms
		ERASE OFF DELAY	Cex = 0.069μF Rex = 33kΩ	t_{EF}	0.86	1.02	1.18	ms
	INDEX, READY Circuit	Index Pulse Width	Cex = 0.033μF Rex = 220kΩ	t_{IXW}	2.61	3.08	3.55	ms
		Index Detection Period	Cex = 0.22μF Rex = 390kΩ	t_{IXI}	31.1	36.6	42.1	ms
	12V Hold Timer	Hold Period at 12V	Cex = 2.3μF Rex = 56kΩ	t_{HV}	47.1	55.5	63.9	ms
	Dissipation Current	Supply Current 1	V_{DD1} = 5.5V, V_{DD2} = 13.2V No Load	I_{DD1}	–	–	65	mA
		Supply Current 2	V_{DD1} = 5.5V, V_{DD2} = 13.2V No Load	I_{DD2}	–	–	10	mA

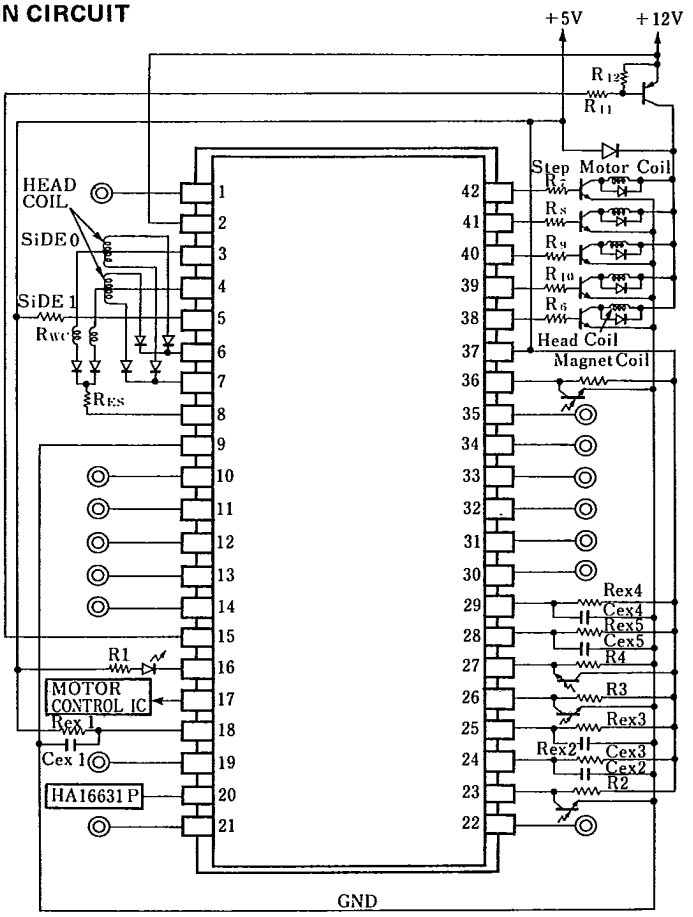
■ Pin Description

Symbol	Name	Description
COM 0	Common Driver 0	Output terminal of Common Driver (SIDE 0). During the Head Select signal is selecting SIDE 0, a common voltage appears on this terminal. The voltage value at WRITE Mode and that READ Mode are shown in the Electrical Characteristics. This terminal supplies a current which equals to write current + erase current. When the SIDE 0 is unselected, a common voltage doesn't appear, and this terminal is pulled down to ground by a internal resistor with high resistance.
COM 1	Common Driver 1	Output terminal of Common Driver. (SIDE 1). The function is as same as that of SIDE 0.
$\overline{\text{SIDE SELECT}}$	Side Select	Input terminal for Head Select signal. This signal selects the SIDE 0 or SIDE 1 of the common driver.
WRITE a, b	Write Drive a, b	Output terminal of Write Driver. The current multiplied by 4 with the determined current at the write current terminal is sinked. WRITE a and WRITE b turn on alternately according to the Write Data "1" or "0".
ERASE	Erase Driver	Output terminal of Erase Driver. The drive transistor turns on during the period of Erase Gate signal keeping low, and the Erase Gate timing is generated by write Gate signal in IC circuit. This terminal has open collector NPN transistor, and erase current must be determined by an external resistor.
WRITE CURRENT	Write Current	The terminal to determine the Write Current. The Write current is determined with connecting an external resistor to +5V supply. The Write Current on the WRITE a, b terminals is multiplied by 4 with the current on the WRITE CURRENT terminal, as follow equation. $I_{WT} = \frac{3.38}{Rex} \times 4$ (mA) where, I_{WT}: WRITE CURRENT on the WRITE a, b Terminals. Rex : External pull up resistor on the WRITE CURRENT terminal, and use the Value in kΩ unit.
$\overline{\text{WRITE DATA}}$	Write Data Input	Write Data input terminal. The signal is devided through the counter in IC, and drives the Write Driver.
$\overline{\text{WRITE GATE}}$	Write Gate	Input terminal for Write Gate signal. The write gate is enable at input Low, and allows data writing. Erase Gate signal is generated with the determined delay from the negative and positive edge of write Gate signal, and drives an erase driver.
$\overline{\text{WP}}$	Write Protect Input	Input terminal for the detected write protect signal from the Disk. Common, Write, Erase drivers are all inhibited at input low, and WRITE PROTECT driver turns ON.
ERASE ON DELAY	Erase ON Timer	Terminal for connecting the external time contact Cex, Rex of internal Mono Multi circuit to determine the delay time between the both negative edge of write Gate and Erase Gate signal. It is necessary to determine the delay time for the fittest value according to the kind of FDD and HEAD component.
ERASE OFF DELAY	Erase OFF Timer	As same as above, but the delay time is determined between the both positive edge of Write Gate signal and Erase Gate signal.
STEP	step signal Input	Terminal for step pulse input to drive the stepping motor to seek tracks. With each one step pulse input, the driver outputs ϕ_1, ϕ_2, ϕ_3, ϕ_4 change sequentialy.
$\overline{\text{DIRECTION}}$	Direction Input	Input terminal for Direction signal to determine the direction of stepping motor revolution. Output drivers change with the direction of $\phi_1 \rightarrow \phi_2 \rightarrow \phi_3 \rightarrow \phi_4$ at the input low, and $\phi_1 \rightarrow \phi_4 \rightarrow \phi_3 \rightarrow \phi_2$ at the input High.
ϕ_1, ϕ_2 ϕ_3, ϕ_4	4 Phase stepper Drive Output	Output terminals to drive the stepping motor coil. With each step pulse input, outputs change with the direction determined by Direction signal. Output driver has emitter follower construction, but the driver cannot drive the stepping motor coil directly. It is necessary to have external driver devices such as discrete transistors.

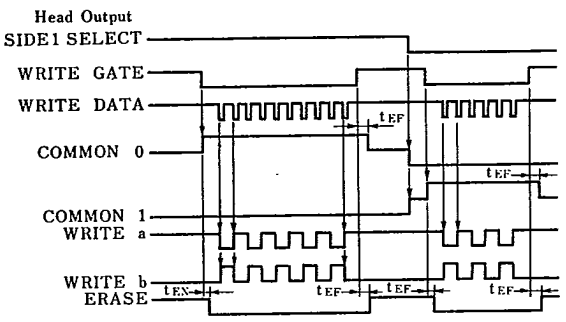
Symbol	Name	Description
$\overline{HV}$	Voltage Change Timer	Timer output terminal to drive an external transistors switching supply voltage 12V to 5V each other for stepping motor coil. With each step pulse input or each head load execution, the output turns ON during the determined period. It is enable to switch supply voltage 12V to 5V alternately and to supply 12V for the stepping motor coil during the period of Low level on this terminal.
HV TIME	HV Timer	Terminal for connecting the external time constant of internal Mono Multi circuit to determine the period of keeping the HV output Low level.
$\overline{WRITE\ PROTECT}$	Write Protect Output	When the input level of $\overline{WP}$ turns Low and the drive select is executed, this output turns ON.
T00	Track 00 Input	Input terminal for 00 track detection. High level input makes the 00 track detection.
TRACK 00	Track 00 Output	Output terminal for 00 track detection. When the input level of T00 is High, and the both output ϕ_1, ϕ_2 are High, this output turns ON.
$\overline{IX}$	Index Input	Input terminal for the detected Index hole signal from the DISK. Input Low shows the hole detection.
$\overline{INDEX}$	Index Ouput	Output for the Index pulse. With each input of the detected Index pulse at the $\overline{IX}$ terminal, the width formed pulse appears on this terminal as a Index pulse.
INDEX PULSE WIDTH	Index pulse Width set	Terminal for connecting the external time constant of the internal Mono Multi circuit to determine the output pulse width on $\overline{INDEX}$. It is enable to adjust the pulse width independently to the diameter of the DISK hole.
$\overline{READY}$	Ready Output	Output of the Ready signal. When the disk revolution gets to the normal, after counting three index pulses, the output on this terminal turns ON, and shows FDD has gone into READY state. If the revolution goes down under the normal value, the output turns OFF rapidly and shows NOT READY state. And also the output shows High level continuously when Drive unit is not selected.
INDEX INTERVAL	Index Interval	Terminal for connecting the external time constant of the internal Mono Multi circuit to determine the reference index period corresponding to the standard revolution number of the DISK. In case of the FDD equipment having another revolution number, it is easier to adjust reference period by changing the time constant.
$\overline{DRIVE\ SELECT}$	Drive Select Input	Input terminal for Drive select signal. Input low makes the selected operation, and Write function, output interface, IU output are all enable.
STAND BY	Stand by Input	Input terminal for Power Save Signal to reduce the power consumption in FDD equipment and LSI. Input high inhibits all output terminals in write and Mechanism control circuit except common driver, so power consumption in external circuit is reduced and this LSI makes itself into sleep mode. At the same time, common driver turns the READ mode.
$\overline{HEAD\ LOAD}$	Head Load	Input terminal for Head Load signal. When $\overline{READY}$ is low and operation is under the not stand-by mode, head load is enable at the input low.
HL	Head Load Output	Terminal for Head Load output. Circuit has a emitter follower construction. But this terminal cannot drive the coil of head load magnet directly. It is necessary to have an external driving transistor.
$\overline{IN\ USE}$	In Use Output	Input terminal for IN USE signal. When the DISK is charged and the DRIVE equipment is selected, and also the operation is under the not stand-by mode, in use output is enable with the input low.
$\overline{IU}$	In Use Output	In Use Output. Circuit has a open collector NPN transistor, and can drive LED directly.
I READ DATA	Read Data Input	Input terminal for Read Data from READ circuit such as HA16631P/MP. When both $\overline{DRIVE\ SELECT}$ and $\overline{STAND\ BY}$ are Low, inverted read data pulses appear on the READ DATA terminal.

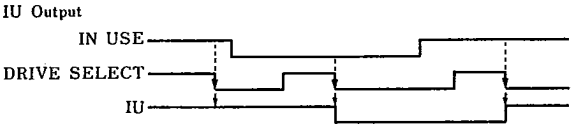
Symbol	Name	Description
$\overline{\text{READ}}$ $\overline{\text{DATA}}$	Read Data Output	Output terminal for Read Data. Circuit has an open collector driver, and negative data pulses appear on this terminal.
DISK IN	Disk in Input	Input terminal for Disk charge detection signal. Input High shows the charged state. When the charged Disk is detected, $\overline{\text{MON}}$ output turns ON and the motor starts, and also IU output turns ON too. This function does not depend on the input level of $\overline{\text{MOTOR ON}}$ and $\overline{\text{IN USE}}$. When the Disk revolution gets to normal state, after counting eight Index pulses, both $\overline{\text{MON}}$ and $\overline{\text{IU}}$ output turns OFF, so the motor stops and IN USE LED turns OFF. After this operation, both $\overline{\text{MON}}$ and $\overline{\text{IU}}$ output depend on the input level of $\overline{\text{MOTOR ON}}$ and $\overline{\text{IN USE}}$. If the Disk is discharged, the motor stops and $\overline{\text{IU}}$ output is inhibited rapidly.
$\overline{\text{MOTOR ON}}$	Motor On	Input terminal for the motor ON, OFF, control signal. Motor ON is enable at the input Low. Under the condition of the charged Disk and not-stand by, $\overline{\text{MON}}$ output turns OFF.
$\overline{\text{MON}}$	Motor On Output	Output terminal for the motor ON, OFF, control signal. Circuit has an open collector NPN driving transistor. Output Low makes the motor ON and High makes OFF. Also this terminal is able to connect to the motor control IC.
V_{DD1}	5V Power Supply	5V Power Supply
V_{DD2}	12V Power Supply	12V Power Supply
GND	Ground	System ground

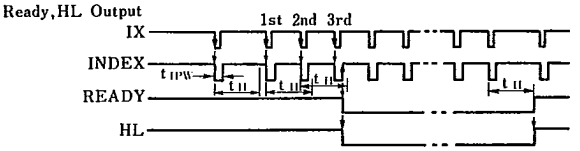
■ EXAMPLE OF APPLICATION CIRCUIT

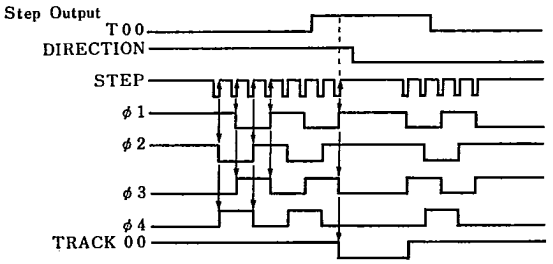


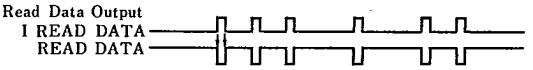
■ TIME CHART

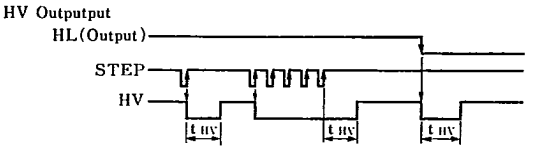


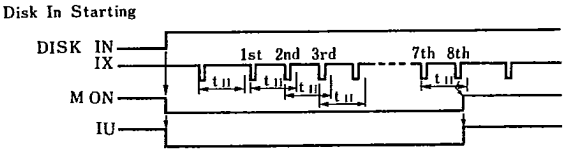












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A World Leader in Technology

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