

**32K Flash Embedded 8-Bit MCU**

# **GMS99C58**

**DATA SHEET**

**Jun. 2001**

**Ver 1.02**



# CONTENTS

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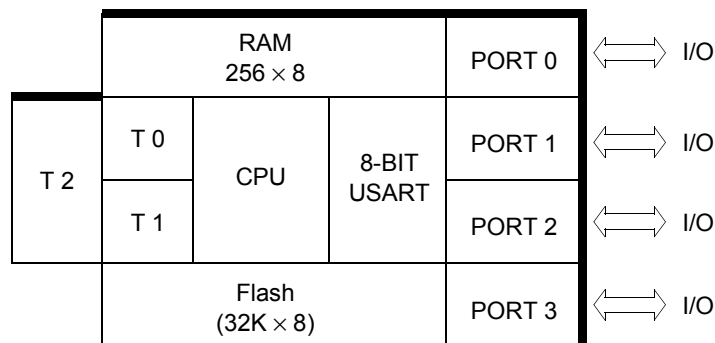
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# GMS99C58

## (32K Flash Embedded 8-Bit MCU)

### Chapter 1. Overview

- Fully compatible to standard 8051 micro controller
- 4.5V to 5.5V operating range
- Versions for 12/24 MHz operating frequency
- 32K × 8Bit Flash ( Endurance: 100 Write/Erase Cycles )
- 256 × 8Bit RAM
- Four 8 Bit ports
- Three 16-bit Timers / Counters (Timer 2 with Up/Down Counter feature)
- USART
- Six interrupt sources, two priority levels
- Power Saving Modes
- 40-PDIP, 44- PLCC and 44-MQFP package
- Temperature ranges : T = 0 °C ~ 70 °C

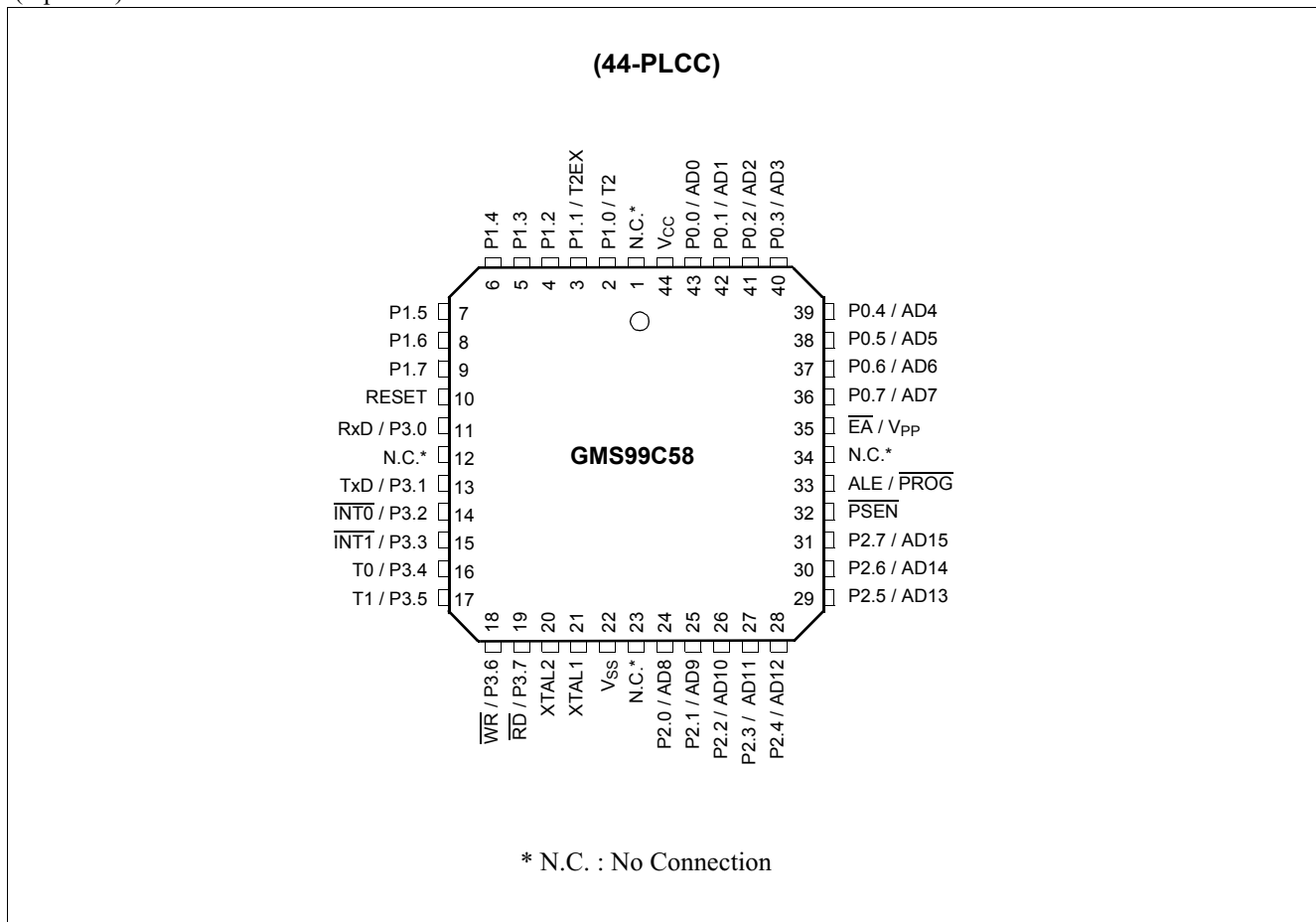


### 1.1 Ordering Information

| TYPE   | Package                       | Description |
|--|-------------------------------|-------------|
| GMS99C58<br>GMS99C58-PL<br>GMS99C58-Q          | 40 PDIP<br>44 PLCC<br>44 MQFP | with 12 MHz |
| GMS99C58-24<br>GMS99C58-PL-24<br>GMS99C58-Q-24 | 40 PDIP<br>44 PLCC<br>44 MQFP | with 24 MHz |

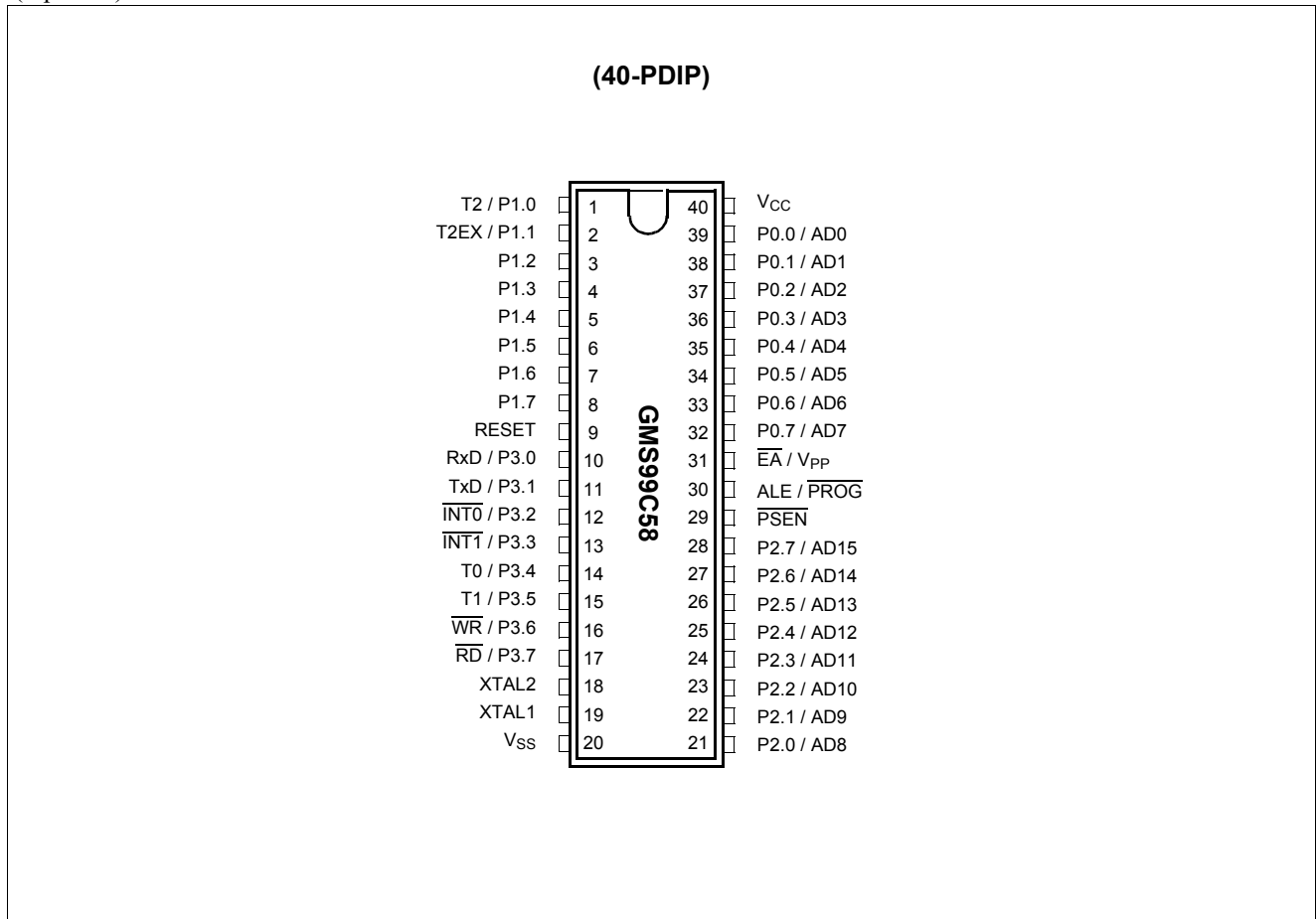
### 1.2 Pin Configuration of 44 PLCC Type

(top view)



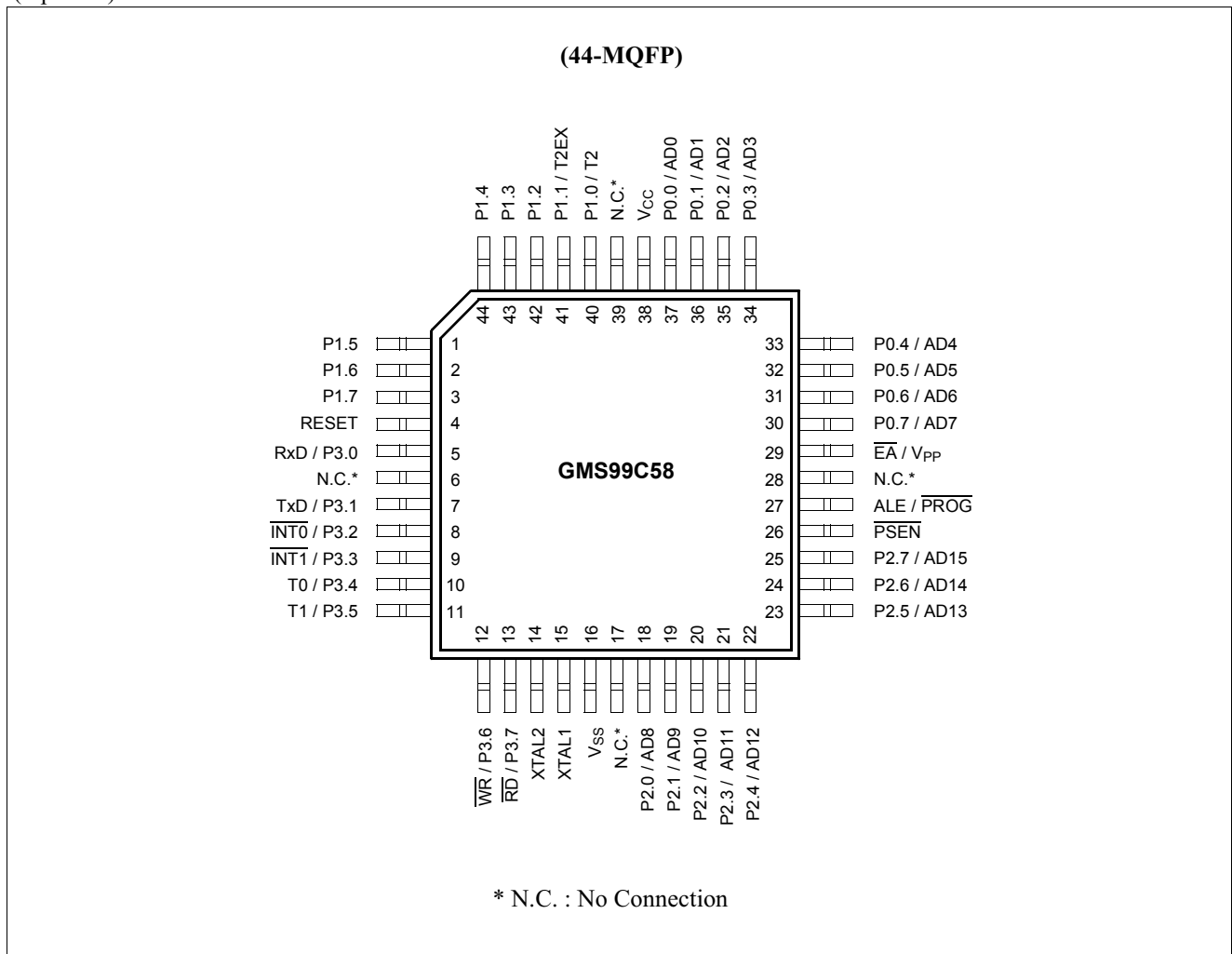
### 1.3 Pin Configuration of 40-PDIP Type

(top view)

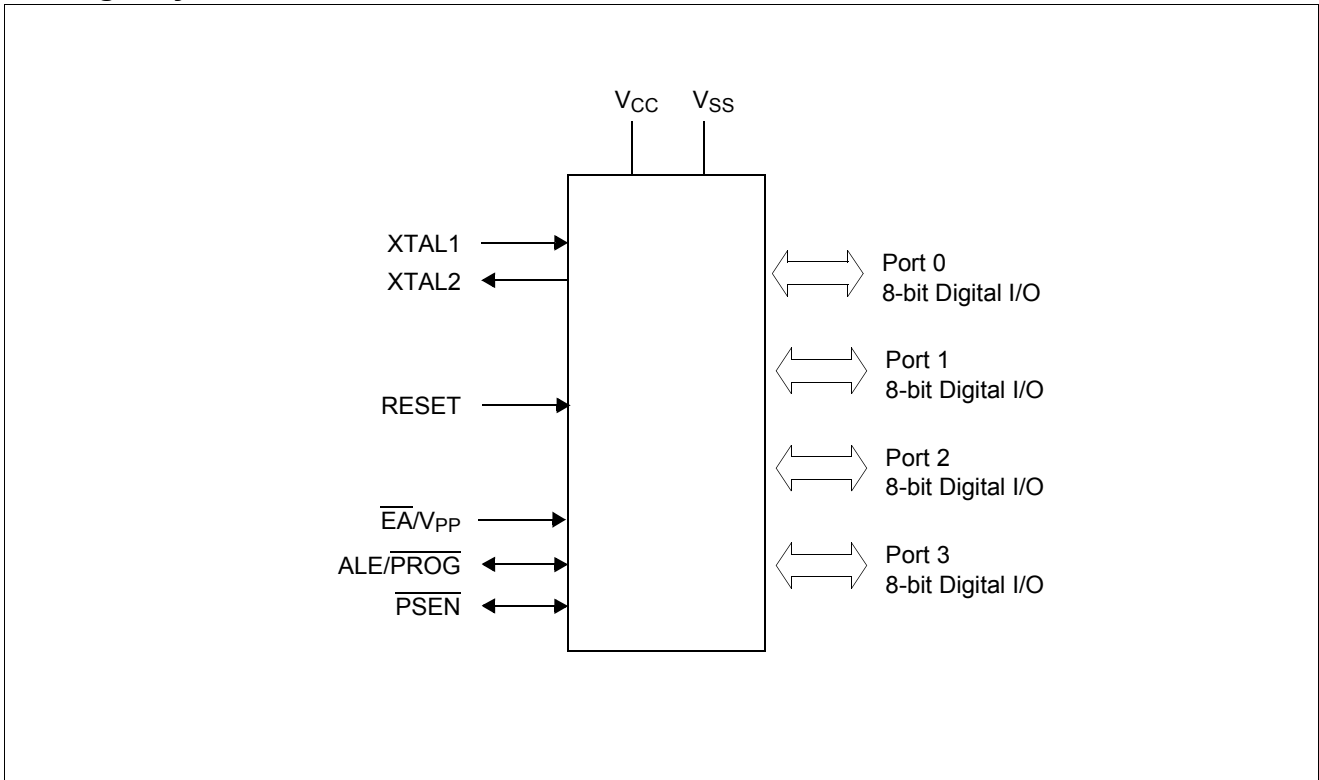


### 1.4 Pin Configuration of 44-MQFP Type

(top view)



## 1.5 Logic Symbol



## 1.6 PIN DEFINITIONS AND FUNCTIONS

| Symbol    | Pin Number   |   |   | Input/<br>Output | Function  |
|-----------|--|---|---|------------------|---|
|           | 44-<br>PLCC  | 40-<br>PDIP   | 44-<br>MQFP   |                  |   |
| P1.0-P1.7 | 2-9<br><br>2<br>3  | 1-8<br><br>1<br>2   | 40-44,<br>1-3<br><br>40<br>41                               | I/O              | <p>Port 1: Port1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have '1' written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (IIL, on the data sheet) because of the internal pull-ups. In addition, Port 1 serves the functions of the following</p> <p>P1.0 : T2 (External Count Input to Timer/ Counter 2),<br/>Clock-Out</p> <p>P1.1 : T2EX (Timer/Counter 2 Capture/ Reload<br/>Trigger and Direction Control</p> <p>Port 1 receives the low-order address bytes during Flash programming and verifying.</p>  |
| P3.0-P3.7 | 11,<br>13-19<br><br>11<br>13<br>14<br>15<br>16<br><br>17<br>18<br>19 | 10-17<br><br>10<br>11<br>12<br>13<br>14<br><br>15<br>16<br>17 | 5, 7-13<br><br>5<br>7<br>8<br>9<br>10<br><br>11<br>12<br>13 | I/O              | <p>Port 3 : Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have '1' written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (IIL, on the data sheet) because of the pullups. Port 3 also serves the functions of various special features of the 8051 Family, as listed below:</p> <p>P3.0 : RXD(serial input port)<br/>P3.1 : TXD(serial output port)<br/>P3.2 : <math>\overline{\text{INT0}}</math>(external interrupt 0)<br/>P3.3 : <math>\overline{\text{INT1}}</math>(external interrupt 1)<br/>P3.4 : T0(Timer 0 external input) &amp; also receives the MSB address byte during flash program, verify, and erase memory algorithm<br/>P3.5 : T1(Timer 1 external input)<br/>P3.6 : <math>\overline{\text{WR}}</math>(external data memory write strobe)<br/>P3.7 : <math>\overline{\text{RD}}</math>(external data memory read strobe)</p> |
| XTAL2     | 20   | 18  | 14  | O                | XTAL2<br>Output of the inverting oscillator amplifier.  |
| XTAL1     | 21   | 19  | 15  | I                | XTAL1 : Input to the inverting oscillator amplifier.  |



| Symbol   | Pin Number  |             |             | Input/<br>Output | Function  |
|--|-------------|-------------|-------------|------------------|---|
|  | 44-<br>PLCC | 40-<br>PDIP | 44-<br>MQFP |                  |   |
| P2.0-P2.7  | 24-31       | 21-28       | 18-25       | I/O              | <p>Port 2 : Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have '1' written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (IIL, on the data sheet) because of the internal pullups.</p> <p>Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting '1'. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.</p> <p>Some Port 2 pins receive the high-order address bits during flash program, verify, and erase memory algorithm</p>   |
| $\overline{\text{PSEN}}$                         | 32          | 29          | 26          | O                | <p><math>\overline{\text{PSEN}}</math> : Program Store Enable is the read strobe to external Program Memory.</p> <p>When the executing code from external Program Memory, <math>\overline{\text{PSEN}}</math> is activated twice each machine cycle, except that two <math>\overline{\text{PSEN}}</math> activations are skipped during each access to external Data Memory.</p>  |
| RESET  | 10          | 9           | 4           | I                | <p>RST : Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum VIH1 voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to VCC.</p>  |
| $\overline{\text{ALE}} / \overline{\text{PROG}}$ | 33          | 30          | 27          | O                | <p>ALE : Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (<math>\overline{\text{ALE}} / \overline{\text{PROG}}</math>) is also the program pulse input during Flash programming.</p> <p>In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.</p> <p>With this bit set, the pin is weakly pulled high.</p> <p>The ALE disable feature will be terminated by reset. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.</p> <p>Throughout the remainder of this data sheet, <math>\overline{\text{ALE}}</math> will refer to the signal coming out of the <math>\overline{\text{ALE}} / \overline{\text{PROG}}</math> pin, and the pin will be referred to as the <math>\overline{\text{ALE}} / \overline{\text{PROG}}</math> pin.</p> |

| Symbol                   | Pin Number    |             |               | Input/<br>Output | Function   |
|--------------------------|---------------|-------------|---------------|------------------|--|
|                          | 44-<br>PLCC   | 40-<br>PDIP | 44-<br>MQFP   |                  |  |
| $\overline{EA} / V_{PP}$ | 35            | 31          | 29            | I                | <p><math>\overline{EA}/V_{PP}</math> : External Access enable. <math>\overline{EA}</math> must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 00000H to 0FFFFH. Note; however, that if any of the Lock bits are programmed, <math>\overline{EA}</math> will be internally latched on reset.</p> <p><math>\overline{EA}</math> should be strapped to VCC for internal program executions.</p> <p>This pin also receives the programming supply voltage (VPP) during Flash programming and erase.</p>   |
| P0.0-P0.7                | 36-43         | 32-39       | 30-37         | I/O              | <p>Port0 : Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have '1' written to then float, and in that state can be used as high impedance inputs.</p> <p>Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting '1'. and can source and sink several LS TTL inputs.</p> <p>Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification.</p> <p>External pullup resistors are required during program verification.</p> |
| VSS                      | 22            | 20          | 16            | -                | Circuit ground potential   |
| VCC                      | 44            | 40          | 38            | -                | Supply terminal for all operating modes  |
| N.C.                     | 1,12<br>23,34 | -           | 6,17<br>28,39 | -                | No connection  |

## Chapter 2. FUNCTIONAL DESCRIPTION

The GMS99C58 ( 8-Bit MCU ) is fully compatible to the standard 8051 microcontroller family.

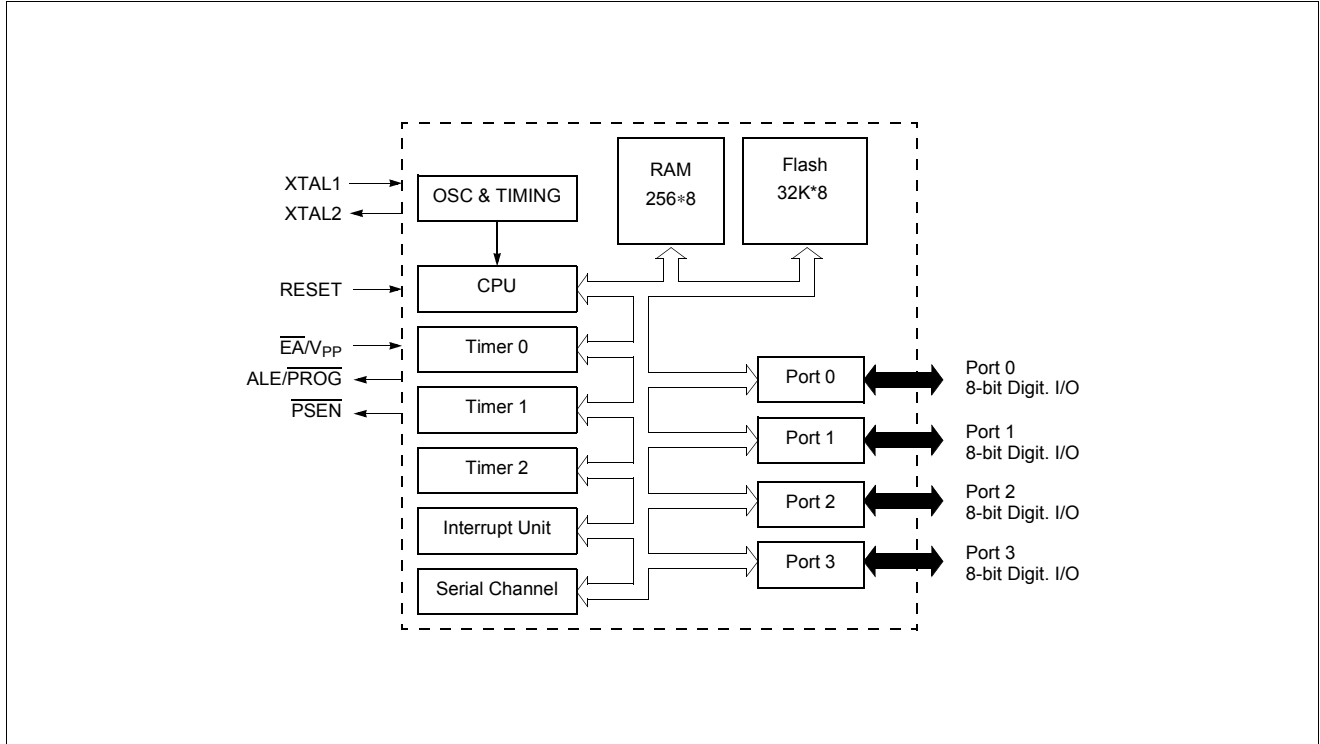
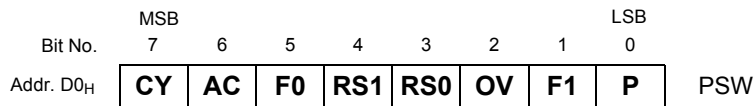


Figure 1. Block Diagram of the GMS99C58

### 2.1 CPU

The GMS99C58 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1.0µs (25MHz: 500ns).

#### 2.1.1 Special Function Register PSW



| Bit       | Function                                  |
|-----------|---|
| <b>CY</b> | Carry Flag                                |
| <b>AC</b> | Auxiliary Carry Flag (for BCD operations) |
| <b>F0</b> | General Purpose Flag                      |

| Bit        |            | Function   |
|------------|------------|--|
| <b>RS1</b> | <b>RS0</b> | Register Bank select control bits  |
| 0          | 0          | Bank 0 selected, data address 00 <sub>H</sub> - 07 <sub>H</sub>  |
| 0          | 1          | Bank 1 selected, data address 08 <sub>H</sub> - 0F <sub>H</sub>  |
| 1          | 0          | Bank 2 selected, data address 10 <sub>H</sub> - 17 <sub>H</sub>  |
| 1          | 1          | Bank 3 selected, data address 18 <sub>H</sub> - 1F <sub>H</sub>  |
| <b>OV</b>  |            | Overflow Flag  |
| <b>F1</b>  |            | General Purpose Flag   |
| <b>P</b>   |            | Parity Flag<br>Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity. |

## 2.2 SPECIAL FUNCTION REGISTERS

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The 27 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in Table 1, Table 2, and Table 3.

In Table 1, they are organized in numeric order of their addresses. In Table 2 they are organized in groups which refer to the functional blocks of the GMS90 Series. Table 3 illustrates the contents of the SFRs.

**Table 1. Special Function Registers in Numeric Order of their Addresses**

| Address    | Register                  | Contents after Reset     | Address    | Register                  | Contents after Reset |
|------------|---------------------------|--------------------------|------------|---------------------------|----------------------|
| <b>80H</b> | <b>P0</b> <sup>1)</sup>   | <b>FFH</b>               | <b>90H</b> | <b>P1</b> <sup>1)</sup>   | <b>FFH</b>           |
| 81H        | SP                        | 07H                      | 91H        | reserved                  | 00H                  |
| 82H        | DPL                       | 00H                      | 92H        | reserved                  | XXH <sup>2)</sup>    |
| 83H        | DPH                       | 00H                      | 93H        | reserved                  | XXH <sup>2)</sup>    |
| 84H        | reserved                  | XXH <sup>2)</sup>        | 94H        | reserved                  | XXH <sup>2)</sup>    |
| 85H        | reserved                  | XXH <sup>2)</sup>        | 95H        | reserved                  | XXH <sup>2)</sup>    |
| 86H        | reserved                  | XXH <sup>2)</sup>        | 96H        | reserved                  | XXH <sup>2)</sup>    |
| 87H        | PCON                      | 0XXX0000B <sup>2)</sup>  | 97H        | reserved                  | XXH <sup>2)</sup>    |
| <b>88H</b> | <b>TCON</b> <sup>1)</sup> | <b>00H</b>               | <b>98H</b> | <b>SCON</b> <sup>1)</sup> | <b>00H</b>           |
| 89H        | TMOD                      | 00H                      | 99H        | SBUF                      | XXH <sup>2)</sup>    |
| 8AH        | TL0                       | 00H                      | 9AH        | reserved                  | XXH <sup>2)</sup>    |
| 8BH        | TL1                       | 00H                      | 9BH        | reserved                  | XXH <sup>2)</sup>    |
| 8CH        | TH0                       | 00H                      | 9CH        | reserved                  | XXH <sup>2)</sup>    |
| 8DH        | TH1                       | 00H                      | 9DH        | reserved                  | XXH <sup>2)</sup>    |
| 8EH        | AUXR0                     | XXXXXXXX0B <sup>2)</sup> | 9EH        | reserved                  | XXH <sup>2)</sup>    |
| 8FH        | reserved                  | XXH <sup>2)</sup>        | 9FH        | reserved                  | XXH <sup>2)</sup>    |

1) Bit-addressable Special Function Register.

2) X means that the value is indeterminate and the location is reserved.

| Address   | Register  | Contents after Reset  | Address   | Register   | Contents after Reset  |
|---|---|---|---|--|---|
| <b>A0H</b><br>A1H<br>A2H<br>A3H<br>A4H<br>A5H<br>A6H<br>A7H | <b>P2</b> <sup>1)</sup><br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved | <b>FFH</b><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup>                     | <b>C8H</b><br>C9H<br>CAH<br>CBH<br>CCH<br>CDH<br>CEH<br>CFH | <b>T2CON</b> <sup>1)</sup><br>T2MOD<br>RC2L<br>RC2H<br>TL2<br>TH2<br>reserved<br>reserved                    | <b>00H</b><br><b>XXXXXX00B</b> <sup>2)</sup><br>00H<br>00H<br>00H<br>00H<br>XXH <sup>2)</sup><br>XXH <sup>2)</sup>  |
| <b>A8H</b><br>A9H<br>AAH<br>ABH<br>ACH<br>ADH<br>AEH<br>AFH | <b>IE</b> <sup>1)</sup><br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved | <b>0X000000B</b> <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup> | <b>D0H</b><br>D1H<br>D2H<br>D3H<br>D4H<br>D5H<br>D6H<br>D7H | <b>PSW</b> <sup>1)</sup><br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved | <b>00H</b><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup>               |
| <b>B0H</b><br>B1H<br>B2H<br>B3H<br>B4H<br>B5H<br>B6H<br>B7H | <b>P3</b> <sup>1)</sup><br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved | <b>FFH</b><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup>                     | <b>D8H</b><br>D9H<br>DAH<br>DBH<br>DCH<br>DDH<br>DEH<br>DFH | reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved                 | XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup>        |
| <b>B8H</b><br>B9H<br>BAH<br>BBH<br>BCH<br>BDH<br>BEH<br>BFH | <b>IP</b> <sup>1)</sup><br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved | <b>XX000000B</b> <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup> | <b>E0H</b><br>E1H<br>E2H<br>E3H<br>E4H<br>E5H<br>E6H<br>E7H | <b>ACC</b> <sup>1)</sup><br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved | <b>00H</b><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup>               |
| <b>C0H</b><br>C1H<br>C2H<br>C3H<br>C4H<br>C5H<br>C6H<br>C7H | reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved                            | <b>XXH</b> <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup>       | <b>E8H</b><br>E9H<br>EAH<br>EBH<br>ECH<br>EDH<br>EEH<br>EFH | reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved<br>reserved                 | <b>XXH</b> <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup><br>XXH <sup>2)</sup> |

| Address    | Register               | Contents after Reset | Address    | Register | Contents after Reset |
|------------|------------------------|----------------------|------------|----------|----------------------|
| <b>F0H</b> | <b>B</b> <sup>1)</sup> | <b>00H</b>           | <b>F8H</b> | reserved | XXH <sup>2)</sup>    |
| F1H        | reserved               | XXH <sup>2)</sup>    | F9H        | reserved | XXH <sup>2)</sup>    |
| F2H        | reserved               | XXH <sup>2)</sup>    | FAH        | reserved | XXH <sup>2)</sup>    |
| F3H        | reserved               | XXH <sup>2)</sup>    | FBH        | reserved | XXH <sup>2)</sup>    |
| F4H        | reserved               | XXH <sup>2)</sup>    | FCH        | reserved | XXH <sup>2)</sup>    |
| F5H        | reserved               | XXH <sup>2)</sup>    | FDH        | reserved | XXH <sup>2)</sup>    |
| F6H        | reserved               | XXH <sup>2)</sup>    | FEH        | reserved | XXH <sup>2)</sup>    |
| F7H        | reserved               | XXH <sup>2)</sup>    | FFH        | reserved | XXH <sup>2)</sup>    |

1) Bit-addressable Special Function Register.

2) X means that the value is indeterminate and the location is reserved.

**Table 2. Special Function Registers - Functional Blocks**

| Block               | Symbol             | Name                                   | Address           | Contents after Reset    |
|---------------------|--------------------|--|-------------------|-------------------------|
| CPU                 | ACC                | Accumulator                            | E0H <sup>1)</sup> | 00H                     |
|                     | B                  | B-Register                             | F0H <sup>1)</sup> | 00H                     |
|                     | DPH                | Data Pointer, High Byte                | 83H               | 00H                     |
|                     | DPL                | Data Pointer, Low Byte                 | 82H               | 00H                     |
|                     | PSW                | Program Status Word Register           | D0H <sup>1)</sup> | 00H                     |
|                     | SP                 | Stack Pointer                          | 81H               | 07H                     |
| Interrupt System    | IE                 | Interrupt Enable Register              | A8H <sup>1)</sup> | 0X000000B <sup>2)</sup> |
|                     | IP                 | Interrupt Priority Register            | B8H <sup>1)</sup> | XX000000B <sup>2)</sup> |
| Ports               | P0                 | Port 0                                 | 80H <sup>1)</sup> | FFH                     |
|                     | P1                 | Port 1                                 | 90H <sup>1)</sup> | XXH                     |
|                     | P2                 | Port 2                                 | A0H <sup>1)</sup> | FFH                     |
|                     | P3                 | Port 3                                 | B0H <sup>1)</sup> | FFH                     |
| Serial Channels     | PCON <sup>3)</sup> | Power Control Register                 | 87H               | 0XXX0000B <sup>2)</sup> |
|                     | SBUF               | Serial Channel Buffer Reg.             | 99H               | XXH <sup>2)</sup>       |
|                     | SCON               | Serial Channel 0 Control Reg.          | 98H <sup>1)</sup> | 00H                     |
| Timer 0/<br>Timer 1 | TCON               | Timer 0/1 Control Register             | 88H <sup>1)</sup> | 00H                     |
|                     | TH0                | Timer 0, High Byte                     | 8CH               | 00H                     |
|                     | TH1                | Timer 1, High Byte                     | 8DH               | 00H                     |
|                     | TL0                | Timer 0, Low Byte                      | 8AH               | 00H                     |
|                     | TL1                | Timer 1, Low Byte                      | 8BH               | 00H                     |
|                     | TMOD               | Timer Mode Register                    | 89H               | 00H                     |
| Timer 2             | T2CON              | Timer 2 Control Register               | C8H <sup>1)</sup> | 00H                     |
|                     | T2MOD              | Timer 2 Mode Register                  | C9H               | 00H                     |
|                     | RC2H               | Timer 2 Reload Capture Reg., High Byte | CBH               | 00H                     |
|                     | RC2L               | Timer 2 Reload Capture Reg., Low Byte  | CAH               | 00H                     |
|                     | TH2                | Timer 2, High Byte                     | CDH               | 00H                     |
|                     | TL2                | Timer 2, Low Byte                      | CCH               | 00H                     |

Table 2. Special Function Registers - Functional Blocks

| Block              | Symbol | Name                   | Address | Contents after Reset     |
|--------------------|--------|------------------------|---------|--------------------------|
| Power Saving Modes | PCON   | Power Control Register | 87H     | 0XXX0000B <sup>2)</sup>  |
| -                  | AUXR0  | Aux. Register 0        | 8EH     | XXXXXXXX0B <sup>2)</sup> |

1) Bit-addressable Special Function register

2) X means that the value is indeterminate and the location is reserved

3) This special function register is listed repeatedly since some bit of it also belong to other functional blocks

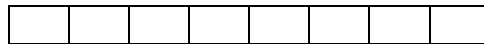
Table 3. Contents of SFRs, SFRs in Numeric Order

| Address | Register | Bit 7 | 6    | 5    | 4    | 3     | 2   | 1    | 0      |
|---------|----------|-------|------|------|------|-------|-----|------|--------|
| 80H     | P0       |       |      |      |      |       |     |      |        |
| 81H     | SP       |       |      |      |      |       |     |      |        |
| 82H     | DPL      |       |      |      |      |       |     |      |        |
| 83H     | DPH      |       |      |      |      |       |     |      |        |
| 87H     | PCON     | SMOD  | -    | -    | -    | GF1   | GF0 | PDE  | IDLE   |
| 88H     | TCON     | TF1   | TR1  | TF0  | TR0  | IE1   | IT1 | IE0  | IT0    |
| 89H     | TMOD     | GATE  | C/T  | M1   | M0   | GATE  | C/T | M1   | M0     |
| 8AH     | TL0      |       |      |      |      |       |     |      |        |
| 8BH     | TL1      |       |      |      |      |       |     |      |        |
| 8CH     | TH0      |       |      |      |      |       |     |      |        |
| 8DH     | TH1      |       |      |      |      |       |     |      |        |
| 8EH     | AUXR0    | -     | -    | -    | -    | -     | -   | -    | A0     |
| 90H     | P1       |       |      |      |      |       |     |      |        |
| 98H     | SCON     | SM0   | SM1  | SM2  | REN  | TB8   | RB8 | TI   | RI     |
| 99H     | SBUF     |       |      |      |      |       |     |      |        |
| A0H     | P2       |       |      |      |      |       |     |      |        |
| A8H     | IE       | EA    | -    | ET2  | ES   | ET1   | EX1 | ET0  | EX0    |
| B0H     | P3       |       |      |      |      |       |     |      |        |
| B8H     | IP       | -     | -    | PT2  | PS   | PT1   | PX1 | PT0  | PX0    |
| C8H     | T2CON    | TF2   | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/T2 | CP/RL2 |

| Address | Register | Bit 7 | 6  | 5  | 4   | 3   | 2  | 1    | 0    |
|---------|----------|-------|----|----|-----|-----|----|------|------|
| C9H     | T2MOD    | -     | -  | -  | -   | -   | -  | T2OE | DCEN |
| CAH     | RC2L     |       |    |    |     |     |    |      |      |
| CBH     | RC2H     |       |    |    |     |     |    |      |      |
| CCH     | TL2      |       |    |    |     |     |    |      |      |
| CDH     | TH2      |       |    |    |     |     |    |      |      |
| D0H     | PSW      | CY    | AC | F0 | RS1 | RS0 | OV | F1   | P    |
| E0H     | ACC      |       |    |    |     |     |    |      |      |
| F0H     | B        |       |    |    |     |     |    |      |      |



SFR bit and byte addressable



SFR not bit addressable

- : this bit location is reserved

### 2.3 TIMER / COUNTER 0 AND 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in Table 4.

Table 4. TIMER / COUNTER 0 AND 1 Operating Modes .

| Mode | Description  | TMOD |     |    |    | Input Clock                   |                               |
|------|--|------|-----|----|----|-------------------------------|-------------------------------|
|      |  | Gate | C/T | M1 | M0 | internal                      | external (Max.)               |
| 0    | 8-bit timer/counter with a divide-by-32 prescaler                                | X    | X   | 0  | 0  | $f_{osc} \div (12 \times 32)$ | $f_{osc} \div (24 \times 32)$ |
| 1    | 16-bit timer/counter   | X    | X   | 0  | 1  | $f_{osc} \div 12$             | $f_{osc} \div 24$             |
| 2    | 16-bit timer/counter with 8-bit auto-reload                                      | X    | X   | 1  | 0  | $f_{osc} \div 12$             | $f_{osc} \div 24$             |
| 3    | Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stop | X    | X   | 1  | 1  | $f_{osc} \div 12$             | $f_{osc} \div 24$             |



In the "timer" function ( $C/\overline{T} = "0"$ ) the register is incremented every machine cycle. Therefore the count rate is  $f_{OSC}/12$ . In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is  $f_{OSC}/24$ . External inputs  $\overline{INT0}$  and  $\overline{INT1}$  (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. Figure 2 illustrates the input clock logic.

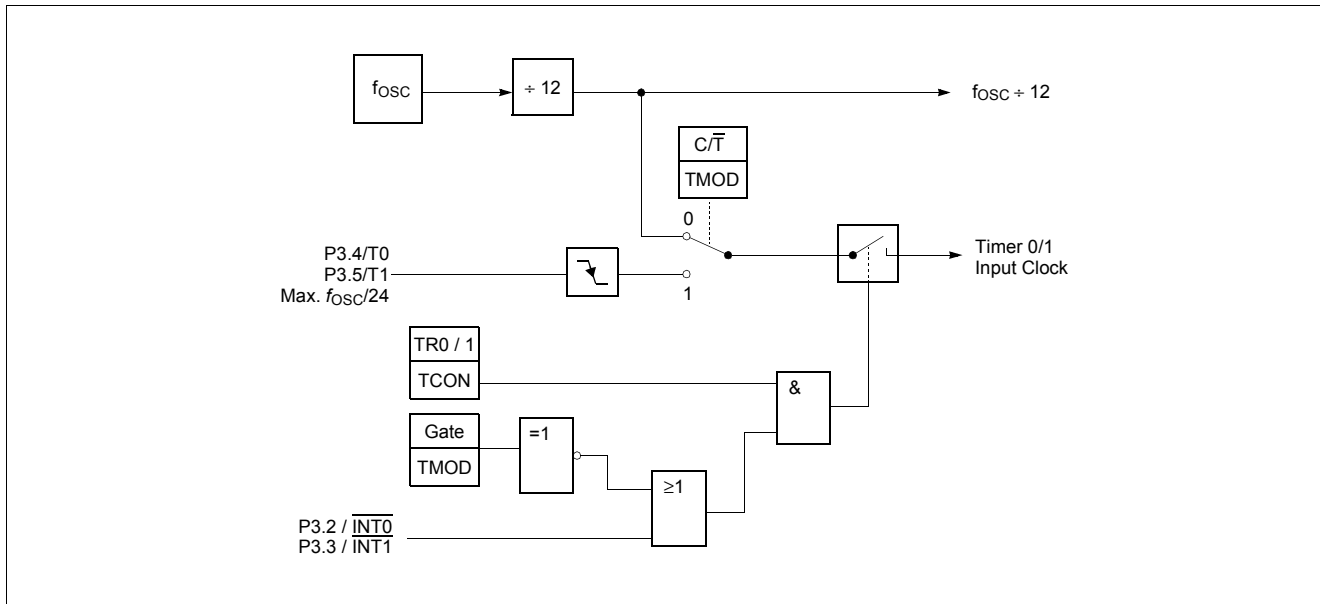


Figure 2. Timer/Counter 0 and 1 Input Clock Logic

## 2.4 TIMER 2

Timer 2 is a 16-bit timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit  $C/\overline{T2}$  (T2CON.1). It has three operating modes as shown in Table 5.

Table 5. Timer/Counter2 Operating Modes.

| Mode                      | T2CON              |            |     | T2 MOD | T2CON | P1.1/<br>T2EX | Remarks  | Input Clock       |                           |
|---------------------------|--------------------|------------|-----|--------|-------|---------------|--|-------------------|---------------------------|
|                           | RCLK<br>or<br>TCLK | CP/<br>RL2 | TR2 | DCEN   | EXEN2 |               |  | internal          | external<br>(P1.0/T2)     |
| 16-bit<br>Auto-<br>Reload | 0                  | 0          | 1   | 0      | 0     | X             | reload upon over-<br>flow reload trig-<br>ger (falling edge)<br>Down counting<br>Up counting | $f_{OSC} \div 12$ | Max.<br>$f_{OSC} \div 24$ |
|                           | 0                  | 0          | 1   | 0      | 1     | ↓             |  |                   |                           |
|                           | 0                  | 0          | 1   | 1      | X     | 0             |  |                   |                           |
|                           | 0                  | 0          | 1   | 1      | X     | 1             |  |                   |                           |
| 16-bit<br>Capture         | 0                  | 1          | 1   | X      | 0     | X             | 16 bit Timer/<br>Counter (only up-<br>counting)<br>capture TH2,TL2<br>→ RC2H,RC2L            | $f_{OSC} \div 12$ | Max.<br>$f_{OSC} \div 24$ |
|                           | 0                  | 1          | 1   | X      | 1     | ↓             |  |                   |                           |

| Mode                      | T2CON              |            |     | T2 MOD | T2CON | P1.1/<br>T2EX | Remarks   | Input Clock           |                               |
|---------------------------|--------------------|------------|-----|--------|-------|---------------|---|-----------------------|-------------------------------|
|                           | RCLK<br>or<br>TCLK | CP/<br>RL2 | TR2 | DCEN   | EXEN2 |               |   | internal              | external<br>(P1.0/T2)         |
| Baud<br>Rate<br>Generator | 1                  | X          | 1   | 0      | 0     | X             | no overflow<br>interrupt request<br>(TF2)<br>extra external<br>interrupt<br>("Timer 2") | f <sub>osc</sub> ÷ 12 | Max.<br>f <sub>osc</sub> ÷ 24 |
|                           | 1                  | X          | 1   | 1      | 1     | ↓             |   |                       |                               |
| Off                       | X                  | X          | 0   | X      | X     | X             | Timer 2 stops   | -                     | -                             |

Note: ↓ = falling edge

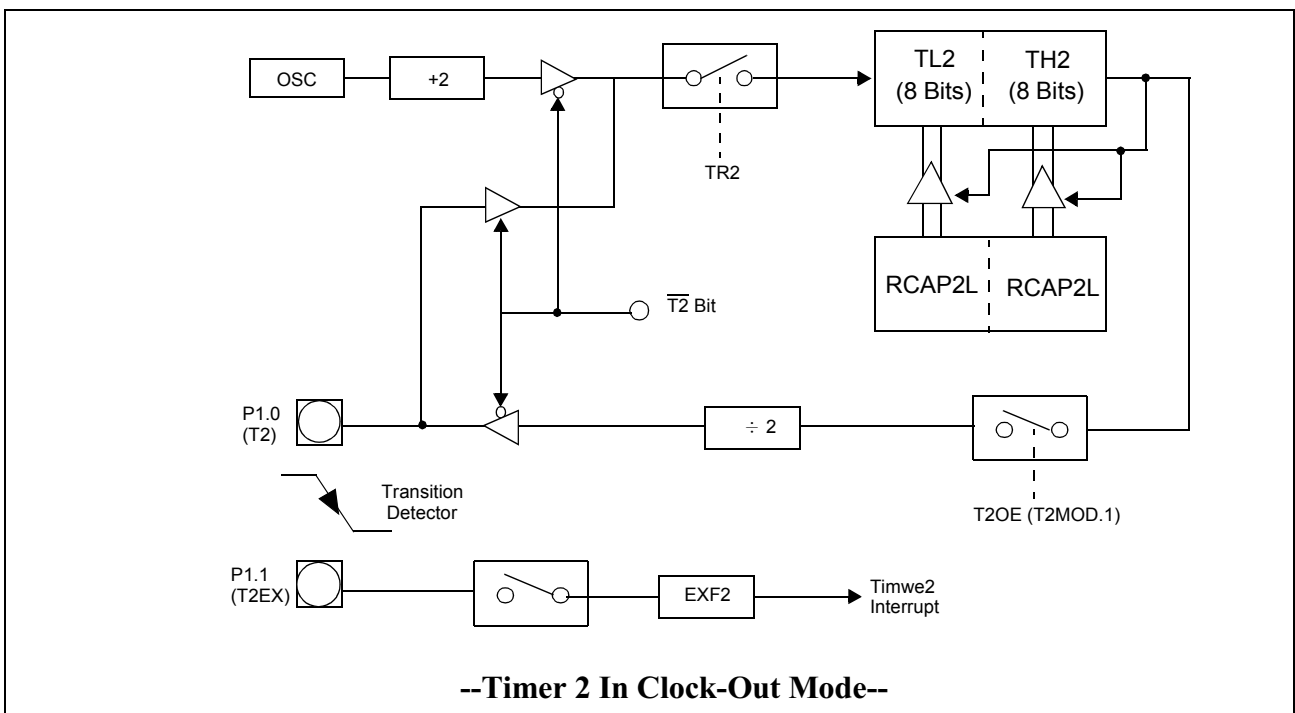
**\*PROGRAMMABLE CLOCK OUT**

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. To configure the Timer/Counter 2 as a clock generator, C/T2 (T2CON.1) must be cleared and bit T2OE(T1MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, TCAP2L) as shown in this equation:

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H}, \text{RCAP2L})}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies can not be determined independently from one another since they both use RCAP2H and RCAP2L.



## 2.5 SERIAL INTERFACE (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in Table 6. The possible baud rates can be calculated using the formulas given in Table 7.

**Table 6. USART Operating Modes**

| Mode | SCON |     | Baudrate                                     | Description   |
|------|------|-----|--|---|
|      | SM0  | SM1 |  |   |
| 0    | 0    | 0   | $\frac{f_{OSC}}{12}$                         | Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first) |
| 1    | 0    | 1   | Timer 1/2 overflow rate                      | 8-bit UART<br>10 bits are transmitted (through TxD) or received (RxD)   |
| 2    | 1    | 0   | $\frac{f_{OSC}}{32}$ or $\frac{f_{OSC}}{64}$ | 9-bit UART<br>11 bits are transmitted (TxD) or received (RxD)   |
| 3    | 1    | 1   | Timer 1/2 overflow rate                      | 9-bit UART<br>Like mode 2 except the variable baud rate   |

**Table 7. Formulas for calculating Baud rates**

| Baud Rate derived from   | Interface Mode | Baudrate   |
|--|----------------|--|
| Oscillator   | 0              | $\frac{f_{OSC}}{12}$   |
|  | 2              | $\frac{2^{SMOD}}{64} \times f_{OSC}$                                 |
| Timer 1 (16-bit timer)<br>(8-bit timer with 8-bit auto reload) | 1,3            | $\frac{2^{SMOD}}{32} \times (Timer\ 1\ overflow)$                    |
|  | 1,3            | $\frac{2^{SMOD}}{32} \times \frac{f_{OSC}}{12 \times [256 - (TH1)]}$ |
| Timer 2  | 1,3            | $\frac{f_{OSC}}{32 \times [65536 - (RC2H, RC2L)]}$                   |

### 2.6 INTERRUPT SYSTEM

The GMS99C58 provides 6 interrupt sources with two priority levels. Figure 3 gives a general overview of the interrupt sources and illustrates the request and control flags.

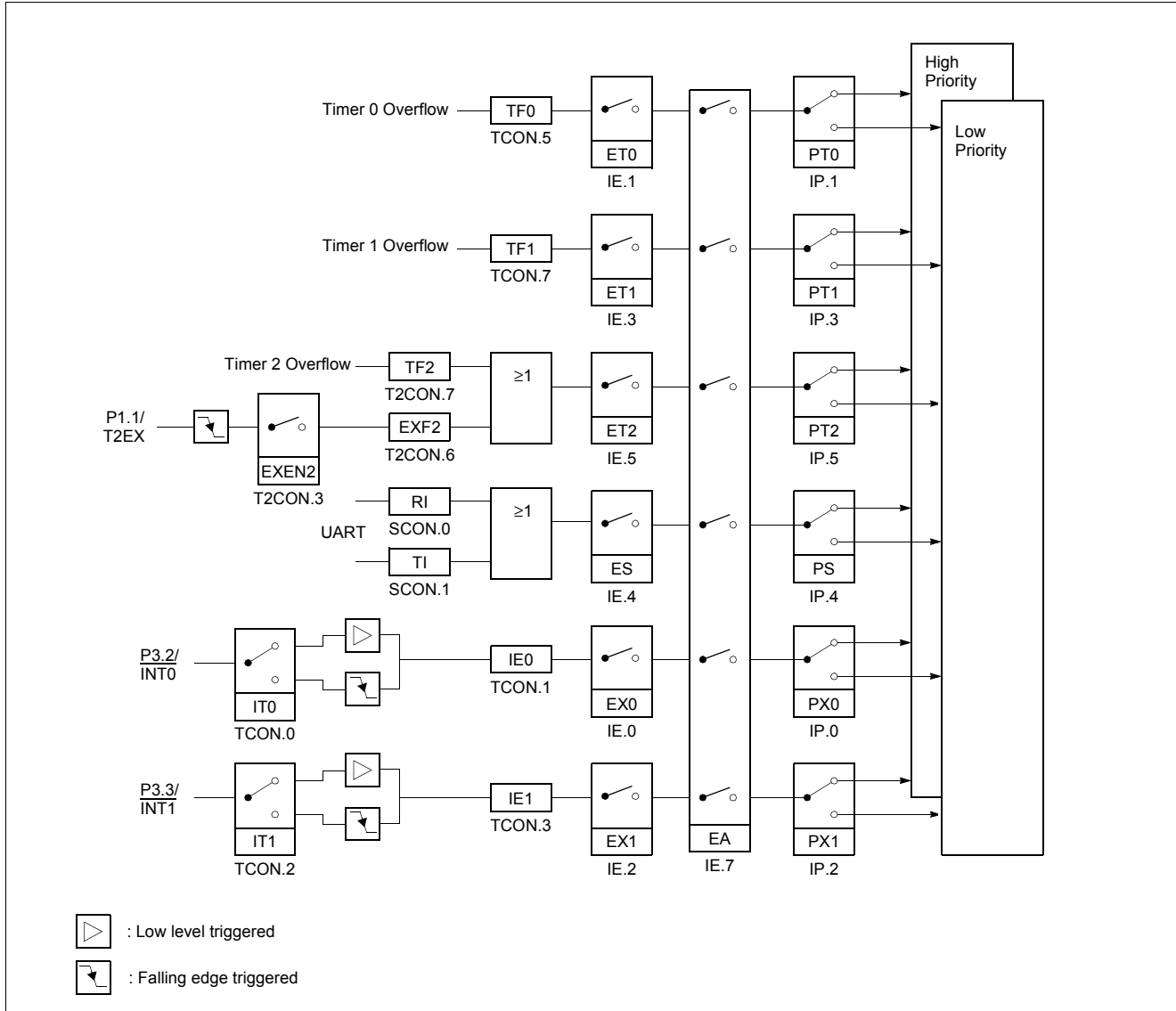


Figure 3. Interrupt Structure

Table 8. Interrupt Sources and their corresponding interrupt vectors

| Source (Request Flags) | Vectors               | Vector Address |
|------------------------|-----------------------|----------------|
| RESET                  | RESET                 | 0000H          |
| IE0                    | External interrupt 0  | 0003H          |
| TF0                    | Timer 0 interrupt     | 000BH          |
| IE1                    | External interrupt 1  | 0013H          |
| TF1                    | Timer 1 interrupt     | 001BH          |
| RI + TI                | Serial port interrupt | 0023H          |
| TF2 + EXF2             | Timer 2 interrupt     | 002BH          |

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in Table 9.

**Table 9. Interrupt Priority-Within-Level**

| Interrupt Source     |            | Priority |
|----------------------|------------|----------|
| External Interrupt 0 | IE0        | High     |
| Timer 0 Interrupt    | TF0        | ↓        |
| External Interrupt 1 | IE1        | ↓        |
| Timer 1 Interrupt    | TF1        | ↓        |
| Serial Channel       | RI + TI    | ↓        |
| Timer 2 Interrupt    | TF2 + EXF2 | Low      |

## 2.7 Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. Table 10 gives a general overview of the power saving modes.

**Table 10. Power Saving Modes Overview**

| Mode            | Entering Instruction Example | Leaving by                            | Remarks   |
|-----------------|------------------------------|---------------------------------------|---|
| Idle mode       | ORL PCON, #01H               | Enabled interrupt.<br>Hardware Reset. | CPU is gated off.<br>CPU status registers maintain their data.<br>Peripherals are active.   |
| Power-Down mode | ORL PCON, #02H               | Hardware Reset                        | Oscillator is stopped, contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR contents). |

In the Power Down mode of operation,  $V_{CC}$  can be reduced to minimize power consumption. It must be ensured, however, that  $V_{CC}$  is not reduced before the Power Down mode is invoked, and that  $V_{CC}$  is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before  $V_{CC}$  is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

## Chapter 3. ELECTRICAL CHARACTERISTICS

### 3.1 Absolute Maximum Ratings

|  |                          |
|--|--------------------------|
| Ambient temperature under bias ( $T_A$ ).....                      | -40 to + 85 °C           |
| Storage temperature ( $T_{ST}$ ).....                              | -65 to + 150 °C          |
| Voltage on $V_{CC}$ pins with respect to ground ( $V_{SS}$ ) ..... | -0.5V to 6.5V            |
| Voltage on any pin with respect to ground ( $V_{SS}$ ).....        | -0.5V to $V_{CC} + 0.5V$ |
| Input current on any pin during overload condition.....            | -10mA to +10mA           |
| Absolute sum of all input currents during overload condition ..... | 100mA                    |
| Power dissipation.....   | TBD                      |

**Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ( $V_{IN} > V_{CC}$  or  $V_{IN} < V_{SS}$ ) the Voltage on  $V_{CC}$  pins with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the absolute maximum ratings.

### 3.2 DC Characteristics (5V Version)

$V_{CC} = 5V \pm 10\%$ ;  $V_{SS} = 0V$ ;  $T_A = 0^\circ C$  to  $70^\circ C$

| Parameter  | Symbol    | Limit Values       |                   | Unit    | Test Conditions   |
|--|-----------|--------------------|-------------------|---------|---|
|  |           | Min.               | Max.              |         |   |
| Input low voltage (except $\overline{EA}$ , RESET)                         | $V_{IL}$  | -0.5               | $0.2V_{CC} - 0.1$ | V       | -   |
| Input low voltage ( $\overline{EA}$ )                                      | $V_{IL1}$ | -0.5               | $0.1V_{CC} - 0.1$ | V       | -   |
| Input low voltage (RESET)  | $V_{IL2}$ | -0.5               | $0.2V_{CC} + 0.1$ | V       | -   |
| Input high voltage (except XTAL1, $\overline{EA}$ , RESET)                 | $V_{IH}$  | $0.2V_{CC} + 0.9$  | $V_{CC} + 0.5$    | V       | -   |
| Input high voltage to XTAL1  | $V_{IH1}$ | $0.7V_{CC}$        | $V_{CC} + 0.5$    | V       | -   |
| Input high voltage to $\overline{EA}$ , RESET                              | $V_{IH2}$ | $0.6V_{CC}$        | $V_{CC} + 0.5$    | V       | -   |
| Output low voltage (ports 1, 2, 3)   | $V_{OL}$  | -                  | 0.45              | V       | $I_{OL} = 1.6mA$ <sup>1)</sup>  |
| Output low voltage (port 0, ALE, $\overline{PSEN}$ )                       | $V_{OL1}$ | -                  | 0.45              | V       | $I_{OL} = 3.2mA$ <sup>1)</sup>  |
| Output high voltage (ports 1, 2, 3)  | $V_{OH}$  | 2.4<br>$0.9V_{CC}$ | -                 | V       | $I_{OH} = -80\mu A$<br>$I_{OH} = -10\mu A$                              |
| Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$ ) | $V_{OH1}$ | 2.4<br>$0.9V_{CC}$ | -<br>-            | V       | $I_{OH} = -800\mu A$ <sup>2)</sup><br>$I_{OH} = -80\mu A$ <sup>2)</sup> |
| Logic 0 input current (ports 1, 2, 3)                                      | $I_{IL}$  | -10                | -50               | $\mu A$ | $V_{IN} = 0.45V$  |

| Parameter   | Symbol       | Limit Values |         | Unit    | Test Conditions                    |
|---|--------------|--------------|---------|---------|------------------------------------|
|   |              | Min.         | Max.    |         |                                    |
| Logical 1-to-0 transition current (ports 1, 2, 3) | $I_{TL}$     | -65          | -650    | $\mu A$ | $V_{IN} = 2.0V$                    |
| Input leakage current (port 0, $\overline{EA}$ )  | $I_{LI}$     | -            | $\pm 1$ | $\mu A$ | $0.45 < V_{IN} < V_{CC}$           |
| Pin capacitance                                   | $C_{IO}$     | -            | 10      | pF      | $f_C = 1MHz$<br>$T_A = 25^\circ C$ |
| <b>Power supply current:</b>                      |              |              |         |         |                                    |
| Active mode, 12MHz <sup>3)</sup>                  | $I_{CC12}$   | -            | 21      | mA      | $V_{CC} = 5V$ <sup>4)</sup>        |
| Idle mode, 12MHz <sup>3)</sup>                    | $I_{idle12}$ | -            | 18      | mA      | $V_{CC} = 5V$ <sup>5)</sup>        |
| Active mode, 24 MHz <sup>3)</sup>                 | $I_{CC24}$   | -            | 36      | mA      | $V_{CC} = 5V$                      |
| Idle mode, 24MHz <sup>3)</sup>                    | $I_{idle24}$ | -            | 20      | mA      | $V_{CC} = 5V$                      |
| Power Down Mode <sup>3)</sup>                     | $I_{PD}$     | -            | 50      | $\mu A$ | $V_{CC} = 5V$ <sup>6)</sup>        |

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$  of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading  $> 100pF$ ), the noise pulse on ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and  $\overline{PSEN}$  to momentarily fall below the  $0.9V_{CC}$  specification when the address lines are stabilizing.
- 3)  $I_{CC}$  Max at other frequencies is given by:  
active mode:  $I_{CC} = 1.27 \times f_{OSC} + 5.73$   
idle mode:  $I_{CC} = 0.28 \times f_{OSC} + 1.45$ .  
where  $f_{OSC}$  is the oscillator frequency in MHz.  $I_{CC}$  values are given in mA and measured at  $V_{CC} = 5V$ .
- 4)  $I_{CC}$  (active mode) is measured with:  
XTAL1 driven with  $t_{CLCH}, t_{CHCL} = 5ns$ ,  $V_{IL} = V_{SS} + 0.5V$ ,  $V_{IH} = V_{CC} - 0.5V$ ; XTAL2 = N.C.;  
 $\overline{EA} = \text{Port0} = \text{RESET} = V_{CC}$ ; all other pins are disconnected.  $I_{CC}$  would be slightly higher if a crystal oscillator is used (appr. 1mA).
- 5)  $I_{CC}$  (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;  
XTAL1 driven with  $t_{CLCH}, t_{CHCL} = 5ns$ ,  $V_{IL} = V_{SS} + 0.5V$ ,  $V_{IH} = V_{CC} - 0.5V$ ; XTAL2 = N.C.;  
 $\text{RESET} = \overline{EA} = V_{SS}$ ;  $\text{Port0} = V_{CC}$ ; all other pins are disconnected;
- 6)  $I_{PD}$  (Power Down Mode) is measured under following conditions:  
 $\overline{EA} = \text{Port0} = V_{CC}$ ;  $\text{RESET} = V_{SS}$ ; XTAL2 = N.C.; XTAL1 =  $V_{SS}$ ; all other pins are disconnected.

### 3.3 AC Characteristics

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a 't' (stand for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address  
 C: Clock  
 D: Input Data  
 H: Logic level HIGH  
 I: Instruction (program memory contents)  
 L: Logic level LOW, or ALE  
 P: PSEN  
 Q: Output Data  
 R: RD signal

T: Time  
 V: Valid  
 W: WR signal  
 X: No longer a valid logic level  
 Z: Float

For example,  
 $t_{AVLL}$  = Time from Address Valid to ALE Low  
 $t_{LLPL}$  = Time from ALE Low to PSEN Low

#### 3.3.1 For $f_{osc}=3.5\text{MHz} \sim 12\text{MHz}$

$V_{CC}=5V \pm 10\%$ ;  $V_{SS}=0V$ ;  $T_A=0^\circ\text{C}$  to  $70^\circ\text{C}$

( $C_L$  for port 0, ALE and  $\overline{\text{PSEN}}$  outputs = 100pF;  $C_L$  for all other outputs = 80pF)

**Table 11. Program Memory Characteristics**

| Parameter  | Symbol             | 12 MHz Oscillator |      | Variable Oscillator<br>1/ $t_{CLCL}$ = 3.5 to 12MHz |                 | Unit |
|--|--------------------|-------------------|------|---|-----------------|------|
|  |                    | Min.              | Max. | Min.  | Max.            |      |
| ALE pulse width  | $t_{LHLL}$         | 127               | -    | $2t_{CLCL}-40$                                      | -               | ns   |
| Address setup to ALE                                   | $t_{AVLL}$         | 43                | -    | $t_{CLCL}-40$                                       | -               | ns   |
| Address hold after ALE                                 | $t_{LLAX}$         | 30                | -    | $t_{CLCL}-53$                                       | -               | ns   |
| ALE low to valid instruction in                        | $t_{LLIV}$         | -                 | 233  | -   | $4t_{CLCL}-100$ | ns   |
| ALE to $\overline{\text{PSEN}}$                        | $t_{LLPL}$         | 58                | -    | $t_{CLCL}-25$                                       | -               | ns   |
| $\overline{\text{PSEN}}$ pulse width                   | $t_{PLPH}$         | 215               | -    | $3t_{CLCL}-35$                                      | -               | ns   |
| $\overline{\text{PSEN}}$ to valid instruction in       | $t_{PLIV}$         | -                 | 150  | -   | $3t_{CLCL}-100$ | ns   |
| Input instruction hold after $\overline{\text{PSEN}}$  | $t_{PXIX}$         | 0                 | -    | 0   | -               | ns   |
| Input instruction float after $\overline{\text{PSEN}}$ | $t_{PXIZ}^\dagger$ | -                 | 63   | -   | $t_{CLCL}-20$   | ns   |
| Address valid after $\overline{\text{PSEN}}$           | $t_{PXAV}^\dagger$ | 75                | -    | $t_{CLCL}-8$  | -               | ns   |
| Address to valid instruction in                        | $t_{AVIV}$         | -                 | 302  | -   | $5t_{CLCL}-115$ | ns   |
| Address float to $\overline{\text{PSEN}}$              | $t_{AZPL}$         | 0                 | -    | 0   | -               | ns   |

$^\dagger$  Interfacing the GMS99C58 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.



Table 12. External Data Memory Characteristics

| Parameter   | Symbol             | 12 MHz Oscillator |      | Variable Oscillator<br>1/t <sub>CLCL</sub> = 3.5 to 12MHz |                         | Unit |
|---|--------------------|-------------------|------|---|-------------------------|------|
|   |                    | Min.              | Max. | Min.  | Max.                    |      |
| $\overline{RD}$ pulse width                         | t <sub>RLRH</sub>  | 400               | -    | 6t <sub>CLCL</sub> -100                                   | -                       | ns   |
| $\overline{WR}$ pulse width                         | t <sub>WLWH</sub>  | 400               | -    | 6t <sub>CLCL</sub> -100                                   | -                       | ns   |
| Address hold after ALE                              | t <sub>LLAX2</sub> | 30                | -    | t <sub>CLCL</sub> -53                                     | -                       | ns   |
| $\overline{RD}$ to valid data in                    | t <sub>RLDV</sub>  | -                 | 252  | -   | 5t <sub>CLCL</sub> -165 | ns   |
| Data hold after $\overline{RD}$                     | t <sub>RHDX</sub>  | 0                 | -    | 0   | -                       | ns   |
| Data float after $\overline{RD}$                    | t <sub>RHDZ</sub>  | -                 | 97   | -   | 2t <sub>CLCL</sub> -70  | ns   |
| ALE to valid data in                                | t <sub>LLDV</sub>  | -                 | 517  | -   | 8t <sub>CLCL</sub> -150 | ns   |
| Address to valid data in                            | t <sub>AVDV</sub>  | -                 | 583  | -   | 9t <sub>CLCL</sub> -165 | ns   |
| ALE to $\overline{WR}$ or $\overline{RD}$           | t <sub>LLWL</sub>  | 200               | 300  | 3t <sub>CLCL</sub> -50                                    | 3t <sub>CLCL</sub> +50  | ns   |
| Address valid to $\overline{WR}$ or $\overline{RD}$ | t <sub>AVWL</sub>  | 203               | -    | 4t <sub>CLCL</sub> -130                                   | -                       | ns   |
| $\overline{WR}$ or $\overline{RD}$ high to ALE high | t <sub>WHLH</sub>  | 43                | 123  | t <sub>CLCL</sub> -40                                     | t <sub>CLCL</sub> +40   | ns   |
| Data valid to $\overline{WR}$ transition            | t <sub>QVWX</sub>  | 33                | -    | t <sub>CLCL</sub> -50                                     | -                       | ns   |
| Data setup before $\overline{WR}$                   | t <sub>QVWH</sub>  | 433               | -    | 7t <sub>CLCL</sub> -150                                   | -                       | ns   |
| Data hold after $\overline{WR}$                     | t <sub>WHQX</sub>  | 33                | -    | t <sub>CLCL</sub> -50                                     | -                       | ns   |
| Address float after $\overline{RD}$                 | t <sub>RLAZ</sub>  | -                 | 0    | -   | 0                       | ns   |

Table 13. External Clock Drive

| Parameter         | Symbol            | Variable Oscillator<br>(Freq. = 3.5 to 12MHz) |                                       | Unit |
|-------------------|-------------------|---|---------------------------------------|------|
|                   |                   | Min.  | Max.                                  |      |
| Oscillator period | t <sub>CLCL</sub> | 83.3  | 285.7                                 | ns   |
| High time         | t <sub>CHCX</sub> | 20  | t <sub>CLCL</sub> - t <sub>CLCX</sub> | ns   |
| Low time          | t <sub>CLCX</sub> | 20  | t <sub>CLCL</sub> - t <sub>CHCX</sub> | ns   |
| Rise time         | t <sub>CLCH</sub> | -   | 20                                    | ns   |
| Fall time         | t <sub>CHCL</sub> | -   | 20                                    | ns   |

### 3.3.2 for $f_{osc}=3.5\text{MHz} \sim 24\text{MHz}$

$V_{CC}=5V \pm 10\%$ ;  $V_{SS}=0V$ ;  $T_A=0^\circ\text{C}$  to  $70^\circ\text{C}$

( $C_L$  for port 0, ALE and  $\overline{\text{PSEN}}$  outputs = 100pF;  $C_L$  for all other outputs = 80pF)

**Table 14. Program Memory Characteristics**

| Parameter  | Symbol             | 24 MHz Oscillator |      | Variable Oscillator<br>1/ $t_{CLCL}$ = 3.5 to 24MHz |                | Unit |
|--|--------------------|-------------------|------|---|----------------|------|
|  |                    | Min.              | Max. | Min.  | Max.           |      |
| ALE pulse width  | $t_{LHLL}$         | 43                | -    | $2t_{CLCL}-40$                                      | -              | ns   |
| Address setup to ALE                                   | $t_{AVLL}$         | 17                | -    | $t_{CLCL}-25$                                       | -              | ns   |
| Address hold after ALE                                 | $t_{LLAX}$         | 17                | -    | $t_{CLCL}-25$                                       | -              | ns   |
| ALE low to valid instruction in                        | $t_{LLIV}$         | -                 | 80   | -   | $4t_{CLCL}-87$ | ns   |
| ALE to $\overline{\text{PSEN}}$                        | $t_{LLPL}$         | 22                | -    | $t_{CLCL}-20$                                       | -              | ns   |
| $\overline{\text{PSEN}}$ pulse width                   | $t_{PLPH}$         | 95                | -    | $3t_{CLCL}-30$                                      | -              | ns   |
| $\overline{\text{PSEN}}$ to valid instruction in       | $t_{PLIV}$         | -                 | 60   | -   | $3t_{CLCL}-65$ | ns   |
| Input instruction hold after $\overline{\text{PSEN}}$  | $t_{PXIX}$         | 0                 | -    | 0   | -              | ns   |
| Input instruction float after $\overline{\text{PSEN}}$ | $t_{PXIZ}^\dagger$ | -                 | 32   | -   | $t_{CLCL}-20$  | ns   |
| Address valid after $\overline{\text{PSEN}}$           | $t_{PXAV}^\dagger$ | 75                | -    | $t_{CLCL}-5$  | -              | ns   |
| Address to valid instruction in                        | $t_{AVIV}$         | -                 | 148  | -   | $5t_{CLCL}-60$ | ns   |
| Address float to $\overline{\text{PSEN}}$              | $t_{AZPL}$         | 0                 | -    | 0   | -              | ns   |

$^\dagger$  Interfacing the GMS99C58 to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

**Table 15. External Data Memory Characteristics**

| Parameter   | Symbol      | 24 MHz Oscillator |      | Variable Oscillator<br>1/ $t_{CLCL}$ = 3.5 to 24MHz |                 | Unit |
|---|-------------|-------------------|------|---|-----------------|------|
|   |             | Min.              | Max. | Min.  | Max.            |      |
| $\overline{\text{RD}}$ pulse width                      | $t_{RLRH}$  | 180               | -    | $6t_{CLCL}-70$                                      | -               | ns   |
| $\overline{\text{WR}}$ pulse width                      | $t_{WLWH}$  | 180               | -    | $6t_{CLCL}-70$                                      | -               | ns   |
| Address hold after ALE                                  | $t_{LLAX2}$ | 15                | -    | $t_{CLCL}-27$                                       | -               | ns   |
| $\overline{\text{RD}}$ to valid data in                 | $t_{RLDV}$  | -                 | 118  | -   | $5t_{CLCL}-90$  | ns   |
| Data hold after $\overline{\text{RD}}$                  | $t_{RHDX}$  | 0                 | -    | 0   | -               | ns   |
| Data float after $\overline{\text{RD}}$                 | $t_{RHDZ}$  | -                 | 63   | -   | $2t_{CLCL}-20$  | ns   |
| ALE to valid data in                                    | $t_{LLDV}$  | -                 | 200  | -   | $8t_{CLCL}-133$ | ns   |
| Address to valid data in                                | $t_{AVDV}$  | -                 | 220  | -   | $9t_{CLCL}-155$ | ns   |
| ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$ | $t_{LLWL}$  | 75                | 175  | $3t_{CLCL}-50$                                      | $3t_{CLCL}+50$  | ns   |

| Parameter   | Symbol            | 24 MHz Oscillator |      | Variable Oscillator<br>1/t <sub>CLCL</sub> = 3.5 to 24MHz |                       | Unit |
|---|-------------------|-------------------|------|---|-----------------------|------|
|   |                   | Min.              | Max. | Min.  | Max.                  |      |
| Address valid to $\overline{WR}$ or $\overline{RD}$ | t <sub>AVWL</sub> | 67                | -    | 4t <sub>CLCL</sub> -97                                    | -                     | ns   |
| $\overline{WR}$ or $\overline{RD}$ high to ALE high | t <sub>WHLH</sub> | 17                | 67   | t <sub>CLCL</sub> -25                                     | t <sub>CLCL</sub> +25 | ns   |
| Data valid to $\overline{WR}$ transition            | t <sub>QVWX</sub> | 5                 | -    | t <sub>CLCL</sub> -37                                     | -                     | ns   |
| Data setup before $\overline{WR}$                   | t <sub>QVWH</sub> | 170               | -    | 7t <sub>CLCL</sub> -122                                   | -                     | ns   |
| Data hold after $\overline{WR}$                     | t <sub>WHQX</sub> | 15                | -    | t <sub>CLCL</sub> -27                                     | -                     | ns   |
| Address float after $\overline{RD}$                 | t <sub>RLAZ</sub> | -                 | 0    | -   | 0                     | ns   |

Table 16. External Clock Drive

| Parameter         | Symbol            | Variable Oscillator<br>(Freq. = 3.5 to 24MHz) |                                       | Unit |
|-------------------|-------------------|---|---------------------------------------|------|
|                   |                   | Min.  | Max.                                  |      |
| Oscillator period | t <sub>CLCL</sub> | 41.7  | 285.7                                 | ns   |
| High time         | t <sub>CHCX</sub> | 12  | t <sub>CLCL</sub> - t <sub>CLCX</sub> | ns   |
| Low time          | t <sub>CLCX</sub> | 12  | t <sub>CLCL</sub> - t <sub>CHCX</sub> | ns   |
| Rise time         | t <sub>CLCH</sub> | -   | 12                                    | ns   |
| Fall time         | t <sub>CHCL</sub> | -   | 12                                    | ns   |

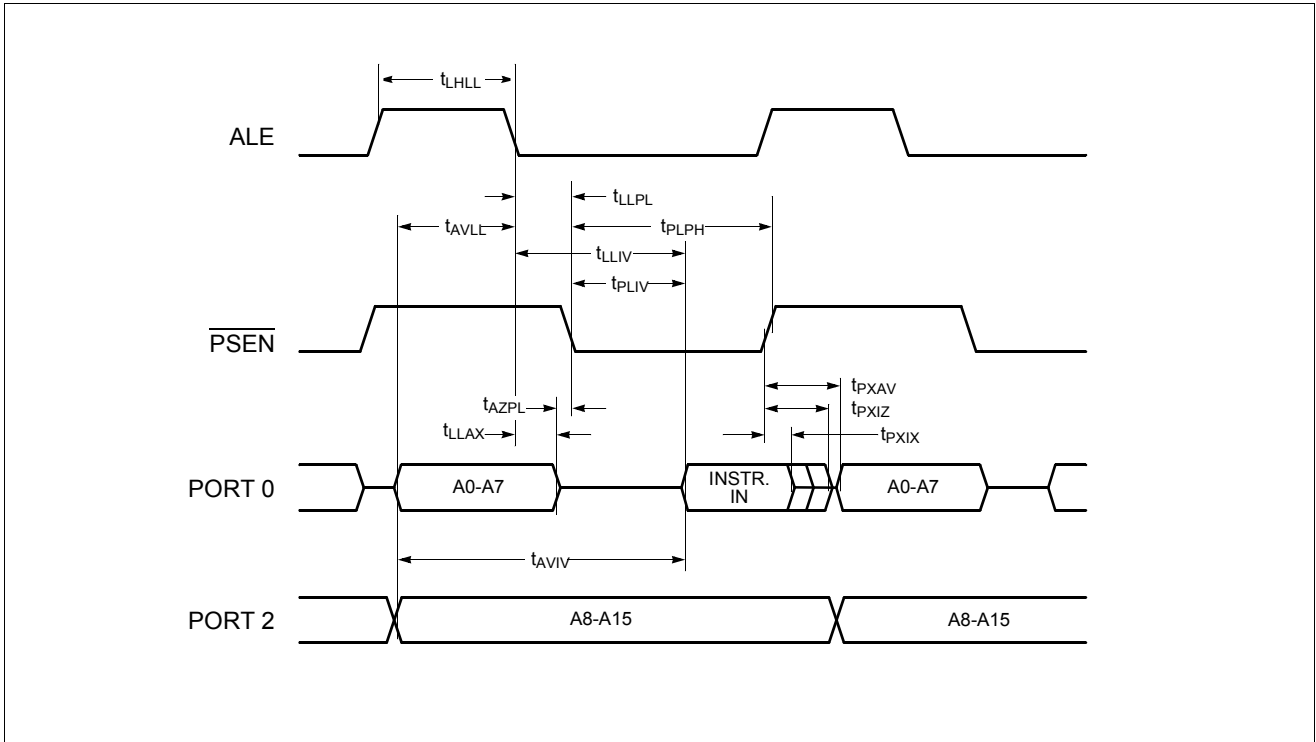


Figure 4. External Program Memory Read Cycle

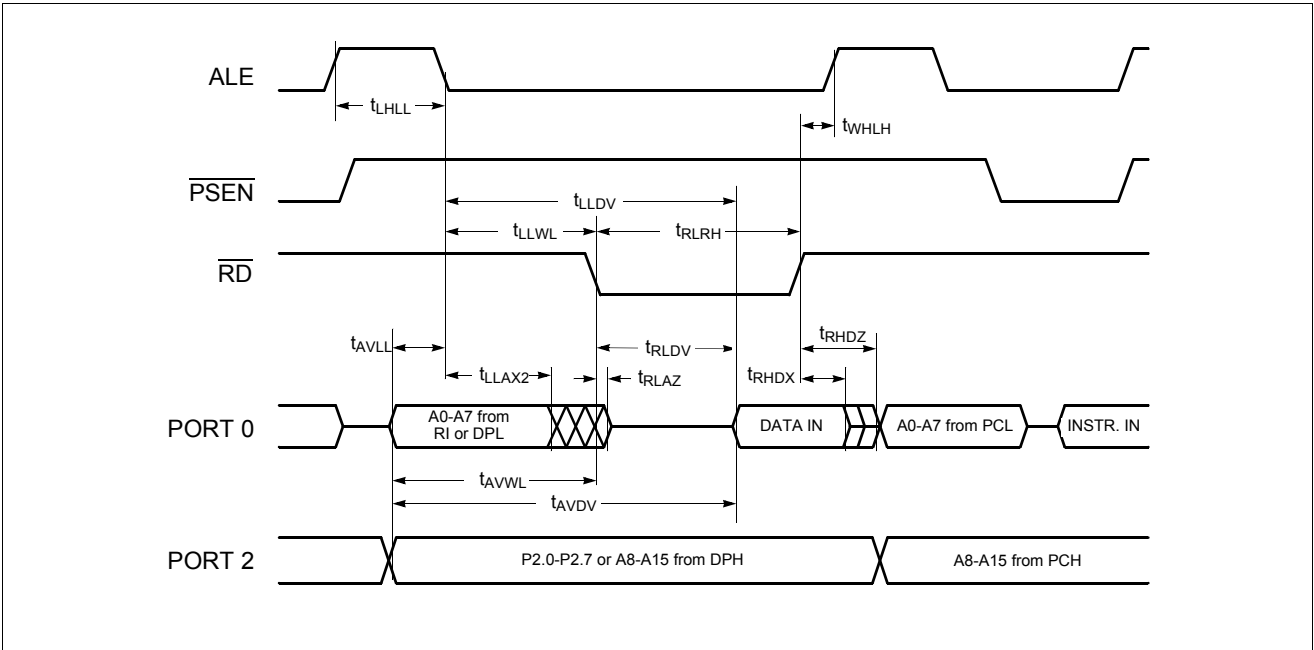


Figure 5. External Data Memory Read Cycle

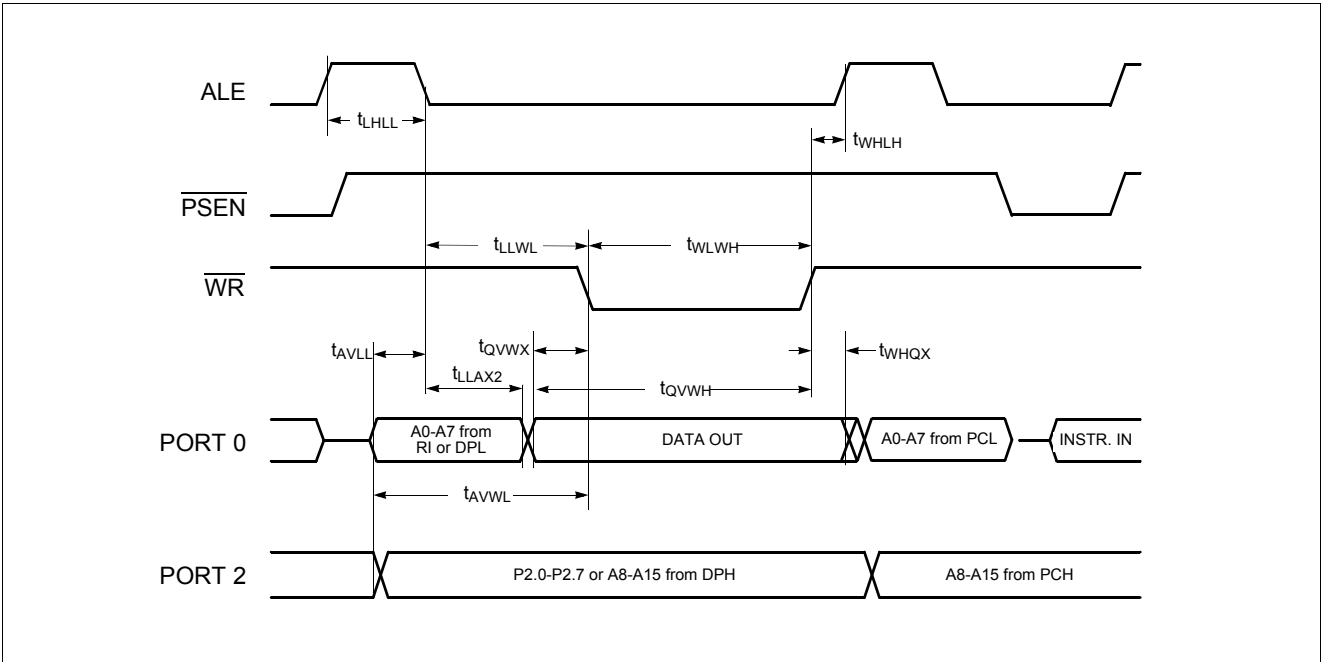


Figure 6. External Data Memory Write Cycle

## Chapter 4. Flash Characteristics

### 4.1 Flash Characteristics

The GMS99C58 is programmed by using a Pulse Programming algorithm. Table 17 shows the logic levels for reading the main memory, for programming the main memory, for programming the encryption table, for programming the security bits, and erase the all Flash cell memory. The circuit configuration and waveforms are shown in Figure 7 and Figure 9. Figure 10 shows the circuit configuration for normal program memory verification.

### 4.2 Program Operation

The setup for pulse programming is shown in Figure 8. Note that the GMS99C58 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers. The address of the Flash location to be programmed is applied to ports 1 and 2, port3 as shown in Figure 7. The code byte to be programmed into that location are held at the “Pgm code Data” levels indicated in Table 17.

To program the encryption table, repeat the pulse programming sequence for addresses 0 through 3FH, using the “Pgm Encryption table” levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the pulse programming sequence using the “Pgm Security Bit” levels after one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the EA/VPP pin must not be allowed to go above the maximum specified VPP level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The VPP source should be well regulated and free glitches and overshoot.

### 4.3 Program Verify Operation

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the memory location to be read is applied to ports 1, 2, and 3 as shown in Figure 10. The other pins are held at the “Verify Code Data” levels indicated in Table 17. The contents of the address location will be emitted on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

### 4.4 Chip erase

All Flash cells are erased electrically at the same time. Chip erase is initiated by using the proper combination of control signal using “Chip Erase mode”. The main memory, lock bit, and encryption memory are written with all “1” in the Chip erase operation. In this mode, Chip erase is self timed and takes about more than 200ms

### 4.5 Program/Verify Algorithms

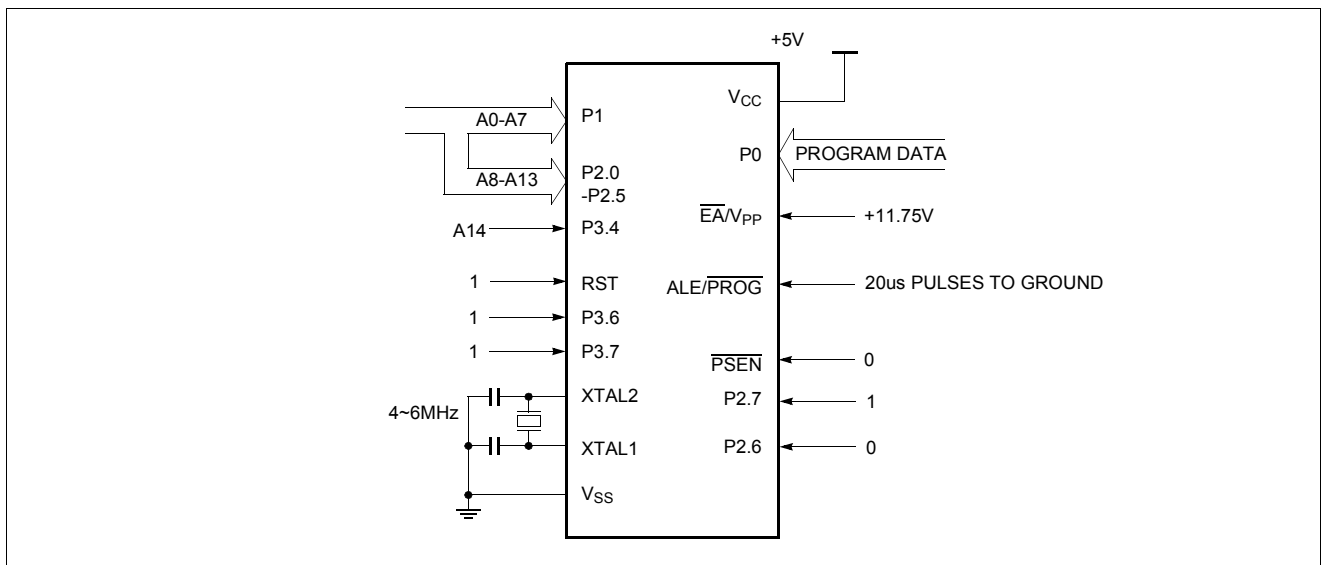
Any algorithm in agreement with the conditions listed in Table 17, and which satisfies the timing specifications, is suitable.

**Table 17. Flash Programming Modes**

| Mode       |                      | RST | PSEN | PROG | $\overline{EV/V_{pp}}$ | P2.7 | P2.6 | P3.7 | P3.6 |
|------------|----------------------|-----|------|------|------------------------|------|------|------|------|
| Verify     | Verify code data     | 1   | 0    | 1    | 1                      | 0    | 0    | 1    | 1    |
| PGM        | Pgm code data        | 1   | 0    | 0    | Vpp                    | 1    | 0    | 1    | 1    |
|            | Pgm encryption table | 1   | 0    | 0    | Vpp                    | 1    | 0    | 1    | 0    |
|            | Pgm security bit 1   | 1   | 0    | 0    | Vpp                    | 1    | 1    | 1    | 1    |
|            | Pgm security bit 2   | 1   | 0    | 0    | Vpp                    | 1    | 1    | 0    | 0    |
| Chip erase |                      | 1   | 0    | 0    | Vpp                    | 0    | 1    | 0    | 0    |

**Note:**

1. “0”: valid low for that pin, “1”: valid high for that pin.
2. VPP= 11.75V ± 0.25V.
3. VCC= 5V ± 10% during programming ,verification, and erasing.
4. ALE/PROG receivers programming and erasing pulses while Vpp is held at 11.75V.
5. ALE/PROG Low Pulse width and repeat limit are 20us and 4 times during programming.
6. ALE/PROG Low Pulse width and repeat limit are 30ms and 5 times during erasing.
7. A14, A13, A12 are forced to Low during the erasing time.



**Figure 7. Programming Code data Configuration**

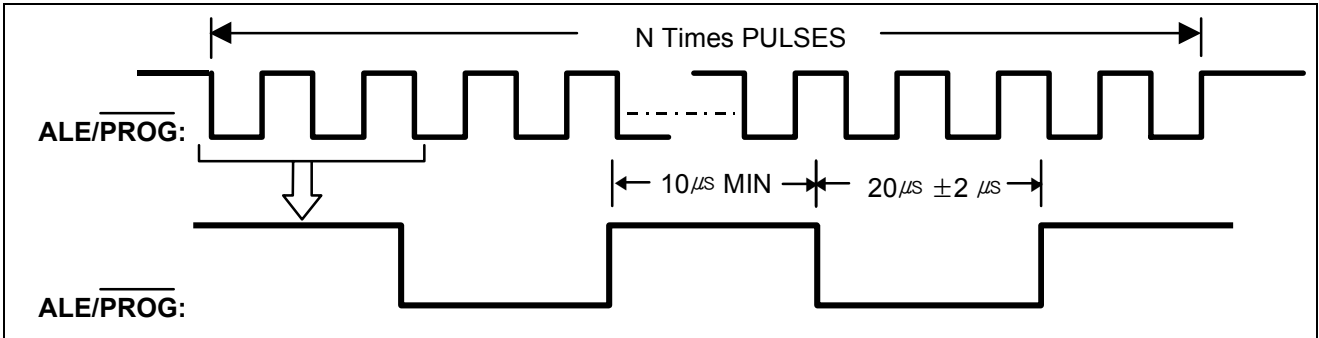


Figure 8. /PROG waveform

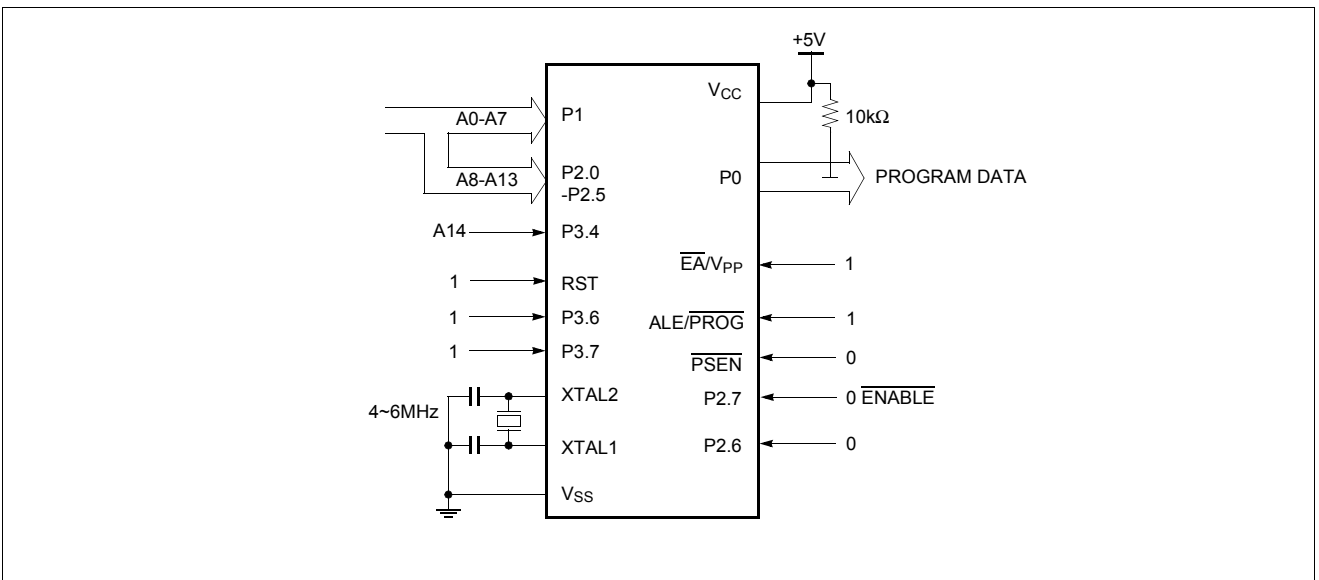


Figure 9. Program Verification



#### 4.6 Flash Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$  to  $27^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ ;

| Parameter                                       | Symbol       | Limit Values |              | Unit          |
|---|--------------|--------------|--------------|---------------|
|   |              | Min.         | Max.         |               |
| Programming supply voltage                      | $V_{PP}$     | 11.5         | 12.0         | V             |
| Programming supply current                      | $I_{PP}$     | -            | 50           | mA            |
| Oscillator frequency                            | $1/t_{CLCL}$ | 4            | 6            | MHz           |
| Address setup to $\overline{PROG}$ low          | $t_{AVGL}$   | $48t_{CLCL}$ | -            | -             |
| Address hold after $\overline{PROG}$            | $t_{GHAX}$   | $48t_{CLCL}$ | -            | -             |
| Data setup to $\overline{PROG}$ low             | $t_{DVGL}$   | $48t_{CLCL}$ | -            | -             |
| Data hold after $\overline{PROG}$               | $t_{GHDX}$   | $48t_{CLCL}$ | -            | -             |
| P2.7 ( $\overline{ENABLE}$ ) high to $V_{PP}$   | $t_{EHS}$    | $48t_{CLCL}$ | -            | -             |
| $V_{PP}$ setup to $\overline{PROG}$ low         | $t_{SHGL}$   | 10           | -            | $\mu\text{s}$ |
| $V_{PP}$ hold after $\overline{PROG}$           | $t_{GHSL}$   | 10           | -            | $\mu\text{s}$ |
| $\overline{PROG}$ width of Program              | $t_{GLGH}$   | 18           | 22           | $\mu\text{s}$ |
| $\overline{PROG}$ width of Erase                | $t_{GLGH}$   | 90           | 110          | ms            |
| Address to data valid                           | $t_{AVQV}$   | -            | $48t_{CLCL}$ | -             |
| $\overline{ENABLE}$ low to data valid           | $t_{ELQV}$   | -            | $48t_{CLCL}$ | -             |
| Data float after $\overline{ENABLE}$            | $t_{EHQZ}$   | 0            | $48t_{CLCL}$ | -             |
| $\overline{PROG}$ high to $\overline{PROG}$ low | $t_{GHGL}$   | 5            | -            | $\mu\text{s}$ |

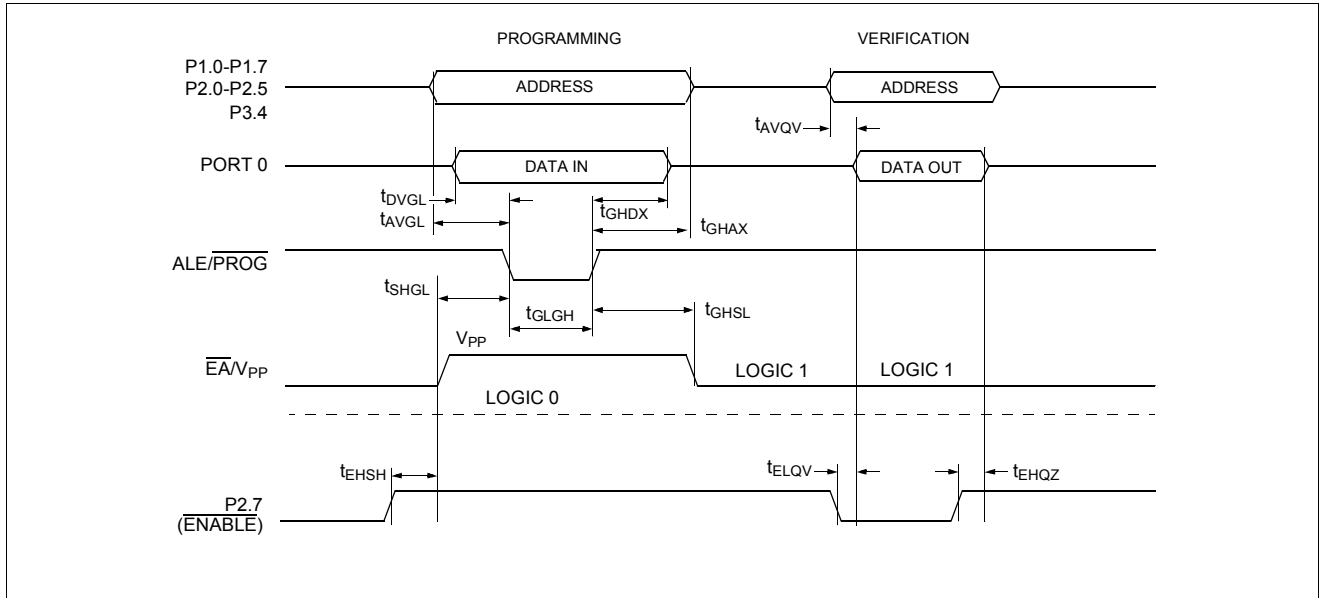


Figure 10. Flash Programming and Verification

### Chapter 5. Recommended Oscillator Circuits

