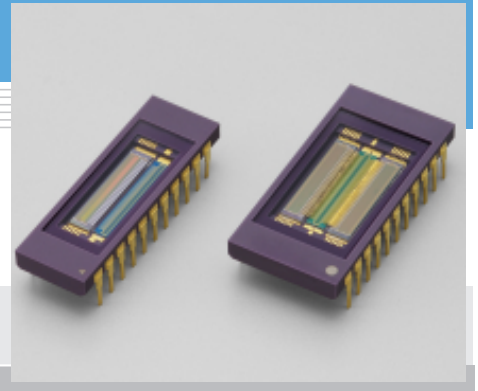


# InGaAs linear image sensor G9494-256D/-512D

Near infrared image sensor (0.9 to 1.7  $\mu\text{m}$ ) with high-speed data rate



HAMAMATSU provides high-speed, near infrared image sensors designed for detectors used in on-line foreign object inspection equipment. These image sensors use square-shaped pixels that are ideally suited for software processing in pattern recognition systems. The signal processing circuit employs CTIA (Capacitive Transfer Impedance Amplifier) method to perform simultaneous charge integration on all pixels, so there is no time lag among the pixel output signals.

## Features

- High-speed data rate: 2 MHz Typ.
- Selectable conversion gain (Cf=0.1 pF, 1 pF)
- Pixel size  
G9494-256D: 50 × 50  $\mu\text{m}$   
G9494-512D: 25 × 25  $\mu\text{m}$
- CMOS readout circuit incorporated
- Low dark current
- Room temperature operation

## Applications

- Foreign object detection monitors
- Near infrared spectroscopy

### ■ Selection guide

Type No.	Cooling	Number of pixels	Pixel pitch ( $\mu\text{m}$ )	Pixel size [ $\mu\text{m}$ (H) × $\mu\text{m}$ (V)]	Spectral response range ( $\mu\text{m}$ )	Defective pixel
G9494-256D	Non-cooled	256	50	50 × 50	0.9 to 1.7 (25 °C)	Less than 1 %
G9494-512D		512	25	25 × 25		

### ■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage	Vdd	-0.3 to +6	V
Clock pulse voltage	V $\phi$	-0.3 to +6	V
Reset pulse voltage	V (RES)	-0.3 to +6	V
Gain selection terminal voltage	VcfsEL	-0.3 to +6	V
Operating temperature *1	Topr	-20 to +70	°C
Storage temperature *1	Tstg	-20 to +85	°C

\*1: No condensation

### ■ Electrical characteristics (Ta=25 °C)

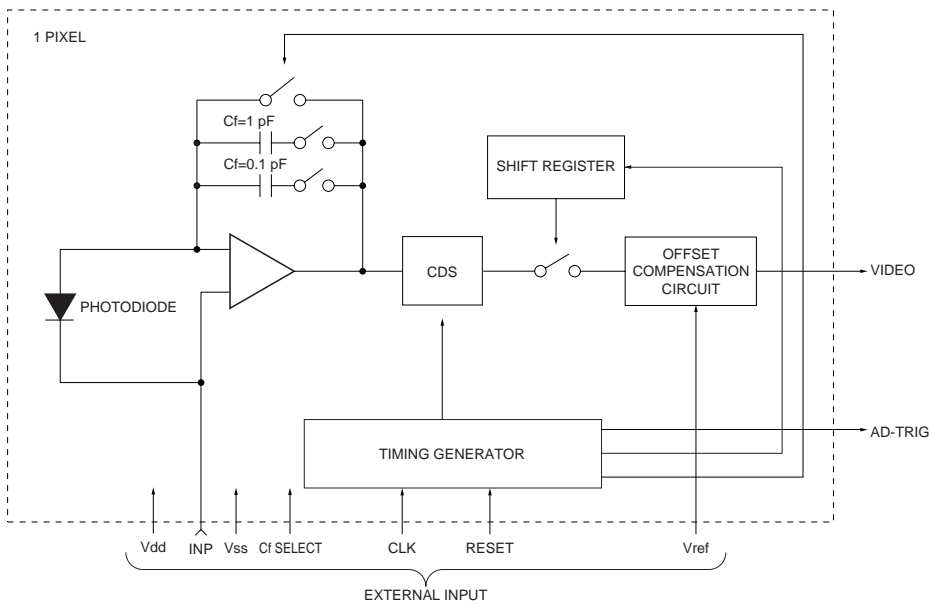
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vdd	4.5	5.0	5.5	V
		4.5	5.0	5.5	
Supply voltage	Vref	-	1.26	-	V
Supply current	Ivdd	-	40	75	mA
		-	80	150	
Supply current	Ivref	-	-	1	mA
		-	-	1	
Ground	Vss	-	0	-	V
Element bias	INP	3.3	3.5	3.6	V
Clock frequency	f	0.1	2	4	MHz
Clock pulse voltage	V $\phi$	4.5	5.0	5.5	V
		-	0	0.4	
Clock pulse rise / fall times	tr $\phi$ , tf $\phi$	0	20	100	ns
Clock pulse width	tpw $\phi$	100	-	-	ns
Reset pulse voltage	V (RES)	4.5	5.0	5.5	V
		-	0	0.4	
Reset pulse rise / fall times	tr (RES), tf (RES)	0	20	100	ns
Reset pulse width *2	tpw (RES)	6/f	-	-	$\mu\text{s}$
Video output voltage	VH	-	3.5	INP	V
		-	1.26	-	
Video output impedance	Zv	-	5	-	k $\Omega$
A/D trigger voltage	Vtrig	-	Vdd	-	V
		-	GND	-	
A/D trigger drive function	Vad	74HC244 1 ch	-	-	-
Data rate	fv	-	f	-	Hz

\*2: 6  $\mu\text{s}$  or more

■ Specification ( $T_a=25\text{ }^\circ\text{C}$ ,  $V_{dd}=5\text{ V}$ ,  $INP=3.5\text{ V}$ ,  $V_{ref}=1.26\text{ V}$ ,  $C_f=0.1\text{ pF}$ ,  $f=2\text{ MHz}$ , integration time  $200\text{ }\mu\text{s}$ , per 1 element)

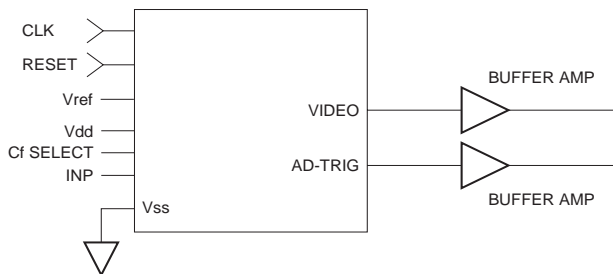
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Peak sensitivity wavelength	$\lambda_p$		-	1.55	-	$\mu\text{m}$
Saturation charge	$Q_{sat}$	$V_\phi=5\text{ V}$	-	0.2	-	pC
Dark current	ID		-	4	20	pA
			-	1	5	
RMS noise voltage (readout noise)	N	Standard deviation Number of integration 50	-	900	2000	$\mu\text{V rms}$
Saturation voltage	$V_{sat}$		-	2	-	V
Photo response non uniformity	PRNU		-	$\pm 5$	$\pm 20$	%
Detective pixel	-		-	-	1	%

### ■ Equivalent circuit



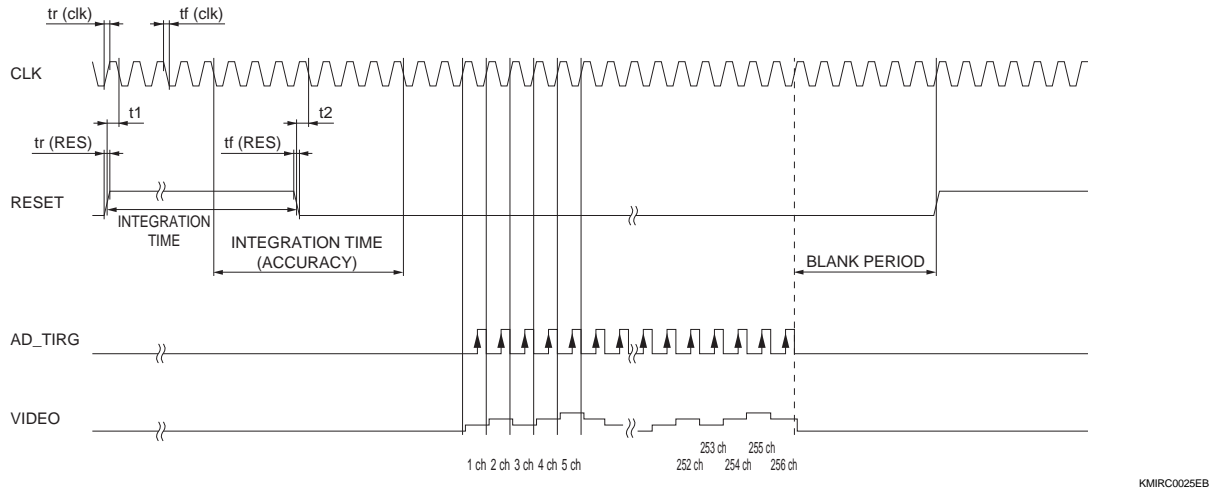
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### ■ Basic circuit connection



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## ■ Timing chart

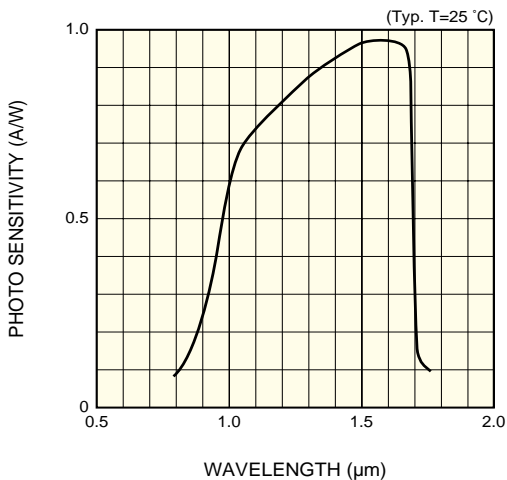


Note) More than 3  $\mu\text{s}$  is required for a blank period from the last pixel to the rising edge of RESET pulse.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	-	0.1	2	4	MHz
Clock pulse width	tpw (clk)	100	-	-	ns
Clock pulse rise / fall times	tr (clk), tf (clk)	0	20	100	ns
Reset pulse width <sup>*3</sup>	tpw (RES)	6/f	-	-	$\mu\text{s}$
Reset pulse rise / fall times	tr (RES), tf (RES)	0	20	100	ns
Clock pulse to start pulse timing	t1, t2	50	-	-	ns
Video delay time	tvd	100	-	-	ns

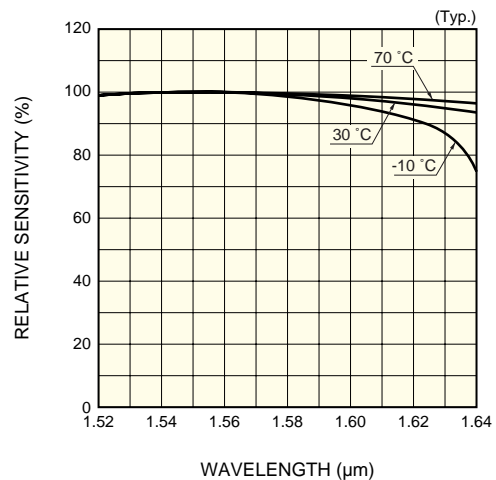
\*3: 6  $\mu\text{s}$  or more

## ■ Spectral response



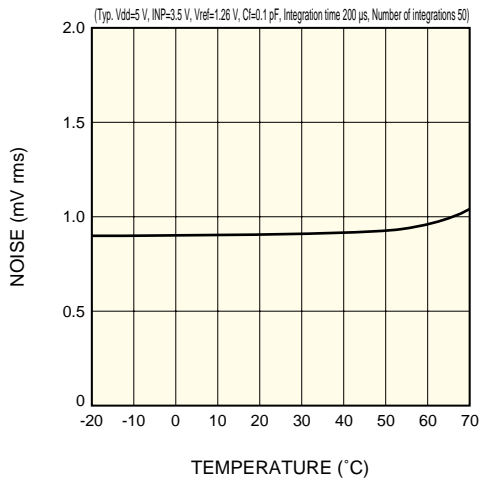
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## ■ Photo sensitivity temperature characteristics



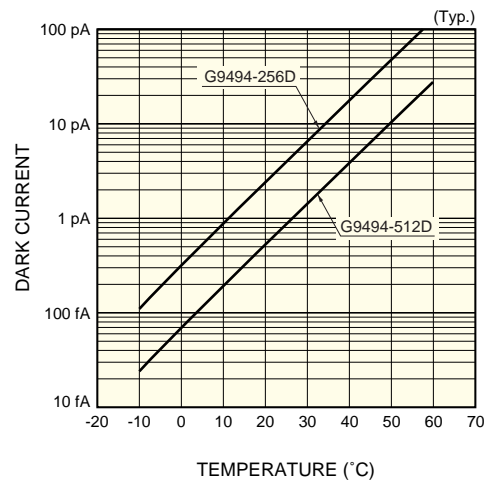
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## ■ Noise vs. temperature



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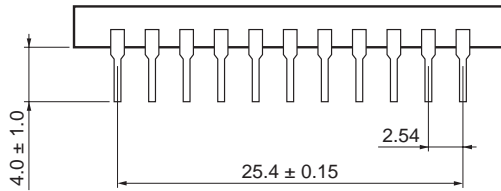
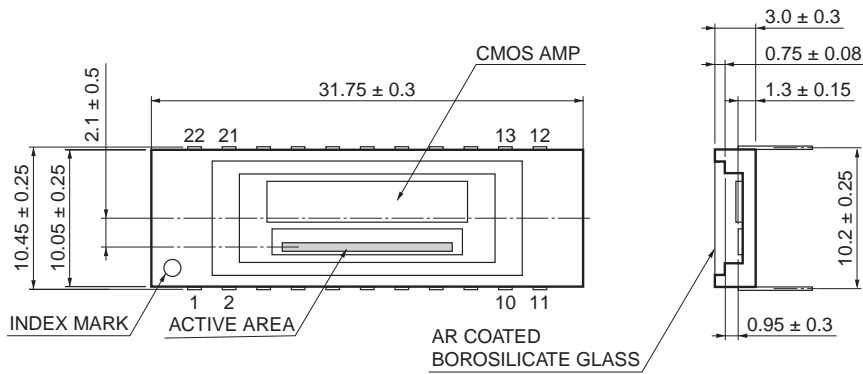
## ■ Dark current vs. temperature



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## ■ Dimensional outlines (unit: mm)

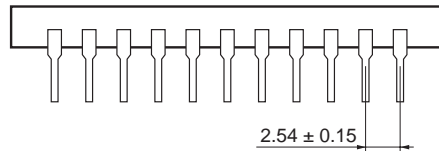
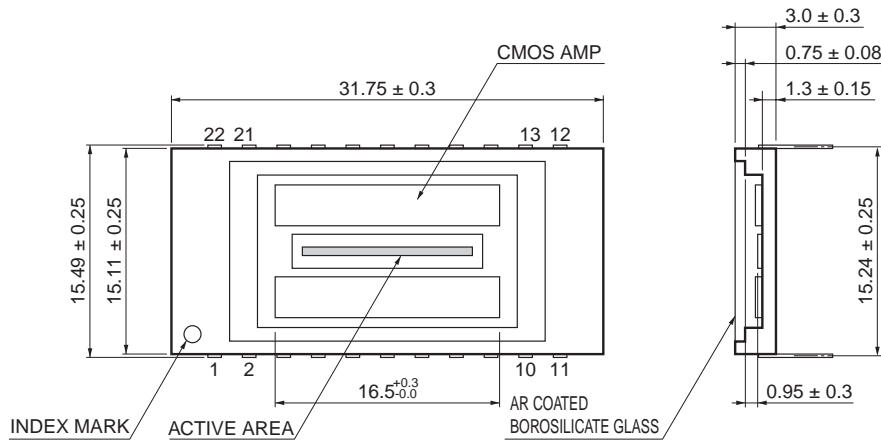
### G9494-256D



Pin No.	Pin connection	Pin No.	Pin connection
1	NC	12	VIDEO
2	NC	13	V <sub>ref</sub>
3	NC	14	CLK
4	NC	15	NC
5	NC	16	INP
6	NC	17	V <sub>ss</sub>
7	NC	18	V <sub>dd</sub>
8	NC	19	NC
9	NC	20	AD-TRIG
10	NC	21	RESET
11	NC	22	CI-SELECT

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## G9494-512D



Pin No.	Pin connection	Pin No.	Pin connection
1	NC	12	VIDEO-ODD
2	RESET-EVEN	13	Vref
3	AD-TRIG-EVEN	14	CLK-ODD
4	NC	15	NC
5	NC	16	INP
6	NC	17	Vss
7	NC	18	Vdd
8	NC	19	NC
9	CLK-EVEN	20	AD-TRIG-ODD
10	NC	21	RESET-ODD
11	VIDEO-EVEN	22	Cf-SELECT

"-EVEN" FOR EVEN No. PIXELS,  
"-ODD" FOR ODD No. PIXELS.

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### Pin connection

Terminal name	Input/Output	Function and recommended connection
CLK	Input (CMOS logic)	Clock pulse for operating the CMOS shift register
RESET	Input (CMOS logic)	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. The width of the reset pulse determines integration time.
Vdd	Input	Supply voltage for operating the signal processing circuit on the CMOS chip
Vss	-	Ground for the signal processing circuit on the CMOS chip
INP	Input	Reset voltage for the charge amplifier array on the CMOS chip
Cf SELECT	Input	Voltage that determines the feedback capacitance (Cf) on the CMOS chip. Cf=0.1 pF at 0 V, and Cf=1 pF at 5 V
Vref	Input	Reset voltage for the offset compensation circuit at the CMOS chip
AD-TRIG	Output	Digital signal for AD conversion; positive polarity
VIDEO	Output	Analog video signal; positive polarity

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