



FSL136HR Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche-Rugged SenseFET (650V)
- Under 50mW Standby Power Consumption at 265V_{AC}, No-load Condition with Burst Mode
- Precision Fixed Operating Frequency with Frequency Modulation for Attenuating EMI
- Internal Startup Circuit
- Built-in Soft-Start: 20ms
- Pulse-by-Pulse Current Limiting
- Various Protections: Over-Voltage Protection (OVP), Overload Protection (OLP), Output-Short Protection (OSP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown Function with Hysteresis (TSD)
- Auto-Restart Mode
- Under-Voltage Lockout (UVLO)
- Low Operating Current: 1.8mA
- Adjustable Peak Current Limit

Applications

- SMPS for VCR, STB, DVD, & DVCD Players
- SMPS for Home Appliance
- Adapter

Related Resources

- [AN-4137-Design Guidelines for Off-line Flyback Converters Using FPS™](#)
- [AN-4141-Troubleshooting and Design Tips for Fairchild Power Switch \(FPS™\) Flyback Applications](#)
- [AN-4147-Design Guidelines for RCD Snubber of Flyback](#)

Description

The FSL136HR integrated Pulse Width Modulator (PWM) and SenseFET is specifically designed for high-performance offline Switch-Mode Power Supplies (SMPS) with minimal external components. FSL136HR includes integrated high-voltage power switching regulators that combine an avalanche-rugged SenseFET with a current-mode PWM control block.

The integrated PWM controller includes: Under-Voltage Lockout (UVLO) protection, Leading-Edge Blanking (LEB), a frequency generator for EMI attenuation, an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, and temperature-compensated precision current sources for loop compensation and fault protection circuitry. The FSL136HR offers good soft-start performance. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSL136HR reduces total component count, design size, and weight; while increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for the design of cost-effective flyback converters.

Maximum Output Power ⁽¹⁾			
230V _{AC} ± 15% ⁽²⁾		85-265V _{AC}	
Adapter ⁽³⁾	Open Frame	Adapter ⁽³⁾	Open Frame
19W	26W	14W	20W

Notes:

1. The junction temperature can limit the maximum output power.
2. 230V_{AC} or 100/115V_{AC} with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FSL136HR	-40 to 105°C	FSL136HR	8-Lead, Dual Inline Package (DIP)	Rail

Typical Application Diagram

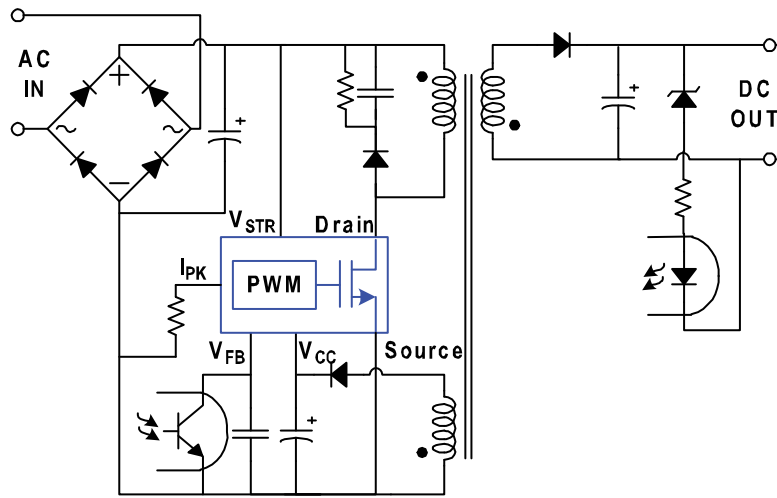


Figure 1. Typical Application

Internal Block Diagram

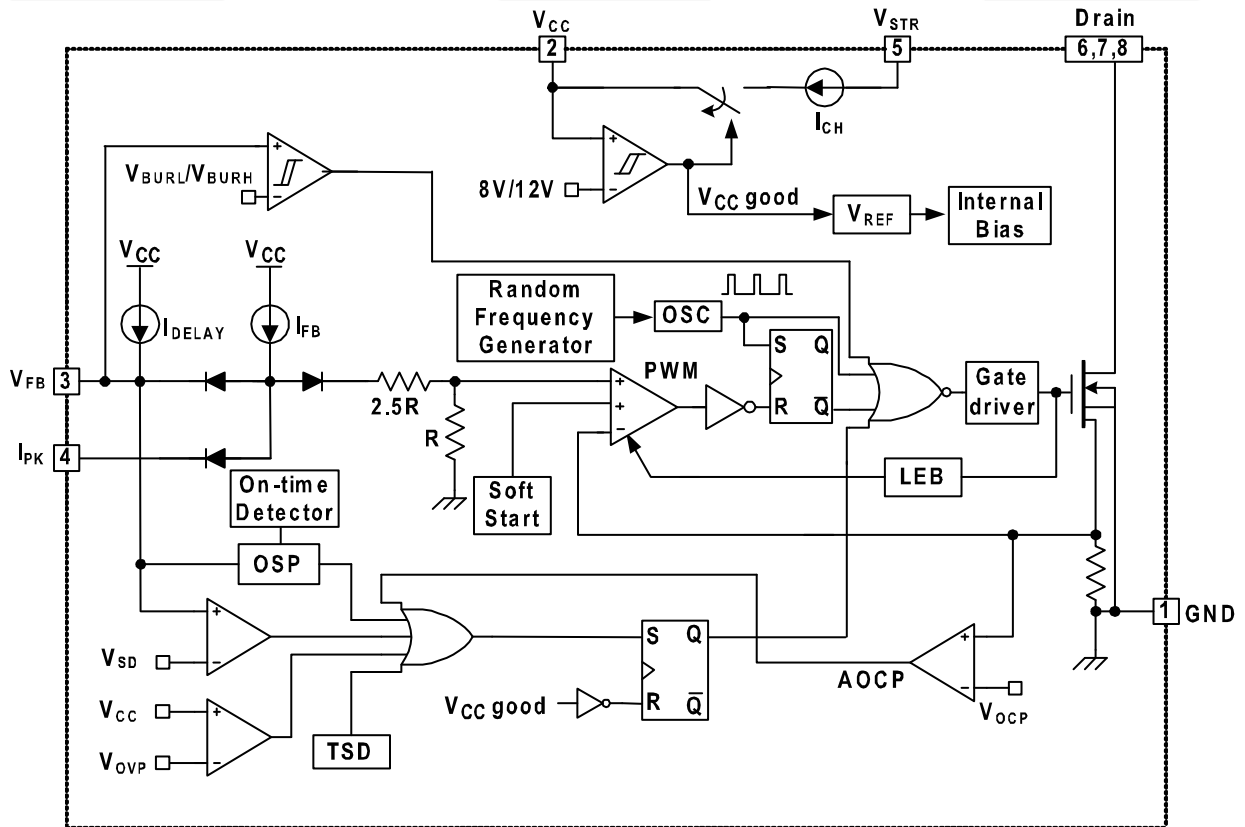


Figure 2. Internal Block Diagram

Pin Configuration

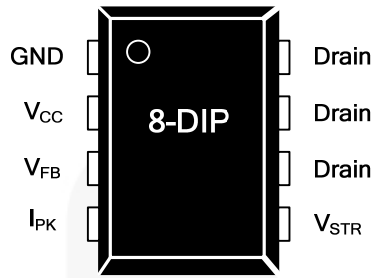


Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	Ground. SenseFET source terminal on the primary side and internal control ground.
2	V _{CC}	Positive Supply Voltage Input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V _{STR}) via an internal switch during startup (see <i>Internal Block Diagram Section</i>). Once V _{CC} reaches the UVLO upper threshold (12V), the internal startup switch opens and device power is supplied via the auxiliary transformer winding.
3	V _{FB}	Feedback Voltage. The non-inverting input to the PWM comparator, it has a 0.4mA current source connected internally, while a capacitor and opto-coupler are typically connected externally. There is a delay while charging external capacitor C _{FB} from 2.4V to 6V using an internal 5μA current source. This delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
4	I _{PK}	Peak Current Limit. Adjusts the peak current limit of the SenseFET. The feedback 0.4mA current source is diverted to the parallel combination of an internal 6kΩ resistor and any external resistor to GND on this pin to determine the peak current limit.
5	V _{STR}	Startup. Connected to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the V _{CC} pin and ground. Once V _{CC} reaches 12V, the internal switch is opened.
6, 7, 8	Drain	Drain. Designed to connect directly to the primary lead of the transformer and capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_J=25^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage	-0.3	650.0	V
V_{DS}	Drain Pin Voltage	-0.3	650.0	V
V_{CC}	Supply Voltage		26	V
V_{FB}	Feedback Voltage Range	-0.3	12.0	V
I_D	Continuous Drain Current		3	A
I_{DM}	Drain Current Pulsed ⁽⁴⁾		12	A
E_{AS}	Single Pulsed Avalanche Energy ⁽⁵⁾		230	mJ
P_D	Total Power Dissipation		1.5	W
T_J	Operating Junction Temperature	Internally Limited		$^{\circ}\text{C}$
T_A	Operating Ambient Temperature	-40	+105	$^{\circ}\text{C}$
T_{STG}	Storage Temperature	-55	+150	$^{\circ}\text{C}$
ESD	Human Body Model, JESD22-A114 ⁽⁶⁾	5.0		KV
	Charged Device Model, JESD22-C101 ⁽⁶⁾	1.5		
Θ_{JA}	Junction-to-Ambient Thermal Resistance ⁽⁷⁾⁽⁸⁾		80	$^{\circ}\text{C}/\text{W}$
Θ_{JC}	Junction-to-Case Thermal Resistance ⁽⁷⁾⁽⁹⁾		19	$^{\circ}\text{C}/\text{W}$
Θ_{JT}	Junction-to-Top Thermal Resistance ⁽⁷⁾⁽¹⁰⁾		33.7	$^{\circ}\text{C}/\text{W}$

Notes:

- Repetitive rating: pulse width limited by maximum junction temperature.
- $L=51\text{mH}$, starting $T_J=25^{\circ}\text{C}$.
- Meets JEDEC standards JESD 22-A114 and JESD 22-C101.
- All items are tested with the standards JESD 51-2 and JESD 51-10 (DIP package).
- Θ_{JA} free-standing, with no heat-sink, under natural convection.
- Θ_{JC} junction-to-lead thermal characteristics under Θ_{JA} test condition. T_C is measured on the source #7 pin closed to plastic interface for Θ_{JA} thermo-couple mounted on soldering.
- Θ_{JT} junction-to-top of thermal characteristic under Θ_{JA} test condition. T_t is measured on top of package. Thermo-couple is mounted in epoxy glue.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
SenseFET Section						
BV _{DSS}	Drain Source Breakdown Voltage	V _{CC} = 0V, I _D = 250μA	650			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650V, V _{GS} = 0V			250	μA
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} = 10V, V _{DS} = 0V, T _C = 25°C		3.5	4.0	Ω
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		290		pF
C _{OSS}	Output Capacitance	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		45		pF
C _{RSS}	Reverse Transfer Capacitance	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		5.5		pF
t _{d(ON)}	Turn-On Delay	V _{DD} = 350V, I _D = 3.5A		12		ns
t _r	Rise Time	V _{DD} = 350V, I _D = 3.5A		22		ns
t _{d(OFF)}	Turn-Off Delay	V _{DD} = 350V, I _D = 3.5A		20		ns
t _f	Fall Time	V _{DD} = 350V, I _D = 3.5A		19		ns
Control Section						
f _{OSC}	Switching Frequency	V _{DS} = 650V, V _{GS} = 0V	90	100	110	KHz
Δf _{OSC}	Switching Frequency Variation	V _{GS} = 10V, V _{GS} = 0V, T _C = 125°C		±5	±10	%
f _{FM}	Frequency Modulation			±3		KHz
D _{MAX}	Maximum Duty Cycle	V _{FB} = 4V	71	77	83	%
D _{MIN}	Minimum Duty Cycle	V _{FB} = 0V	0	0	0	%
V _{START}	UVLO Threshold Voltage		11	12	13	V
V _{STOP}		After Turn-On	7	8	9	V
I _{FB}	Feedback Source Current	V _{FB} = 0V	320	400	480	μA
t _{S/S}	Internal Soft-Start Time	V _{FB} = 4V	15	20	25	ms
Burst Mode Section						
V _{BURH}	Burst Mode Voltage	T _J = 25°C	0.4	0.5	0.6	V
V _{BURL}			0.25	0.35	0.45	V
V _{BUR(HYS)}				150		mV
Protection Section						
I _{LIM}	Peak Current Limit	T _J = 25°C, di/dt = 300mA/μs	1.89	2.15	2.41	A
t _{CLD}	Current Limit Delay Time ⁽¹¹⁾		200			ns
V _{SD}	Shutdown Feedback Voltage	V _{CC} = 15V	5.5	6.0	6.5	V
I _{DELAY}	Shutdown Delay Current	V _{FB} = 5V	3.5	5.0	6.5	μA
V _{OVp}	Over-Voltage Protection Threshold	V _{FB} = 2V	22.5	24.0	25.5	V
t _{OSP}	Output Short Protection ⁽¹¹⁾	Threshold Time		1.00	1.35	μs
V _{OSP}		Threshold Feedback Voltage	T _J = 25°C OSP Triggered When t _{ON} < t _{OSP} , V _{FB} > V _{OSP} and Lasts Longer than t _{OSP_FB}	1.44	1.60	V
t _{OSP_FB}		Feedback Blanking Time		2.0	2.5	μs
V _{AoCP}	AoCP Voltage ⁽¹¹⁾	T _J = 25°C	0.85	1.00	1.15	V
TSD	Thermal Shutdown ⁽¹¹⁾	Shutdown Temperature	125	137	150	°C
HYS _{TSD}		Hysteresis			60	°C
t _{LEB}	Leading-Edge Blanking Time ⁽¹¹⁾		300			ns

Continued on the following page...

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Total Device Section						
I _{OP1}	Operating Supply Current ⁽¹¹⁾ (While Switching)	V _{CC} = 14V, V _{FB} > V _{BURH}		2.5	3.5	mA
I _{OP2}	Operating Supply Current (Control Part Only)	V _{CC} = 14V, V _{FB} < V _{BURL}		1.8	2.5	mA
I _{CH}	Startup Charging Current	V _{CC} = 0V	0.90	1.10	1.30	mA
V _{STR}	Minimum V _{STR} Supply Voltage	V _{CC} = V _{FB} = 0V, V _{STR} Increase	35			V

Note:

11. Though guaranteed by design, it is not 100% tested in production.

Typical Performance Characteristics

These characteristic graphs are normalized at 25.



Figure 4. Operating Frequency vs. Temperature



Figure 5. Maximum Duty Cycle vs. Temperature



Figure 6. Operating Supply Current vs. Temperature



Figure 7. Start Threshold Voltage vs. Temperature



Figure 8. Stop Threshold Voltage vs. Temperature



Figure 9. Feedback Source Current vs. Temperature

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A=25$.

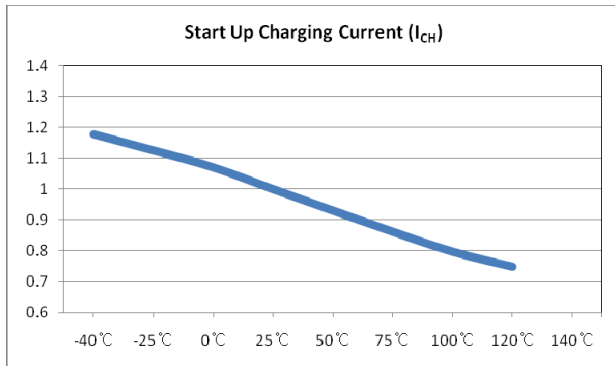


Figure 10. Startup Charging Current vs. Temperature

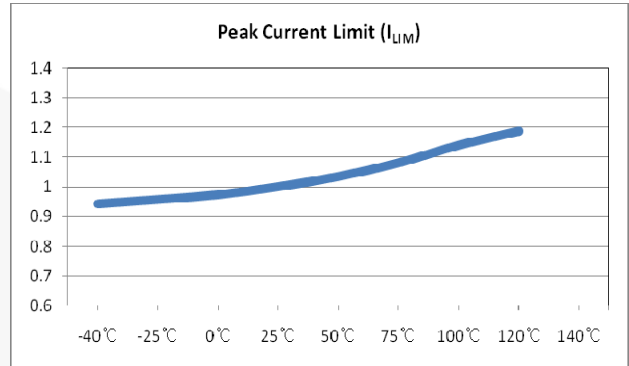


Figure 11. Peak Current Limit vs. Temperature

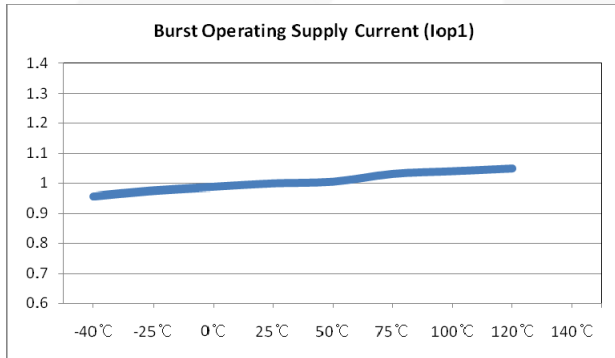


Figure 12. Burst Operating Supply Current vs. Temperature

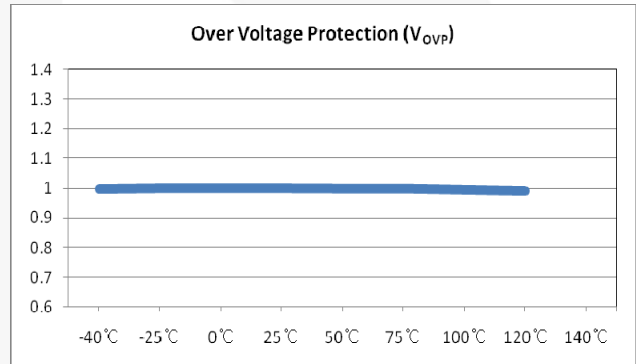


Figure 13. Over Voltage Protection vs. Temperature

Functional Description

Startup

At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_A) connected with the V_{CC} pin, as illustrated in Figure 14. When V_{CC} reaches the start voltage of 12V, the FPS™ begins switching and the internal high-voltage current source is disabled. The FPS continues normal switching operation and the power is provided from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8V.

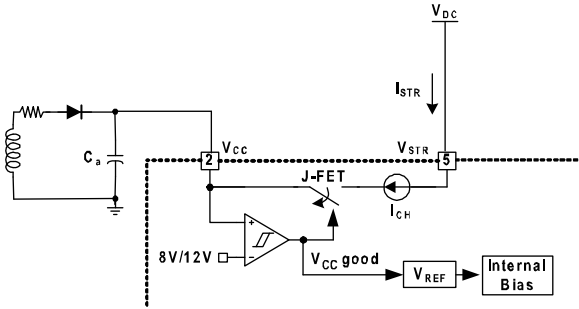


Figure 14. Startup Circuit

Oscillator Block

The oscillator frequency is set internally and the FPS has a random frequency fluctuation function. Fluctuation of the switching frequency of a switched power supply can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the range of the frequency variation. The range of frequency variation is fixed internally; however, its selection is randomly chosen by the combination of external feedback voltage and internal free-running oscillator. This randomly chosen switching frequency effectively spreads the EMI noise nearby switching frequency and allows the use of a cost-effective inductor instead of an AC input line filter to satisfy the world-wide EMI requirements.

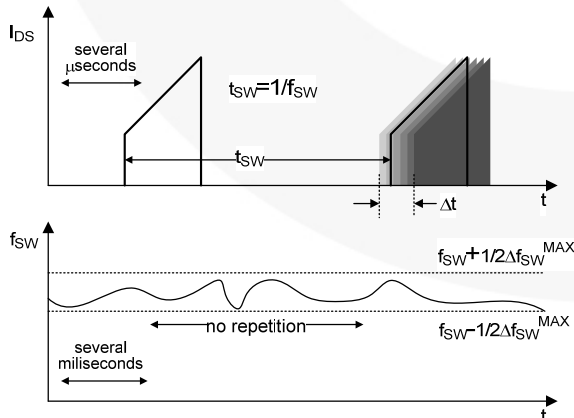


Figure 15. Frequency Fluctuation Waveform

Feedback Control

The FSL136HR employs current-mode control, as shown in Figure 16. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the shunt regulator reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage V_{FB} is pulled down, and the duty cycle is reduced. This typically occurs when the input voltage is increased or the output load is decreased.

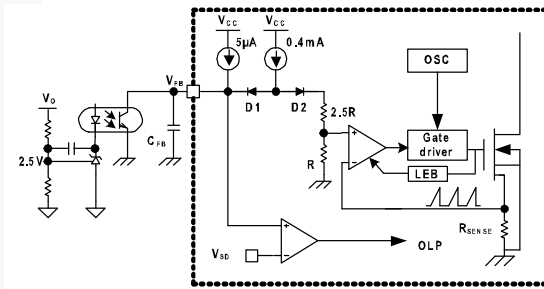


Figure 16. Pulse-Width-Modulation Circuit

Leading-Edge Blanking (LEB)

At the instant the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically cause a high-current spike through the SenseFET. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading-edge blanking (LEB) circuit (see the Figure 16). This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

Protection Circuits

The FPS has several protective functions, such as overload protection (OLP), over-voltage protection (OVP), output-short protection (OSP), under-voltage lockout (UVLO), abnormal over-current protection (AOCP), and thermal shutdown (TSD). Because these various protection circuits are fully integrated in the IC without external components, the reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage V_{STOP} (8V), the protection is reset and the internal high-voltage current source charges the V_{CC} capacitor via the V_{STR} pin. When V_{CC} reaches the UVLO start voltage V_{START} (12V), the FPS resumes normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

OSP detects V_{FB} and SenseFET turn-on time. When the V_{FB} is higher than 1.6V and the SenseFET turn-on time is lower than 1.2 μ s, the FPS recognizes this condition as an abnormal error and shuts down PWM switching until V_{CC} reaches V_{START} again. An abnormal condition is shown in Figure 20.

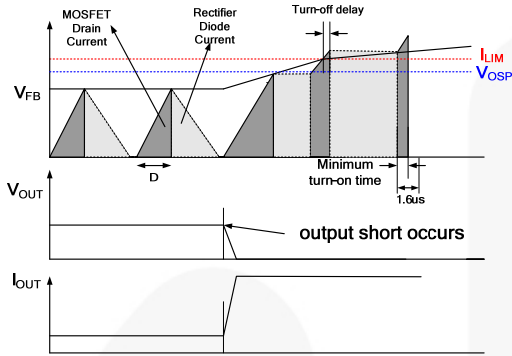


Figure 20. Output Short Waveforms (OSP)

Soft-Start

The FPS has an internal soft-start circuit that slowly increases the feedback voltage, together with the SenseFET current after it starts. The typical soft-start time is 20ms, as shown in Figure 21, where progressive increments of the SenseFET current are allowed during the startup phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. Soft-start helps prevent transformer saturation and reduce the stress on the secondary diode.

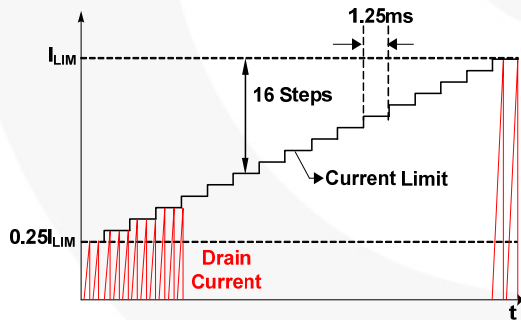


Figure 21. Internal Soft-Start

Burst Operation

To minimize power dissipation in standby mode, the FPS enters burst mode. As the load decreases, the feedback voltage decreases. As shown in Figure 22, the device automatically enters burst mode when the feedback voltage drops below V_{BURH} . Switching continues until the feedback voltage drops below V_{BURL} . At this point, switching stops and the output voltages drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} , switching resumes. The feedback

voltage then falls and the process repeats. Burst mode alternately enables and disables switching of the SenseFET and reduces switching loss in standby mode.

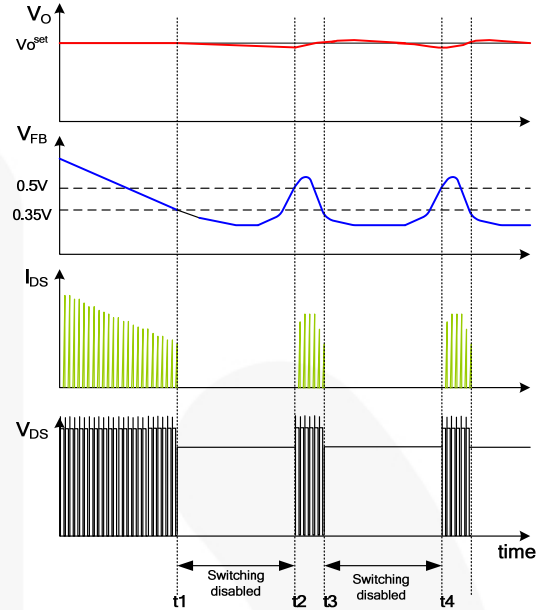


Figure 22. Burst-Mode Operation

Adjusting Peak Current Limit

As shown in Figure 23, a combined 6k Ω internal resistance is connected to the non-inverting lead on the PWM comparator. An external resistance of R_x on the current limit pin forms a parallel resistance with the 6k Ω when the internal diodes are biased by the main current source of 400 μ A. For example, FSL136HR has a typical SenseFET peak current limit (I_{LIM}) of 2.15A. I_{LIM} can be adjusted to 1.5A by inserting R_x between the I_{PK} pin and the ground. The value of the R_x can be estimated by the following equations:

$$2.15A \cdot 1.5A = 6k\Omega \cdot Xk\Omega \quad (1)$$

$$X = R_x \parallel 6k\Omega \quad (2)$$

where X is the resistance of the parallel network.

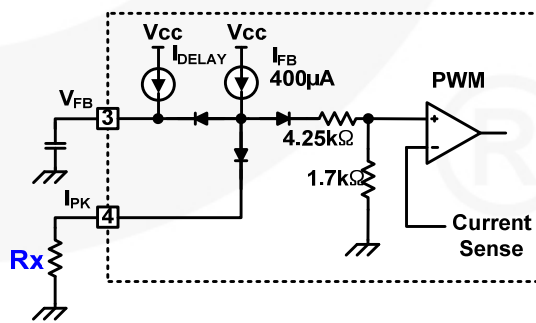






Figure 23. Peak Current Limit Adjustment



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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