

FM1608

64Kb Byte-wide FRAM Memory



Features

64K bit Ferroelectric Nonvolatile RAM

- Organized as 8,192 x 8 bits
- High endurance 10 Billion (10^{10}) read/writes
- 10 year data retention at 85° C
- NoDelay™ write
- Advanced high-reliability ferroelectric process

Superior to BBSRAM Modules

- No battery concerns
- Monolithic reliability
- True surface mount solution, no rework steps
- Superior for moisture, shock, and vibration
- Resistant to negative voltage undershoots

SRAM & EEPROM Compatible

- JEDEC 8Kx8 SRAM & EEPROM pinout
- 120 ns access time
- 180 ns cycle time
- Equal access & cycle time for reads and writes

Low Power Operation

- 15 mA active current
- 20 μ A standby current

Industry Standard Configuration

- Industrial temperature -40° C to +85° C
- 28-pin SOP or DIP

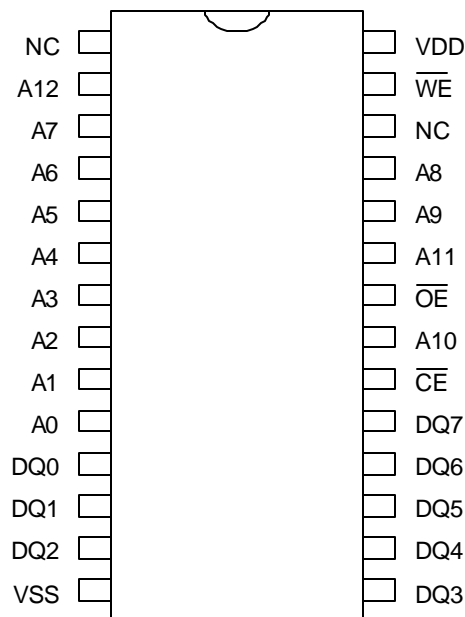
Description

The FM1608 is a 64-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile but operates in other respects as a RAM. It provides data retention for 10 years while eliminating the reliability concerns, functional disadvantages and system design complexities of battery-backed SRAM. Its fast write and high write endurance make it superior to other types of nonvolatile memory.

In-system operation of the FM1608 is very similar to other RAM based devices. Memory read- and write-cycles require equal times. The FRAM memory, however, is nonvolatile due to its unique ferroelectric memory process. Unlike BBSRAM, the FM1608 is a truly monolithic nonvolatile memory. It provides the same functional benefits of a fast write without the serious disadvantages associated with modules and batteries or hybrid memory solutions.

These capabilities make the FM1608 ideal for nonvolatile memory applications requiring frequent or rapid writes in a byte-wide environment. The availability of a true surface-mount package improves the manufacturability of new designs, while the DIP package facilitates simple design retrofits. The FM1608 offers guaranteed operation over an industrial temperature range of -40°C to +85°C.

Pin Configuration



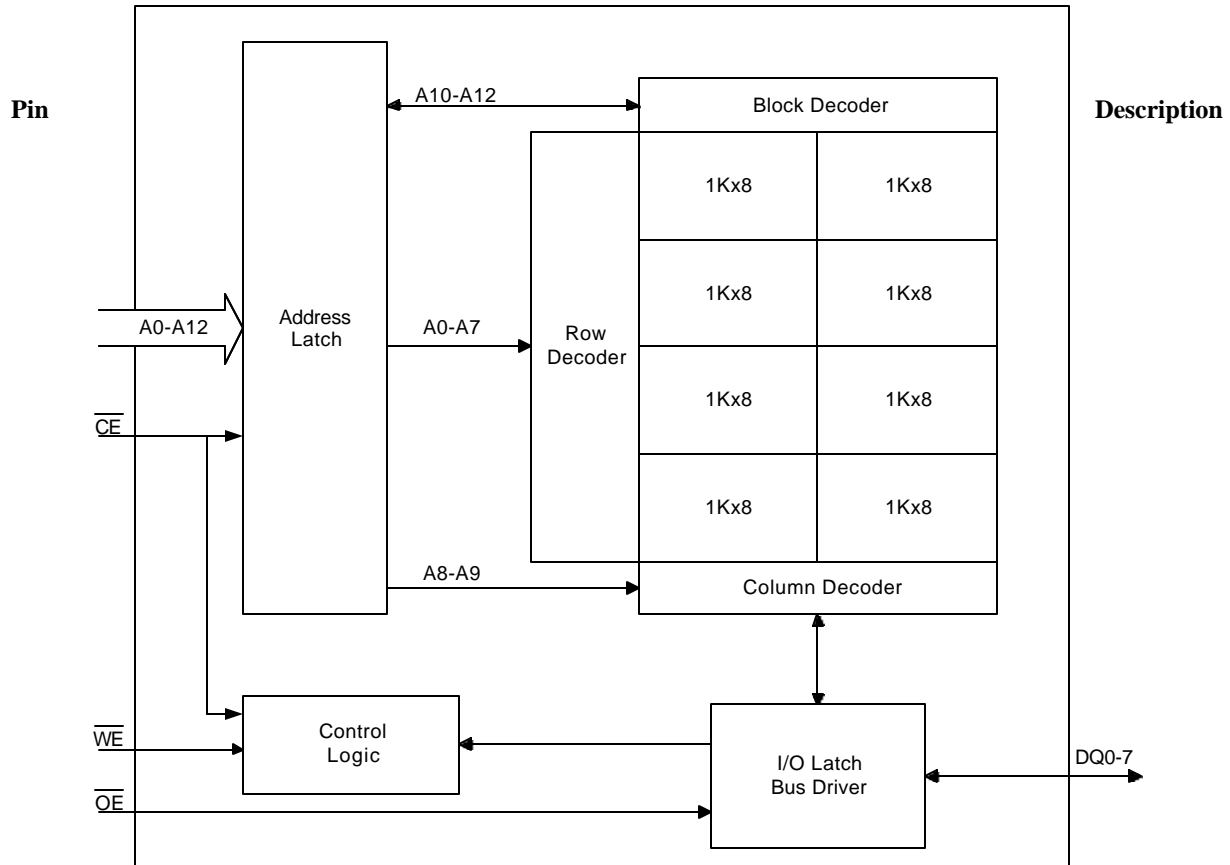
Ordering Information

FM1608-120-P	120 ns access, 28-pin plastic DIP
FM1608-120-S	120 ns access, 28-pin SOP

This data sheet contains design specifications for product development. These specifications may change in any manner without notice

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Figure 1. Block Diagram



Pin Name	Pin Number	I/O	Pin Description
A0-A12	2-10, 21, 23-25	I	Address. The 13 address lines select one of 8,192 bytes in the FRAM array. The address value will be latched on the falling edge of \overline{CE} .
DQ0-7	11-13, 15-19	I/O	Data. 8-bit bi-directional data bus for accessing the FRAM array.
\overline{CE}	20	I	Chip Enable. \overline{CE} selects the device when low. The falling edge of \overline{CE} causes the address to be latched internally. Address changes that occur after \overline{CE} goes low will be ignored until the next falling edge occurs.
\overline{OE}	22	I	Output Enable. When \overline{OE} is low the FM1608 drives the data bus when valid data is available. Taking \overline{OE} high causes the DQ pins to be tri-stated.
\overline{WE}	27	I	Write Enable. Taking \overline{WE} low causes the FM1608 to write the contents of the data bus to the address location latched by the falling edge of \overline{CE} .
VDD	28	I	Supply Voltage. 5V
VSS	14	I	Ground.

Functional Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	Function
H	X	X	Standby/Precharge
\Downarrow	X	X	Latch Address
L	H	L	Read
L	L	X	Write

Overview

The FM1608 is a byte-wide FRAM memory. The memory array is logically organized as 8,192 x 8 and is accessed using an industry standard parallel interface. The FM1608 is inherently nonvolatile via its unique ferroelectric process. All data written to the part is immediately nonvolatile with no delay. Functional operation of the FRAM memory is similar to SRAM type devices. The major operating difference between the FM1608 and an SRAM (beside nonvolatile storage) is that the FM1608 latches the address on the falling edge of /CE.

Memory Architecture

Users access 8,192 memory locations each with 8 data bits through a parallel interface. The complete address of 13-bits specifies each of the 8,192 bytes uniquely. Internally, the memory array is organized into 8 blocks of 1Kb each. The 3 most-significant address lines decode one of 8 blocks. This block segmentation has no effect on operation, however the user may wish to group data into blocks by its endurance requirements as explained in a later section.

The access and cycle time are the same for read and write memory operations. Writes occur immediately at the end of the access with no delay. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. A pre-charge operation, where /CE goes inactive, is a part of every memory cycle. Thus unlike SRAM, the FM1608 access and cycle times are not equal.

Note that the FM1608 has no special power-down demands. It will not block user access and it contains no power-management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that VDD is within data sheet tolerances to prevent incorrect operation.

Memory Operation

The FM1608 is designed to operate in a manner very similar to other byte-wide memory products. For users familiar with BBSRAM, the performance is comparable but the byte-wide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the obvious differences result from the higher write performance of FRAM technology including NoDelay writes and much higher write endurance.

Read Operation

A read operation begins on the falling edge of /CE. At this time, the address bits are latched and a memory

cycle is initiated. Once started, a complete memory cycle must be completed internally regardless of the state of /CE. Data becomes available on the bus after the access time has been satisfied.

After the address has been latched, the address value may change upon satisfying the hold time parameter. Unlike an SRAM, changing address values will have no effect on the memory operation after the address is latched.

The FM1608 will drive the data bus when /OE is asserted to a low state. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients due to invalid data. When /OE is inactive the data bus will remain tri-stated.

Write Operation

Writes occur in the FM1608 in the same time interval as reads. The FM1608 supports both /CE and /WE controlled write cycles. In all cases, the address is latched on the falling edge of /CE.

In a /CE controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the part begins the memory cycle as a write. The FM1608 will not drive the data bus regardless of the state of /OE.

In a /WE controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls after the falling edge of /CE. Therefore the memory cycle begins as a read. The data bus will be driven according to the state of /OE until /WE falls. The timing of both /CE and /WE controlled write cycles is shown in the electrical specifications.

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever is first. Data set-up time, as shown in the electrical specifications, indicates the interval during which data cannot change prior to the end of the write access.

Unlike other truly nonvolatile memory technologies, there is no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus

cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Pre-charge Operation

The pre-charge operation is an internal condition where the state of the memory is prepared for a new access. All memory cycles consist of a memory access and a pre-charge. The pre-charge is user initiated by taking the /CE signal high or inactive. It must remain high for at least the minimum pre-charge timing specification.

The user dictates the beginning of this operation since a pre-charge will not begin until /CE rises. However the device has a maximum /CE low time specification that must be satisfied.

Endurance and Memory Architecture

Data retention is specified in the electrical specifications below. This section elaborates on the relationship between data retention and endurance.

FRAM offers substantially higher write endurance than other nonvolatile memories. Above a certain level, however, the effect of increasing memory accesses on FRAM produces an increase in the soft error rate. There is a higher likelihood of data loss but the memory continues to function properly. This effect becomes significant only after 100 million (1E8) read/write cycles, far more than allowed by other nonvolatile memory technologies.

Endurance is a soft specification. Therefore, the user may operate the device with different levels of cycling for different portions of the memory. For example, critical data needing the highest reliability level could be stored in memory locations that receive comparatively few cycles. Data with frequent changes or shorter-term use could be located in an area receiving many more cycles. A scratchpad area, needing little if any retention can be cycled virtually without limit.

Internally, a FRAM operates with a read and restore mechanism similar to a DRAM. Therefore, each cycle, be it read or write, involves a change of state. The memory architecture is based on an array of rows and columns. Each access causes an endurance cycle for an entire row. Therefore, data locations targeted for substantially differing numbers of cycles should not be located within the same row. To balance the endurance cycles and allow the user the maximum

flexibility, the FM1608 employs a unique memory organization as described below.

The memory array is divided into 8 blocks, each 1Kx8. The 3-upper address lines decode the block selection as shown in Figure 2. Data targeted for significantly different numbers of cycles should be located in separate blocks since memory rows do not extend across block boundaries.

Figure 2. Address Blocks

Block 7	1FFFh 1C00h
Block 6	1BFFh
Block 5	1800h 17FFh
Block 4	1400h 13FFh
Block 3	1000h 0FFFh
Block 2	0C00h 0BFFh
Block 1	0800h 07FFh
Block 0	0400h 03FFh
	0000h

Each block of 1Kx8 consists of 256 rows and 4 columns. The address lines A0-A7 decode row selection and A8-A9 lines decode column selection. This scheme facilitates a relatively uniform distribution of cycles across the rows of a block. By allowing the address LSBs to decode row selection, the user avoids applying multiple cycles to the same row when accessing sequential data. For example, 256 bytes can be accessed sequentially without accessing the same row twice. In this example, one cycle would be applied to each row. An entire block of 1Kx8 can be read or written with only four cycles applied to each row. Figure 3 illustrates the organization within a memory block.

FRAM Design Considerations

When designing with FRAM for the first time, users of SRAM will recognize a few minor differences. First, bitwise FRAM memories latch each address on the falling edge of chip enable. This allows the address bus to change after starting the memory access. Since every access latches the memory address on the falling edge of /CE, users should not ground it as they might with SRAM.

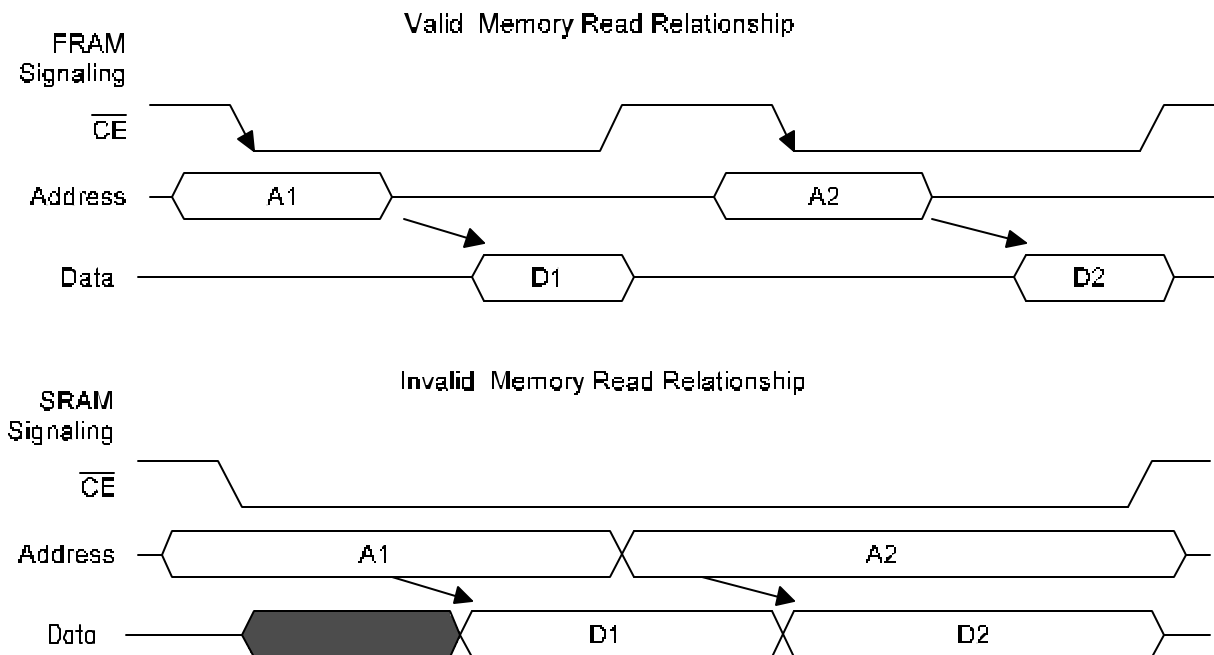
Users that are modifying existing designs to use FRAM should examine the hardware address decoders. Decoders should be modified to qualify addresses with an address valid signal if they do not already. In many cases, this is the only change required. Systems that drive chip enable active, then inactive for each valid address may need no modifications. An example of the target signal relationships is shown in Figure 4. Also shown is a common SRAM signal relationship that will not work for the FM1608.

The main design issue is to create a decoder scheme that will drive /CE active, then inactive for each address. This accomplishes the two goals of latching the new address and creating the precharge period.

A second design consideration relates to the level of VDD during operation. Battery-backed SRAMs are forced to monitor VDD in order to switch to battery backup. They typically block user access below a certain VDD level in order to prevent loading the battery with current demand from an active SRAM. The user can be abruptly cut off from access to the nonvolatile memory in a power down situation with no warning or indication.

FRAM memories do not need this system overhead. The memory will not block access at any VDD level. The user, however, should prevent the processor from accessing memory when VDD is out-of-tolerance. The common design practice of holding a processor in reset when VDD drops is adequate; no special provisions must be taken for FRAM design.

Figure 4. Memory Address Relationships



Electrical Specifications

Absolute Maximum Ratings

<i>Description</i>	<i>Ratings</i>
Ambient storage or operating temperature	-40°C to + 85°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
Lead temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability

DC Operating Conditions TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD	Power Supply	4.5	5.0	5.5	V	1
IDD	VDD Supply Current - Active		5	15	mA	2
ISB	Standby Current - TTL			400	μA	3
ISB	Standby Current - CMOS		7	20	μA	4
ILI	Input Leakage Current			10	μA	5
ILO	Output Leakage Current			10	μA	5
VIL	Input Low Voltage	-1.0		0.8	V	1
VIH	Input High Voltage	2.0		VDD + 1.0	V	1
VOL	Output Low Voltage			0.4	V	1,6
VOH	Output High Voltage	2.4V			V	1,7

Notes

1. Referenced to VSS.
2. VDD = 5.5V, /CE cycling at minimum cycle time. All inputs at CMOS levels, all outputs unloaded.
3. VDD = 5.5V, /CE at VIH, All inputs at TTL levels, all outputs unloaded.
4. VDD = 5.5V, /CE at VIH, All inputs at CMOS levels, all outputs unloaded.
5. VIN, VOUT between VDD and VSS.
6. IOL = 4.2 mA
7. IOH = -2.0 mA

Read Cycle AC Parameters TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Max	Units	Notes
tCE	Chip Enable Access Time (to data valid)		120	ns	
tCA	Chip Enable Active Time	120	10,000	ns	
tRC	Read Cycle Time	180		ns	
tPC	Precharge Time	60		ns	
tAS	Address Setup Time	0		ns	
tAH	Address Hold Time	10		ns	
tOE	Output Enable Access Time		10	ns	
tHZ	Chip Enable to Output High-Z		15	ns	1
tOHZ	Output Enable to Output High-Z		15	ns	1

Write Cycle AC Parameters TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Max	Units	Notes
tCA	Chip Enable Active Time	120	10,000	ns	
tCW	Chip Enable to Write High	120		ns	
tWC	Write Cycle Time	180		ns	
tPC	Precharge Time	60		ns	
tAS	Address Setup Time	0		ns	
tAH	Address Hold Time	10		ns	
tWP	Write Enable Pulse Width	40		ns	
tDS	Data Setup	40		ns	
tDH	Data Hold	0		ns	
tWZ	Write Enable Low to Output High Z		15	ns	1
tWX	Write Enable High to Output Driven	10		ns	1
tHZ	Chip Enable to Output High-Z		15	ns	1
tWS	Write Setup	0		ns	2
tWH	Write Hold	0		ns	2

Notes

- 1 This parameter is periodically sampled and not 100% tested.
- 2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. There is no timing specification associated with this relationship.

Power Cycle Timing TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Units	Notes
tPU	VDD Min to First Access Start	1	μs	
tPD	Last Access Complete to VDD Min	0	μs	

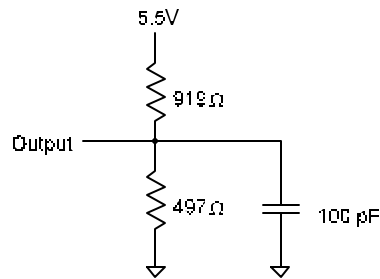
Capacitance TA = 25° C, f=1.0 MHz, VDD = 5V

Symbol	Parameter	Max	Units	Notes
CI/O	Input Output Capacitance	8	pF	
CIN	Input Capacitance	6	pF	

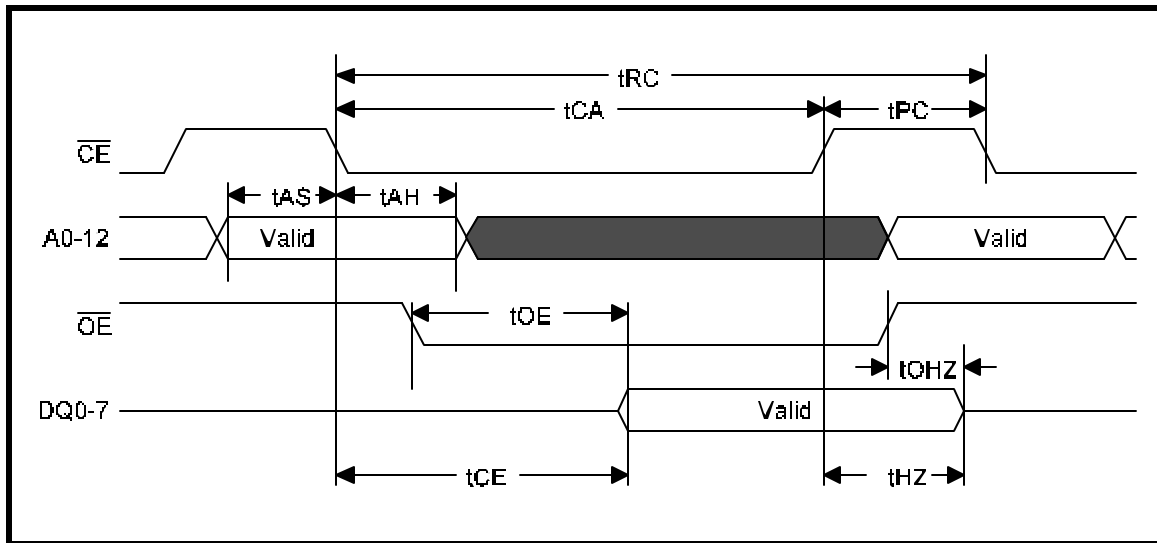
AC Test Conditions

Input Pulse Levels	0 to 3V
Input rise and fall times	10 nS
Input and output timing levels	1.5V

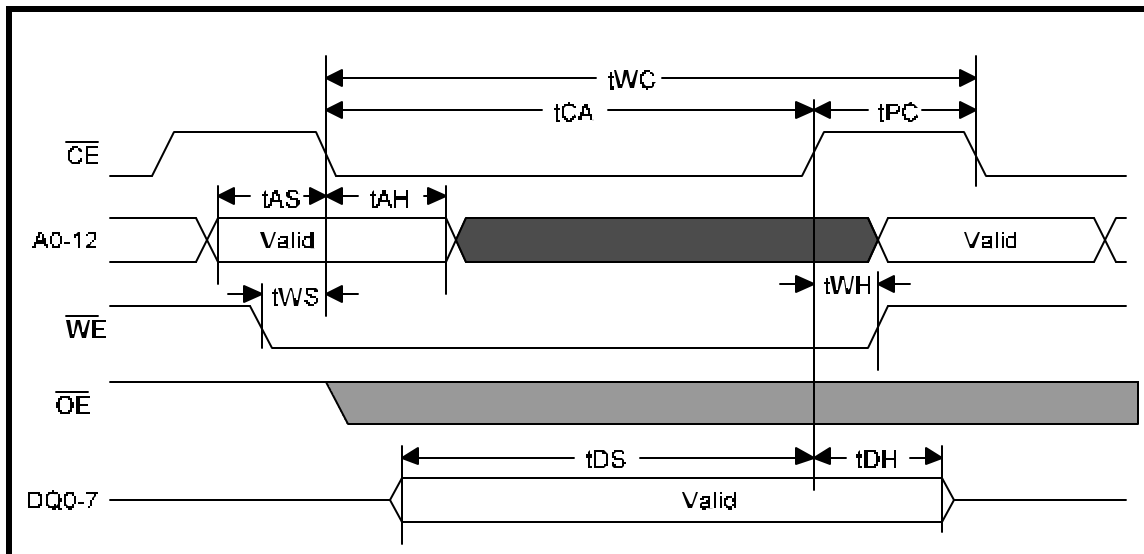
Equivalent AC Load Circuit



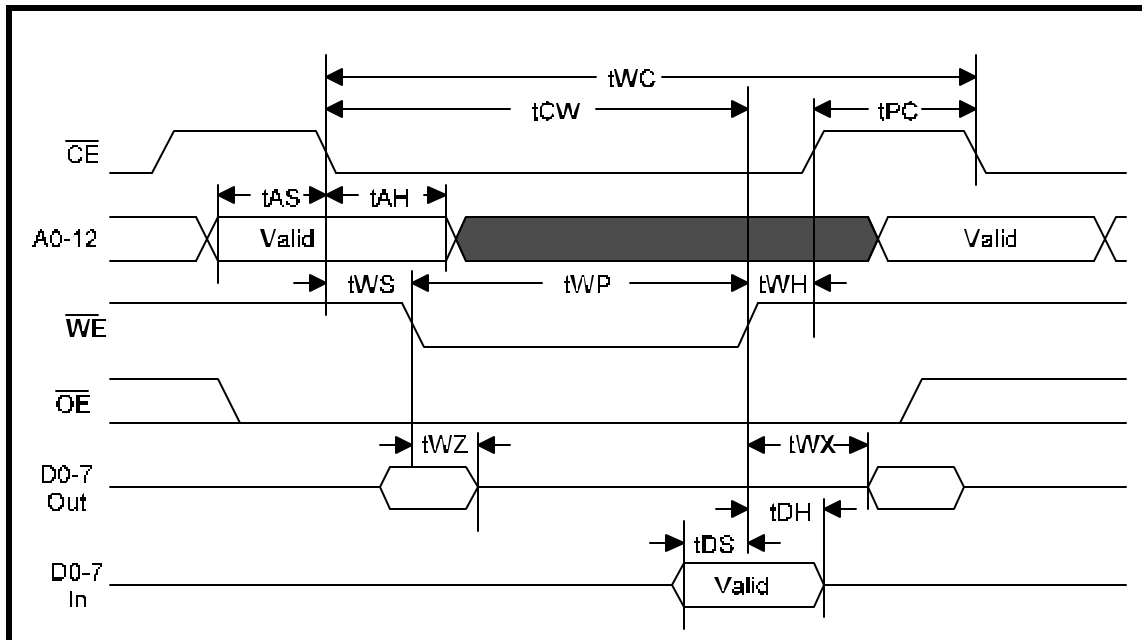
Read Cycle Timing



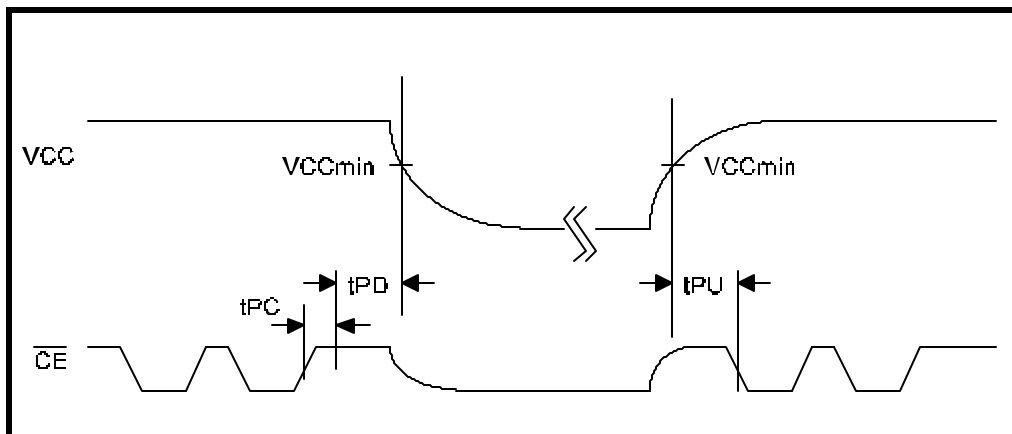
Write Cycle Timing - /CE Controlled Timing



Write Cycle Timing - /WE Controlled Timing



Power Cycle Timing



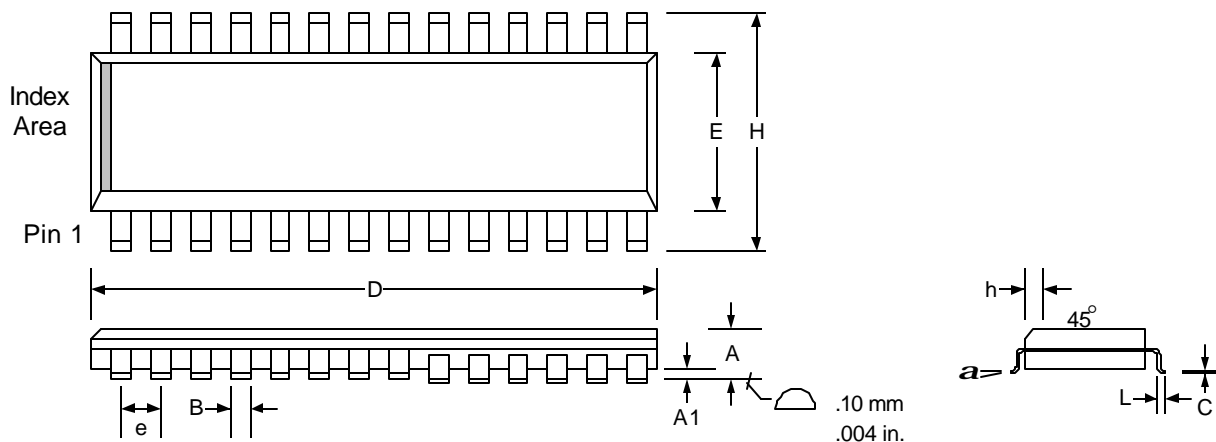
Data Retention TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Parameter	Min	Units	Notes
Data Retention	10	Years	1

Notes

1. Data retention is specified at 85° C. The relationship between retention, temperature, and the associated reliability level is characterized separately.

28-pin SOP JEDEC MS-013

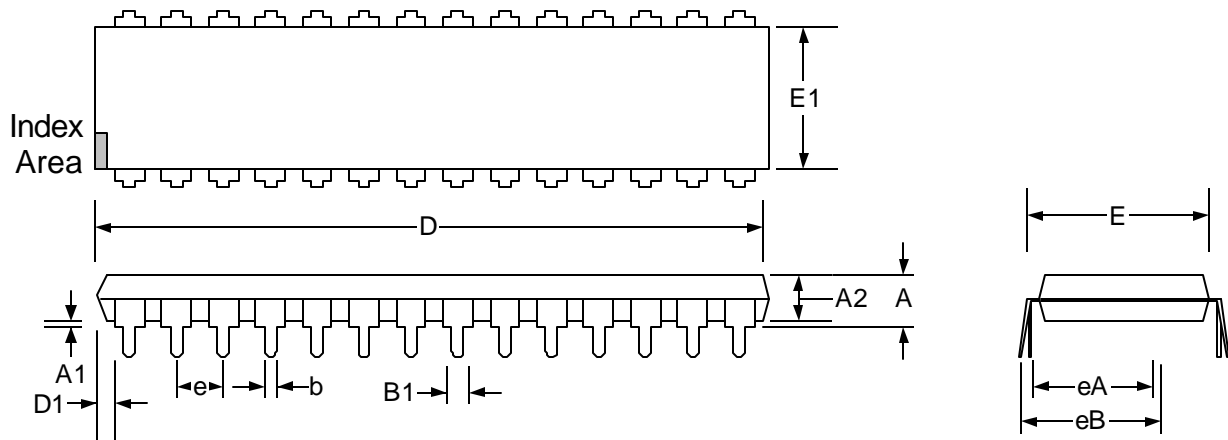


Selected Dimensions

For complete dimensions and notes, refer to JEDEC MS-013
 Controlling dimensions is in millimeters. Conversions to inches are not exact.

Symbol	Dim	Min	Nom.	Max
A	mm in.	2.35 0.0926		2.65 0.1043
A1	mm in.	0.10 0.004		0.30 0.0118
B	mm in.	0.33 0.013		0.51 0.020
C	mm in.	0.23 0.0091		0.32 0.0125
D	mm in.	17.70 0.6969		18.10 0.7125
E	mm in.	7.40 0.2914		7.60 0.2992
e	mm in.		1.27 BSC 0.050 BSC	
H	mm in.	10.00 0.394		10.65 0.419
h	mm in.	0.25 0.010		0.75 0.029
L	mm in.	.40 0.016		1.27 0.050
α		0°		8°

28-pin DIP JEDEC MS-011



Selected Dimensions

For complete dimensions and notes, refer to JEDEC MS-011
 Controlling dimensions is in inches. Conversions to millimeters are not exact.

Symbol	Dim	Min	Nom.	Max
A	in. mm			0.250 6.35
A1	in. mm	0.015 0.39		
A2	in. mm	0.125 3.18		0.195 4.95
B	in. mm	0.014 0.356		0.022 0.558
B1	in. mm	0.030 0.77		0.070 1.77
D	in. mm	1.380 35.1		1.565 39.7
D1	in. mm	0.005 0.13		
E	in. mm	0.600 15.24		0.625 15.87
E1	in. mm	0.485 12.32		0.580 14.73
e	in. mm		0.100 BSC 2.54 BSC	
eA	in. mm		0.600 BSC 15.24 BSC	
eB	in. mm			0.700 17.78
L	in. mm	0.115 2.93		0.200 5.08