



STANDARD
MICROSYSTEMS
CORPORATION

FDC87W22

Power I/O Controller

FEATURES

- 5 Volt Operation
- Floppy Disk Controller (FDC)
 - Compatible with IBM PC/AT Disk Drive Systems
 - Variable Write Pre-Compensation with Track Selectable Capability
 - DMA Enable Logic
 - Non-Burst Mode DMA Option
 - Supports Floppy Disk Drives and Tape Drives
 - Detects All Overrun and Underrun Conditions
 - Data Rate and Drive Control Registers
 - Built-in Address Mark Detection Circuit to Simplify the Read Electronics
 - IBM PC System Address Decoder
 - Supports up to Two Embedded Hard Disk Drives (IDE AT BUS)
 - Single 24 MHz Crystal Input
 - FDD Anti-Virus Functions With Software Write Protect and FDD Write Enable Signal, Write Data Signal Force Inactive
 - Supports up to Four 3.5-Inch or 5.25-Inch Floppy Disk Drives
 - Completely Compatible with Industry Standard 82077
 - 360Kbps/720K/1.2M/1.44M/2.88M Format
 - 250Kbps, 300Kbps, 500Kbps, 1 Mbps Data Transfer Rate
 - Supports Vertical Recording Format
 - 16-Byte Data FIFOs
- Serial Ports
 - Two High-speed 16550 Compatible UARTs with 16-Byte Send/Receive FIFOs
 - MIDI Compatible
 - Fully Programmable Serial-Interface Characteristics:
 - 5, 6, 7 or 8-Bit Characters
 - Even, Odd or No Parity Bit Generation/Detection
 - 1, 1.5 or 2 Stop Bits Generation
 - Internal Diagnostic Capabilities:
 - Loop-Back Controls for Communications Link Fault Isolation
 - Break, Parity, Overrun, Framing Error Simulation
 - Programmable Baud Generator Allows Division of 1.8461 MHz and 24 MHz by 1 to $(2^{16}-1)$
- Parallel Port
 - Compatible with IBM Parallel Port
 - Supports Parallel Port with Bidirectional Lines
 - Supports Enhanced Parallel Port (EPP)
 - Compatible with IEEE 1284 Specification
 - Supports Extended Capabilities Port (ECP)
 - Compatible with IEEE 1284 Specification
 - Extension FDD Mode Supports Disk Drive B Through Parallel Port
 - Extension Adapter Mode Supports Pocket Devices Through Parallel Port

- Extension 2FDD Mode Supports Disk Drives A And B Through Parallel Port
- JOYSTICK Mode Supports Joystick Through Parallel Port
- Programmable Configuration Settings
- Immediate or Automatic Power-Down Mode for Power Management
- ISA Host Interface
- All Hardware Power-On Settings Have Internal Pull-Up or Pull-Down Resistors as Default Value
- Configurable Plug and Play Registers
- Infrared Communication Port
- 100 Pin QFP Package

GENERAL DESCRIPTION

The FDC87W22 integrates a disk drive adapter, serial port (UART), parallel port, IDE bus interface, and game port decoder onto a single chip. The FDC87W22 also has additional powerful features such as configurable plug-and-play registers for the whole chip and infrared support in one of the serial ports.

The disk drive adapter functions of the FDC87W22 include a floppy disk drive controller compatible with the industry standard 82077/765 data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated into the FDC87W22 greatly reduces the number of components required for interfacing with floppy disk drives. The FDC87W22 supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/S, 300 Kb/S, 500 Kb/S, and 1 Mb/S.

The FDC87W22 provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system.

The FDC87W22 supports one PC-compatible printer port. Additional bidirectional I/O

capability is available by hardware control or software programming. The parallel port also supports the Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). The FDC87W22 supports two embedded hard disk drive (AT bus) interfaces and a game port with decoded read/write output. The chip's Extension FDD Mode and Extension 2FDD Mode allow one or two external floppy disk drives to be connected to the computer through the printer interface pins in notebook computer applications.

The Extension Adapter Mode of the FDC87W22 allows pocket devices to be installed through the printer interface pins in notebook computer applications according to a protocol set by SMSC, but with upgraded performance. The JOYSTICK mode allows a joystick to be connected to a parallel port with a signal switching cable. The configuration registers support mode selection, function enable/disable, and power down function selection. Moreover, the configurable PnP registers are compatible with the plug-and-play feature in Windows 95™, which makes system resource allocation more efficient than ever.

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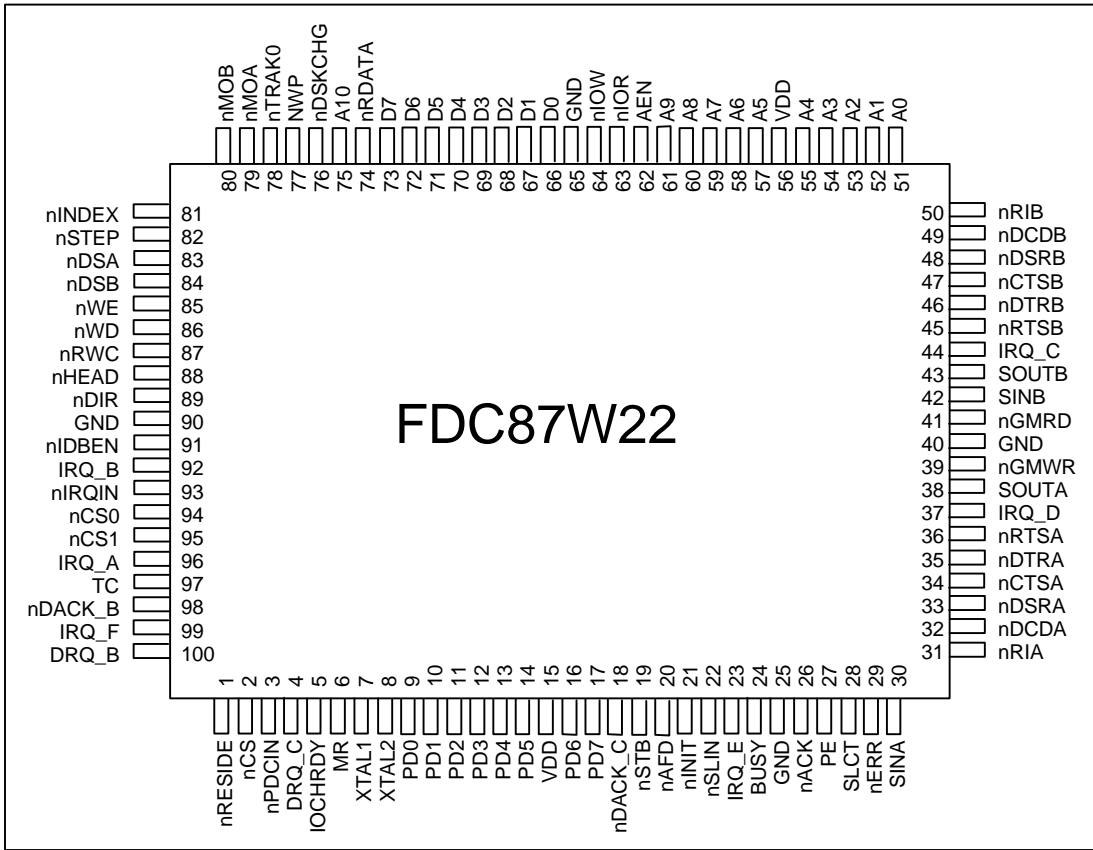
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PIN CONFIGURATION



PIN DESCRIPTION

| | |
|--------|---|
| I/O8t | TTL level bidirectional pin with 8 mA source-sink capability |
| I/O12t | TTL level bidirectional pin with 12 mA source-sink capability |
| I/O24t | TTL level bidirectional pin with 24 mA source-sink capability |
| OUT8t | TTL level output pin with 8 mA source-sink capability |
| OUT12t | TTL level output pin with 12 mA source-sink capability |
| OD12 | Open-drain output pin with 12 mA sink capability |
| OD24 | Open-drain output pin with 24 mA sink capability |
| INt | TTL level input pin |
| INc | CMOS level input pin |
| INcs | CMOS level schmitt-triggered input pin |

Note: Refer to DC CHARACTERISTICS section for details.

Host Interface

| SYMBOL | PIN | I/O | FUNCTION |
|----------------|----------------|--|--|
| D0–D7 | 66-73 | I/O _{24t} | System data bus bits 0-7 |
| A0–A9 | 51-55 57-61 | IN _c | System address bus bits 0-9 |
| A10 | 75 | IN _c | In ECP Mode, this pin is the A10 address input. |
| IOCHRDY | 5 | OD ₂₄ | In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle. |
| MR | 6 | IN _{cs} | Master Reset. Active high. MR is low during normal operations. |
| nCS | 2 | IN _t | Active low chip select signal |
| AEN | 62 | IN _c | System address bus enable |
| nIOR | 63 | IN _{cs} | CPU I/O read signal |
| nIOW | 64 | IN _{cs} | CPU I/O write signal |
| DRQ_B | 100 | OUT _{12t} | DMA request signal B |
| nDACK_B | 98 | IN _c | DMA Acknowledge signal B |
| DRQ_C | 4 | OUT _{12t} | DMA request signal C |
| nDACK_C | 18 | IN _c | DMA Acknowledge signal C |
| TC | 97 | IN _c | Terminal Count. When active, this pin indicates termination of a DMA transfer. |
| nIRQIN | 93 | IN _c | Interrupt request input |
| IRQ_A/ GIO1 | 96 | OUT _{12t} I/O _{12t} | When CR16 Bit 4 (GOIQSEL) = 0: Interrupt request signal A; When CR16 Bit 4 (GOIQSEL) = 1: General Purpose I/O port 1. |

| SYMBOL | PIN | I/O | FUNCTION |
|----------------|-----|--|--|
| IRQ_B/ GIO0 | 92 | OUT _{12t} I/O _{12t} | When CR16 Bit 4 (GOIQSEL) = 0: Interrupt request signal B; When CR16 Bit 4 (GOIQSEL) = 1: General Purpose I/O port 0. |
| IRQ_C | 44 | OUT _{12t} | Interrupt request signal C |
| IRQ_D | 37 | OUT _{12t} | Interrupt request signal D |
| IRQ_E | 23 | OUT _{12t} | Interrupt request signal E |
| IRQ_F | 99 | OUT _{12t} | Interrupt request signal F |
| XTAL1 | 7 | IN _c | XTAL oscillator input |
| XTAL2 | 8 | OUT _{8t} | XTAL oscillator output |

Serial Port Interface

| SYMBOL | PIN | I/O | FUNCTION |
|----------------------------|----------|-------------------|--|
| nCTSA nCTSA | 34 47 | IN _t | Clear To Send is the modem control input. The function of these pins can be tested by reading Bit 4 of the handshake status register. |
| nDSRA nDSRB | 33 48 | IN _t | Data Set Ready. An active low indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| nDCDA nDCDB | 32 49 | IN _t | Data Carrier Detect. An active low indicates the modem or data set has detected a data carrier. |
| nRIA nRIB | 31 50 | IN _t | Ring Indicator. An active low indicates that a ring signal is being received by the modem or data set. |
| SINA SINB/IRRX1 | 30 42 | IN _t | Serial Input. Used to receive serial data from the communication link. |
| SOUTA/ PIRIDE | 38 | I/O _{8t} | UART A Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled up internally and is defined as PIRIDE, which provides the power-on value for CR16 bit 1 (IRIDE). A 47 kΩ is recommended when intends to pull down at power-on reset. |
| SOUTB/ IRTX1/ PGMDRQ | 43 | I/O _{8t} | UART B Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled up internally and is defined as PGMDRQ, which provides the power-on value for CR16 bit 3 (GMDRQ). A 47 kΩ is recommended when intends to pull down at power-on reset. |

| SYMBOL | PIN | I/O | FUNCTION |
|-------------------|------------|-------------------|--|
| nDTRA PHEFRAS | 35 | I/O _{8t} | <p>UART A Data Terminal Ready. An active low informs the modem or data set that the controller is ready to communicate.</p> <p>During power-on reset, this pin is pulled down internally and is defined as PHEFRAS, which provides the power-on value for CR16 bit 0 (HEFRAS). A 47 kΩ is recommended when intends to pull up at power-on reset.</p> |
| nDTRB | 46 | O _{8t} | <p>UART B Data Terminal Ready. An active low informs the modem or data set that controller is ready to communicate.</p> |
| nRTSA PPNPCVS | 36 | I/O _{8t} | <p>UART A Request To Send. An active low informs the modem or data set that the controller is ready to send data.</p> <p>During power-on reset, this pin is pulled up internally and is defined as PPNPCVS, which provides the power-on value for CR16 bit 2 (PNPCVS). A 47 kΩ is recommended when intends to pull down at power-on reset.</p> |
| nRTSB PGOIQSEL | 45 | I/O _{8t} | <p>UART B Request To Send. An active low informs the modem or data set that the controller is ready to send data.</p> <p>During power-on reset, this pin is pulled down internally and is defined as PGOIQSEL, which provides the power-on value for CR16 bit 4 (GOIQSEL). A 47 kΩ is recommended when intends to pull up at power-on reset.</p> |

Game Port/Power Down Interface

in Adapter mode or Portable mode (default is Adapter mode). If Bit 3 of CR16 is 0, pin 39 and 41 are used for DMA A operation.

If Bit 3 of CR16 (GMDRQ) is 1, Bit 4 of CR3 (GMODS0) determines whether the game port is

| SYMBOL | PIN | I/O | FUNCTION |
|-----------------|-----|--|--|
| nGMRD PFDCEN | 41 | OUT _{8t} OUT _{8t} | When CR16 Bit 3 (GMDRQ) = 1: Adapter mode: Game port read control signal. Portable mode: When parallel port is selected as Extension FDD/Extension 2FDD mode, this pin will be active. The active state is dependent on bit 7 of CRA (PFDCACT), and default is low active. When CR16 Bit 3 (GMDRQ) = 0: DMA acknowledge signal A. |
| nDACK_A | | IN _t | |
| nGMWR PEXTEN | 39 | OUT _{8t} OUT _{8t} | When CR16 Bit 3 (GMDRQ) = 1: Adapter mode: Game port write control signal. Portable mode: When a particular extended mode is selected for the parallel port, this pin will be active. The extended modes include Extension Adapter mode, EPP mode, ECP mode, and ECP/EPP mode, which are selected using bit 3 - bit 0 of CRA. The active state is dependent on bit 6 of CRA (PEXTACT); the default is low active. When CR16 Bit 3 (GMDRQ) = 0: DMA request signal A. |
| DRQ_A | | OUT _{8t} | |
| PDCIN | 3 | IN _c | This input pin controls the chip power down. When this pin is active, the clock supply to the chip will be inhibited and the output pins will be tri-stated as defined in CR4 and CR6. The PDCIN is pulled down internally. Its active state is defined by bit 4 of CRA (PDCHACT). Default is high active. |

Multi-Mode Parallel Port

The following pins have eight functions, which are controlled by bits PRTMOD0, PRTMOD1, and PRTMOD2 of CR0 and CR9 (refer to the Extended Functions section).

| SYMBOL | PIN | I/O | FUNCTION |
|---------------|------------|---|---|
| BUSY | 24 | IN _t OD ₁₂ IN _t OD ₁₂ — | <p>PRINTER MODE: BUSY An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nMOB2 This pin is for Extension FDD B; the function of this pin is the same as that of the nMOB pin.</p> <p>EXTENSION ADAPTER MODE: XIRQ This pin is an interrupt request generated by the Extension Adapter and is an active high input.</p> <p>EXTENSION 2FDD MODE: nMOB2 This pin is for Extension FDD A and B; the function of this pin is the same as that of the nMOB pin.</p> <p>JOYSTICK MODE: NC pin.</p> |
| nACK | 26 | IN _t OD ₁₂ IN _t OD ₁₂ — | <p>PRINTER MODE: nACK An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nDSB2 This pin is for the Extension FDD B; its functions are the same as those of the nDSB pin.</p> <p>EXTENSION ADAPTER MODE: XDRQ DMA request generated by the Extension Adapter. An active high input.</p> <p>EXTENSION 2FDD MODE: nDSB2 This pin is for Extension FDD A and B; this function of this pin is the same as that of the nDSB pin.</p> <p>JOYSTICK MODE: NC pin.</p> |

| SYMBOL | PIN | I/O | FUNCTION |
|---------------|------------|--|---|
| PE | 27 | IN _t OD ₁₂ OUT _{12t} OD ₁₂ – | <p>PRINTER MODE: PE</p> <p>An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.</p> <p>Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nWD2</p> <p>This pin is for Extension FDD B; its function is the same as that of the nWD pin.</p> <p>EXTENSION ADAPTER MODE: XA0</p> <p>This pin is system address A0 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: nWD2</p> <p>This pin is for Extension FDD A and B; this function of this pin is the same as that of the nWD pin.</p> <p>JOYSTICK MODE: NC pin.</p> |
| SLCT | 28 | IN _t OD ₁₂ OUT _{12t} OD ₁₂ – | <p>PRINTER MODE: SLCT</p> <p>An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nWE2</p> <p>This pin is for Extension FDD B; its functions are the same as those of the nWE pin.</p> <p>EXTENSION ADAPTER MODE: XA1</p> <p>This pin is system address A1 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: nWE2</p> <p>This pin is for Extension FDD A and B; this function of this pin is the same as that of the nWE pin.</p> <p>JOYSTICK MODE: NC pin.</p> |

| SYMBOL | PIN | I/O | FUNCTION |
|---------------|------------|--|---|
| nERR | 29 | IN _t OD ₁₂ OUT _{12t} OD ₁₂ — | <p>PRINTER MODE: nERR An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nHEAD2 This pin is for Extension FDD B; its function is the same as that of the nHEAD pin.</p> <p>EXTENSION ADAPTER MODE: XA2 This pin is system address A2 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: nHEAD2 This pin is for Extension FDD A and B; its function is the same as that of the nHEAD pin.</p> <p>JOYSTICK MODE: NC pin.</p> |
| nSLIN | 22 | OD ₁₂ OD ₁₂ OUT _{12t} OD ₁₂ OUT _{12t} | <p>PRINTER MODE: nSLIN Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nSTEP2 This pin is for Extension FDD B; its function is the same as that of the nSTEP pin.</p> <p>EXTENSION ADAPTER MODE: XTC This pin is the DMA terminal count for the Extension Adapter. The count is sent by TC directly.</p> <p>EXTENSION 2FDD MODE: nSTEP2 This pin is for Extension FDD A and B; its function is the same as that of the nSTEP pin .</p> <p>JOYSTICK MODE: VDD for joystick.</p> |

| SYMBOL | PIN | I/O | FUNCTION |
|---------------|------------|--|---|
| nINIT | 21 | OD ₁₂ OD ₁₂ OUT _{12t} OD ₁₂ OUT _{12t} | PRINTER MODE: nINIT Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: nDIR2 This pin is for Extension FDD B; its function is the same as that of the nDIR pin. EXTENSION ADAPTER MODE: nXDACK This pin is the DMA acknowledge output for the Extension Adapter; the output is sent directly from nPDACKX. EXTENSION 2FDD MODE: nDIR2 This pin is for Extension FDD A and B; its function is the same as that of the nDIR pin. JOYSTICK MODE: VDD for joystick. |
| nAFD | 20 | OD ₁₂ OD ₁₂ OUT _{12t} OD ₁₂ OUT _{12t} | PRINTER MODE: nAFD An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: nRWC2 This pin is for Extension FDD B; its function is the same as that of the nRWC pin. EXTENSION ADAPTER MODE: nXRD This pin is the I/O read command for the Extension Adapter. When the Extension Adapter base address is written to the Extension Adapter address register, nXRD and nXWR go low simultaneously so that the command register on the Extension Adapter can latch the same base address. EXTENSION 2FDD MODE: nRWC2 This pin is for Extension FDD A and B; its function is the same as that of the nRWC pin. JOYSTICK MODE: VDD for joystick. |

| SYMBOL | PIN | I/O | FUNCTION |
|---------------|------------|--|--|
| nSTB | 19 | OD ₁₂ - OUT _{12t} - OUT _{12t} | <p>PRINTER MODE: nSTB An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: This pin is a tri-state output.</p> <p>EXTENSION ADAPTER MODE: nXWR This pin is the I/O write command for the Extension Adapter. When the Extension Adapter base address is written to the Extension Adapter address register, nXRD and nXWR go low simultaneously so that the command register on the Extension Adapter can latch the same base address.</p> <p>EXTENSION 2FDD MODE: This pin is a tri-state output.</p> <p>JOYSTICK MODE: VDD for joystick.</p> |
| PD0 | 9 | I/O _{24t} IN _t I/O _{24t} IN _t I/O _{24t} | <p>PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nINDEX2 This pin is for Extension FDD B; the function of this pin is the same as that of the nINDEX pin. This pin is pulled high internally.</p> <p>EXTENSION ADAPTER MODE: XD0 This pin is system data bus D0 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: nINDEX2 This pin is for Extension FDD A and B; this function of this pin is the same as nINDEX pin. This pin is pulled high internally.</p> <p>JOYSTICK MODE: JP0 This pin is the paddle 0 input for joystick.</p> |

| SYMBOL | PIN | I/O | FUNCTION |
|---------------|------------|--|---|
| PD1 | 10 | I/O _{24t} IN _t I/O _{24t} IN _t I/O _{24t} | <p>PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nTRAK02 This pin is for Extension FDD B; the function of this pin is the same as that of the nTRAK0 pin. This pin is pulled high internally.</p> <p>EXTENSION ADAPTER MODE: XD1 This pin is system data bus D1 for the Extension Adapter.</p> <p>EXTENSION. 2FDD MODE: nTRAK02 This pin is for Extension FDD A and B; this function of this pin is the same as nTRAK0 pin. This pin is pulled high internally.</p> <p>JOYSTICK MODE: JP1 This pin is the paddle 1 input for joystick.</p> |
| PD2 | 11 | I/O _{24t} IN _t I/O _{24t} IN _t - | <p>PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nWP2 This pin is for Extension FDD B; the function of this pin is the same as that of the nWP pin. This pin is pulled high internally.</p> <p>EXTENSION ADAPTER MODE: XD2 This pin is system data bus D2 for the Extension Adapter.</p> <p>EXTENSION. 2FDD MODE: nWP2 This pin is for Extension FDD A and B; this function of this pin is the same as that of the nWP pin. This pin is pulled high internally.</p> <p>JOYSTICK MODE: NC pin</p> |

| SYMBOL | PIN | I/O | FUNCTION |
|---------------|------------|---|---|
| PD3 | 12 | I/O _{24t} IN _t I/O _{24t} IN _t - | <p>PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nRDATA2 Motor on B for Extension FDD B; the function of this pin is the same as that of the nRDATA pin. This pin is pulled high internally.</p> <p>EXTENSION ADAPTER MODE: XD3 This pin is system data bus D3 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: nRDATA2 This pin is for Extension FDD A and B; this function of this pin is the same as that of the nRDATA pin. This pin is pulled high internally.</p> <p>JOYSTICK MODE: NC pin</p> |
| PD4 | 13 | I/O _{24t} IN _t I/O _{24t} IN _t IN _t | <p>PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: nDSHCHG2 Drive select B for Extension FDD B; the function of this pin is the same as that of nDSHCHG pin. This pin is pulled high internally.</p> <p>EXTENSION ADAPTER MODE: XD4 This pin is system data bus D4 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: nDSKCHG2 This pin is for Extension FDD A and B; this function of this pin is the same as that of the nDSKCHG pin. This pin is pulled high internally.</p> <p>JOYSTICK MODE: JB0 This pin is the button 0 input for the joystick.</p> |

| SYMBOL | PIN | I/O | FUNCTION |
|---------------|------------|--|--|
| PD5 | 14 | I/O _{24t} - I/O _{24t} - IN _t | <p>PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: This pin is a tri-state output.</p> <p>EXTENSION ADAPTER MODE: XD5 This pin is system data bus D5 for the Extension Adapter</p> <p>EXTENSION 2FDD MODE: This pin is a tri-state output.</p> <p>JOYSTICK MODE: JB1 This pin is the button 1 input for the joystick.</p> |
| PD6 | 16 | I/O _{24t} - I/O _{24t} OD ₂₄ - | <p>PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: This pin is a tri-state output.</p> <p>EXTENSION ADAPTER MODE: XD6 This pin is system data bus D6 for the Extension Adapter</p> <p>EXTENSION. 2FDD MODE: nMOA2 This pin is for Extension FDD A; its function is the same as that of the nMOA pin.</p> <p>JOYSTICK MODE: NC pin</p> |
| PD7 | 17 | I/O _{24t} - I/O _{24t} OD ₂₄ - | <p>PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: This pin is a tri-state output.</p> <p>EXTENSION ADAPTER MODE: XD7 This pin is system data bus D7 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: nDSA2 This pin is for Extension FDD A; its function is the same as that of the nDSA pin.</p> <p>JOYSTICK MODE: NC pin</p> |

IDE and FDC Interface

| SYMBOL | PIN | I/O | FUNCTION |
|-------------------|------------|--|--|
| nRESIDE/ IRQ_G | 1 | OUT _{12t} OUT _{12t} | When CR16 Bit 1 (IRIDE) = 0: Active low reset signal for IDE; When CR16 Bit 1 (IRIDE) = 1: Interrupt request signal G. |
| nIDBEN/ IRQ_H | 91 | OUT _{12t} OUT _{12t} | When CR16 Bit 1 (IRIDE) = 0: Active low enable signal for IDE; When CR16 Bit 1 (IRIDE) = 1: Interrupt request signal H. |
| nCS1/ IRTX2 | 95 | OUT _{12t} OUT _{12t} | When CR16 Bit 1 (IRIDE) = 0: This pin is used to select the IDE controller. nCS1 decodes the HDC addresses specified in CR22. When CR16 Bit 1 (IRIDE) = 1: Function as a InfraRed transmission data line. |
| nCS0/ IRRX2 | 94 | OUT _{12t} IN _t | When CR16 Bit 1 (IRIDE) = 0: This pin is used to select the IDE controller. nCS0 decodes HDC addresses specified in CR21. When CR16 Bit 1 (IRIDE) = 1: Function as a InfraRed receiving line. |
| nWE | 85 | OD ₂₄ | Write enable. An open drain output. |
| nDIR | 89 | OD ₂₄ | Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion |
| nHEAD | 88 | OD ₂₄ | Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1 |
| nRWC | 87 | OD ₂₄ | Reduced write current. This signal can be used on two-speed disk drives to select the transfer rate. An open drain output. Logic 0 = 250 Kb/s Logic 1 = 500 Kb/s When bit 5 of CR9 (EN3MODE) is set to high, the three-mode FDD function is enabled, and the pin will have a different definition. Refer to the EN3MODE bit in CR9. |
| nWD | 86 | OD ₂₄ | Write data. This logic low open drain writes precompensation serial data to the selected FDD. An open drain output. |
| nSTEP | 82 | OD ₂₄ | Step output pulses. This active low open drain output produces a pulse to move the head to another track. |

| SYMBOL | PIN | I/O | FUNCTION |
|---------|------------------|------------------|--|
| nINDEX | 81 | IN _{CS} | This schmitt input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| nTRAK0 | 78 | IN _{CS} | Track 0. This schmitt input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| nWP | 77 | IN _{CS} | Write protected. This active low schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| nRDATA | 74 | IN _{CS} | The read data input signal from the FDD. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| nDSKCHG | 76 | IN _{CS} | Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| nMOA | 79 | OD ₂₄ | Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output. |
| nMOB | 80 | OD ₂₄ | Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output. |
| nDSA | 83 | OD ₂₄ | Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output. |
| nDSB | 84 | OD ₂₄ | Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output. |
| VDD | 15, 56 | | +5 power supply for the digital circuitry |
| GND | 25, 40 65, 90 | | Ground |

FDC FUNCTIONAL DESCRIPTION

FDC87W22 FDC

The floppy disk controller of the FDC87W22 integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to 1 M bits/sec data rate.

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

AT Interface

The interface consists of the standard asynchronous signals: nRD, nWR, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or

PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

$$\text{THRESHOLD \#} \times (1/\text{DATA/RATE}) * 8 - 1.5 \mu\text{S} = \text{DELAY}$$

| FIFO THRESHOLD | MAXIMUM DELAY TO SERVICING AT 500K BPS |
|----------------|--|
| | Data Rate |
| 1 Byte | $1 \times 16 \mu\text{S} - 1.5 \mu\text{S} = 14.5 \mu\text{S}$ |
| 2 Byte | $2 \times 16 \mu\text{S} - 1.5 \mu\text{S} = 30.5 \mu\text{S}$ |
| 8 Byte | $8 \times 16 \mu\text{S} - 1.5 \mu\text{S} = 6.5 \mu\text{S}$ |
| 15 Byte | $15 \times 16 \mu\text{S} - 1.5 \mu\text{S} = 238.5 \mu\text{S}$ |
| FIFO THRESHOLD | MAXIMUM DELAY TO SERVICING AT 1M BPS |
| | Data Rate |
| 1 Byte | $1 \times 8 \mu\text{S} - 1.5 \mu\text{S} = 6.5 \mu\text{S}$ |
| 2 Byte | $2 \times 8 \mu\text{S} - 1.5 \mu\text{S} = 14.5 \mu\text{S}$ |
| 8 Byte | $8 \times 8 \mu\text{S} - 1.5 \mu\text{S} = 62.5 \mu\text{S}$ |
| 15 Byte | $15 \times 8 \mu\text{S} - 1.5 \mu\text{S} = 118.5 \mu\text{S}$ |

At the start of a command the FIFO is always disabled and command parameters must be sent based upon the RQM and DIO bit settings in the main status register. When the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data are not transferred.

An overrun and underrun will terminate the current command and the data transfer. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting nDACK and addresses need not be valid.

Note that if the DMA controller is programmed to function in verify mode a pseudo read is performed by the FDC based only on nDACK. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled the above operation is performed by using the new VERIFY command. No DMA operation is needed.

Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires a 1 Mbps data rate for the FDC. At this data rate the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

FDC Core

The FDC87W22 FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-

byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

FDC Commands

Command Symbol Descriptions:

| | |
|----------|---|
| C: | Cylinder number 0 - 256 |
| D: | Data Pattern |
| DIR: | Step Direction DIR = 0, step out DIR = 1, step in |
| DS0: | Disk Drive Select 0 |
| DS1: | Disk Drive Select 1 |
| DTL: | Data Length |
| EC: | Enable Count |
| EOT: | End of Track |
| EFIFO: | Enable FIFO |
| EIS: | Enable Implied Seek |
| EOT: | End of track |
| FIFOTHR: | FIFO Threshold |
| GAP: | Gap length selection |
| GPL: | Gap Length |
| H: | Head number |
| HDS: | Head number select |
| HLT: | Head Load Time |
| HUT: | Head Unload Time |
| LOCK: | Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset |
| MFM: | MFM or FM Mode |
| MT: | Multitrack |
| N: | The number of data bytes written in a sector |
| NCN: | New Cylinder Number |
| ND: | Non-DMA Mode |
| OW: | Overwritten |
| PCN: | Present Cylinder Number |
| POLL: | Polling Disable |
| PRETRK: | Precompensation Start Track Number |
| R: | Record |
| RCN: | Relative Cylinder Number |
| R/W: | Read/Write |
| SC: | Sector/per cylinder |
| SK: | Skip deleted data address mark |
| SRT: | Step Rate Time |
| ST0: | Status Register 0 |
| ST1: | Status Register 1 |
| ST2: | Status Register 2 |
| ST3: | Status Register 3 |
| WG: | Write gate alters timing of WE |

(1) Read Data

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----------------|-----------------|-----|----|----|----|-----|-----|-----|---|
| Command | W | MT | MFM | SK | 0 | 0 | 1 | 1 | 0 | Command codes Sector ID information prior to command execution |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- C ----- | | | | | | | | |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | |
| W | ----- DTL ----- | | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution Sector ID information after command execution |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(2) Read Deleted Data

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----------------|-----------------|-----|----|----|----|-----|-----|-----|---|
| Command | W | MT | MFM | SK | 0 | 1 | 1 | 0 | 0 | Command codes Sector ID information prior to command execution |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- C ----- | | | | | | | | |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | |
| W | ----- DTL ----- | | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution Sector ID information after command execution |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(3) Read A Track

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----------------|-----------------|-----|----|----|----|-----|-----|-----|--|
| Command | W | 0 | MFM | 0 | 0 | 0 | 0 | 1 | 0 | Command codes Sector ID information prior to command execution |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- C ----- | | | | | | | | |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | |
| W | ----- DTL ----- | | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution Sector ID information after command execution |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(4) Read ID

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|-----------------|-----|----|----|----|-----|-----|-----|--|
| Command | W | 0 | MFM | 0 | 0 | 1 | 0 | 1 | 0 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| Execution | | | | | | | | | | The first correct ID information on the cylinder is stored in Data Register |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution Disk status after the command has been completed |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(5) Verify

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|---------------------------------------|-----|----|----|----|-----|-----|-----|---|
| Command | W | MT | MFM | SK | 1 | 0 | 1 | 1 | 0 | Command codes Sector ID information prior to command execution |
| | W | EC | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- C ----- | | | | | | | | |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- ----- DTL/SC ----- | | | | | | | | |
| Execution | | | | | | | | | | No data transfer takes place |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution Sector ID information after command execution |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(6) Version

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|----|----|----|----|----|----|----|----|---------------------|
| Command | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Command code |
| Result | R | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Enhanced controller |

(7) Write Data

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS | |
|-----------|---------------|-----------------|-----|----|----|----|-----|-----|-----|---|--|
| Command | W | MT | MFM | 0 | 0 | 0 | 1 | 0 | 1 | Command codes Sector ID information prior to Command execution | |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | | |
| | W | ----- C ----- | | | | | | | | | |
| | W | ----- H ----- | | | | | | | | | |
| | W | ----- R ----- | | | | | | | | | |
| | W | ----- N ----- | | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | | |
| | W | ----- DTL ----- | | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system | |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after Command execution Sector ID information after Command execution | |
| | R | ----- ST1 ----- | | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | | |
| | R | ----- C ----- | | | | | | | | | |
| | R | ----- H ----- | | | | | | | | | |
| | R | ----- R ----- | | | | | | | | | |
| R | ----- N ----- | | | | | | | | | | |

(8) Write Deleted Data

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS | |
|-----------|-----------------|-----------------|-----|----|----|----|-----|-----|-----|---|---|
| Command | W | MT | MFM | 0 | 0 | 1 | 0 | 0 | 1 | Command codes Sector ID information prior to command execution | |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | | |
| | W | ----- C ----- | | | | | | | | | |
| | W | ----- H ----- | | | | | | | | | |
| | W | ----- R ----- | | | | | | | | | |
| | W | ----- N ----- | | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | | |
| W | ----- DTL ----- | | | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system | |
| Result | R | ----- ST0 ----- | | | | | | | | | Status information after command execution Sector ID information after command execution |
| | R | ----- ST1 ----- | | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | | |
| | R | ----- C ----- | | | | | | | | | |
| | R | ----- H ----- | | | | | | | | | |
| | R | ----- R ----- | | | | | | | | | |
| | R | ----- N ----- | | | | | | | | | |

(9) Format A Track

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS | |
|-----------------------------------|-----|-----------------------|-----|----|----|----|-----|-----|-----|---|--|
| Command | W | 0 | MFM | 0 | 0 | 1 | 1 | 0 | 1 | Command codes Bytes/Sector Sectors/Cylinder Gap 3 Filler Byte | |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | | |
| | W | ----- N ----- | | | | | | | | | |
| | W | ----- SC ----- | | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | | |
| | W | ----- D ----- | | | | | | | | | |
| Execution for Each Sector Repeat: | W | ----- C ----- | | | | | | | | | Input Sector Parameters |
| | W | ----- H ----- | | | | | | | | | |
| | W | ----- R ----- | | | | | | | | | |
| | W | ----- N ----- | | | | | | | | | |
| Result | R | ----- ST0 ----- | | | | | | | | | Status information after command execution |
| | R | ----- ST1 ----- | | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | | |
| | R | ----- Undefined ----- | | | | | | | | | |
| | R | ----- Undefined ----- | | | | | | | | | |
| | R | ----- Undefined ----- | | | | | | | | | |
| | R | ----- Undefined ----- | | | | | | | | | |

(10) Recalibrate

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|----|----|----|----|----|----|-----|-----|-------------------------------------|
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | 0 | DS1 | DS0 | |
| Execution | | | | | | | | | | Head retracted to Track 0 Interrupt |

(11) Sense Interrupt Status

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|-----------------|----|----|----|----|----|----|----|--|
| Command | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Command code |
| Result | R | ----- ST0 ----- | | | | | | | | Status information at the end of each seek operation |
| | R | ----- PCN ----- | | | | | | | | |

(12) Specify

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|---------------|----|----|----|---------------|----|----|----|---------------|
| Command | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Command codes |
| | W | -----SRT----- | | | | -----HUT----- | | | | |
| | W | -----HLT----- | | | | | | | | |

(13) Seek

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|-----------------|----|----|----|----|-----|-----|-----|--|
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- NCN ----- | | | | | | | | |
| Execution | R | | | | | | | | | Head positioned over proper cylinder on diskette |

(14) Configure

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|------------------|-----|-------|------|-------------------|----|----|----|----------------------------|
| Command | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Configure information |
| | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | W | 0 | EIS | EFIFO | POLL | -----FIFOTHR----- | | | | |
| | W | -----PRETRK----- | | | | | | | | |
| Execution | | | | | | | | | | Internal registers written |

(15) Relative Seek

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|-----------------|-----|----|----|----|-----|-----|-----|---------------|
| Command | W | 1 | DIR | 0 | 0 | 1 | 1 | 1 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- RCN ----- | | | | | | | | |

(16) Dumpreg

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS | |
|---------|-----|-------------------------|----|------------|----|----|-----------------|--------|----|--------------------------|--|
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | Registers placed in FIFO | |
| Result | R | ----- PCN-Drive 0----- | | | | | | | | | |
| | R | ----- PCN-Drive 1 ----- | | | | | | | | | |
| | R | ----- PCN-Drive 2----- | | | | | | | | | |
| | R | ----- PCN-Drive 3 ----- | | | | | | | | | |
| | R | -----SRT ----- | | | | | ----- HUT ----- | | | | |
| | R | ----- HLT ----- | | | | | ND | | | | |
| | R | ----- SC/EOT ----- | | | | | | | | | |
| | R | LOCK 0 | | D3 | D2 | D1 | D0 | GAP WG | | | |
| | R | 0 EIS | | EFIFO POLL | | | FIFOTHR ----- | | | | |
| | R | -----PRETRK ----- | | | | | | | | | |

(17) Perpendicular Mode

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|----|----|----|----|----|----|--------|----|--------------|
| Command | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Command Code |
| | W | OW | 0 | D3 | D2 | D1 | D0 | GAP WG | | |

(18) Lock

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|------|----|----|------|----|----|----|----|--------------|
| Command | W | LOCK | 0 | 0 | 1 | 0 | 1 | 0 | 0 | Command Code |
| Result | R | 0 | 0 | 0 | LOCK | 0 | 0 | 0 | 0 | |

(19) Sense Drive Status

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|-----------------|----|----|----|----|-----|-----|-----|-------------------------------------|
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Command Code |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| Result | R | ----- ST3 ----- | | | | | | | | Status information about disk drive |

(20) Invalid

| PHASE | R/W | D7 D6 D5 D4 D3 D2 D1 D0 | REMARKS |
|---------|-----|---------------------------|--|
| Command | W | ----- Invalid Codes ----- | Invalid codes (no operation - FDC goes into standby state) |
| Result | R | ----- ST0 ----- | ST0 = 80H |

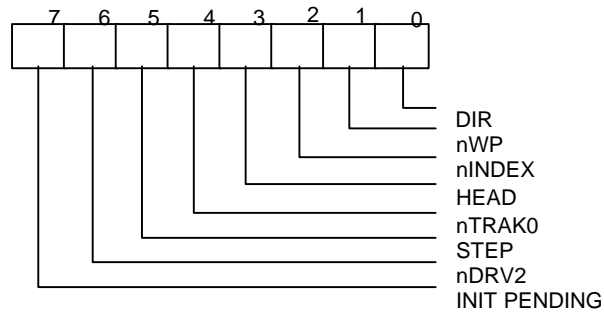
Register Descriptions

There are several status, data, and control registers in FDC87W22. These registers are defined below:

| ADDRESS OFFSET | REGISTER | |
|-------------------|--------------------|--------------------|
| | READ | WRITE |
| base address + 0 | SA REGISTER | |
| base address + 1 | SB REGISTER | |
| base address + 2 | | DO REGISTER |
| base address + 3 | TD REGISTER | TD REGISTER |
| base address + 4 | MS REGISTER | DR REGISTER |
| base address + 5 | DT (FIFO) REGISTER | DT (FIFO) REGISTER |
| base address + 7 | DI REGISTER | CC REGISTER |

Status Register A (SA Register) (Read base address + 0)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

nDRV2 (Bit 6):

0 A second drive has been installed
1 A second drive has not been installed

STEP (Bit 5):

This bit indicates the complement of nSTEP output.

nTRAK0 (Bit 4):

This bit indicates the value of nTRAK0 input.

HEAD (Bit 3):

This bit indicates the complement of nHEAD output.

0 side 0
1 side 1

nINDEX (Bit 2):

This bit indicates the value of nINDEX output.

nWP (Bit 1):

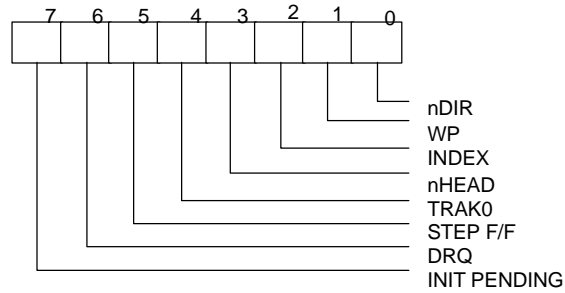
0 disk is write-protected
1 disk is not write-protected

DIR (Bit 0)

This bit indicates the direction of head movement.

0 outward direction
1 inward direction

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRQ (Bit 6):

This bit indicates the value of DRQ output pin.

STEP F/F (Bit 5):

This bit indicates the complement of latched nSTEP output.

TRAK0 (Bit 4):

This bit indicates the complement of nTRAK0 input.

nHEAD (Bit 3):

This bit indicates the value of nHEAD output.

0 side 1

1 side 0

INDEX (Bit 2):

This bit indicates the complement of nINDEX output.

WP (Bit 1):

0 disk is not write-protected

1 disk is write-protected

nDIR(Bit 0)

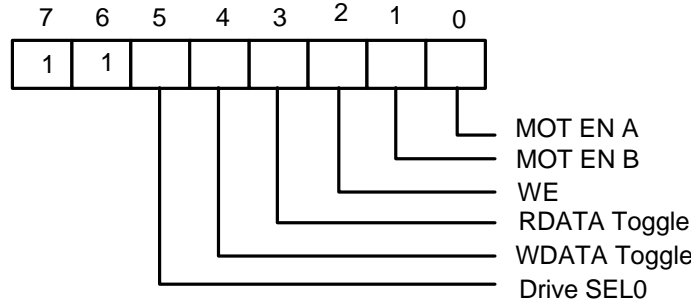
This bit indicates the direction of head movement.

0 inward direction

1 outward direction

Status Register B (SB Register) (Read base address + 1)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



Drive SEL0 (Bit 5):

This bit indicates the status of DO REGISTER bit 0 (drive select bit 0).

WDATA Toggle (Bit 4):

This bit changes state at every rising edge of the nWD output pin.

RDATA Toggle (Bit 3):

This bit changes state at every rising edge of the nRDATA output pin.

WE (Bit 2):

This bit indicates the complement of the nWE output pin.

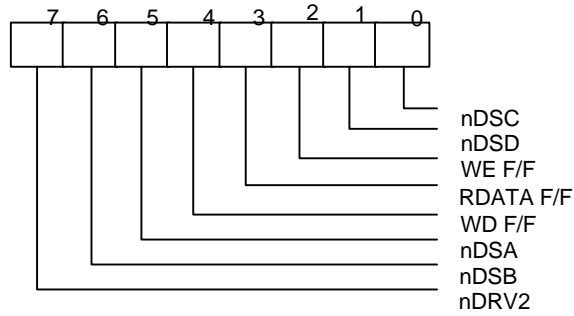
MOT EN B (Bit 1)

This bit indicates the complement of the nMOB output pin.

MOT EN A (Bit 0)

This bit indicates the complement of the nMOA output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



nDRV2 (Bit 7):

- 0 A second drive has been installed
- 1 A second drive has not been installed

nDSB (Bit 6):

This bit indicates the status of nDSB output pin.

nDSA (Bit 5):

This bit indicates the status of nDSA output pin.

WD F/F (Bit 4):

This bit indicates the complement of the latched nWD output pin at every rising edge of the nWD output pin.

RDATA F/F (Bit 3):

This bit indicates the complement of the latched nRDATA output pin .

WE F/F (Bit 2):

This bit indicates the complement of latched nWE output pin.

nDSD (Bit 1):

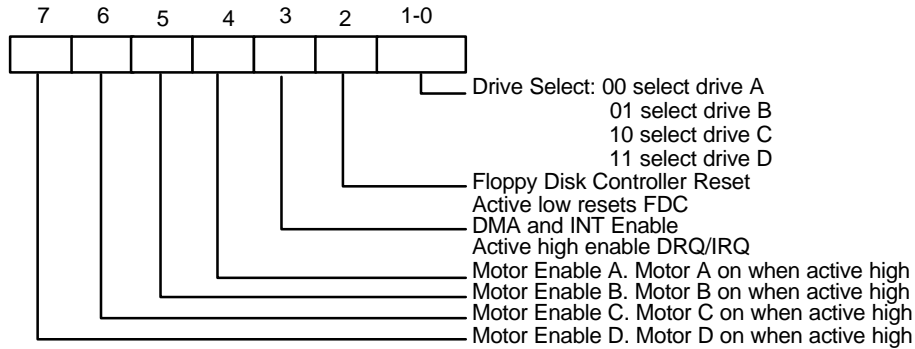
- 0 Drive D has been selected
- 1 Drive D has not been selected

nDSC (Bit 0):

- 0 Drive C has been selected
- 1 Drive C has not been selected

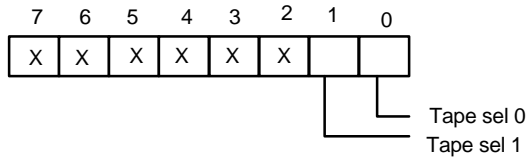
Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and FDC resetting. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

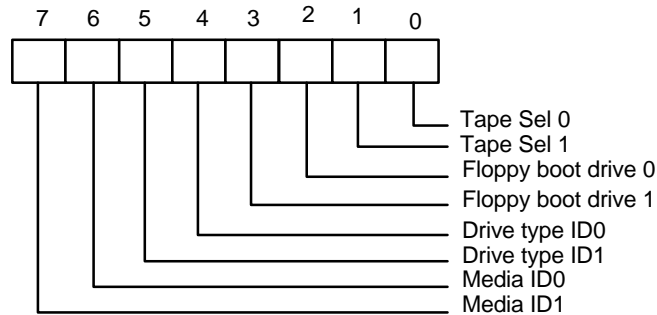


Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information of the floppy disk drive. In normal floppy mode, this register includes only bit 0 and 1. The bit definitions are as follows:



If three mode FDD function is enabled (EN3MODE = 1 in CR9), the bit definitions are as follows:



Media ID1 Media ID0 (Bit 7, 6):

These two bits are read only. These two bits reflect the value of CR8 bit 3, 2.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits of CR7. Which two bits are reflected depends on the last drive selected in the DO REGISTER.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of CR8 bit 1, 0.

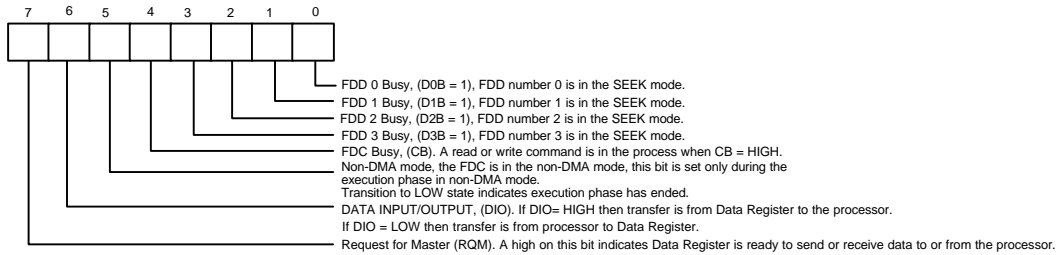
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

| TAPE SEL 1 | TAPE SEL 0 | DRIVE SELECTED |
|------------|------------|----------------|
| 0 | 0 | None |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

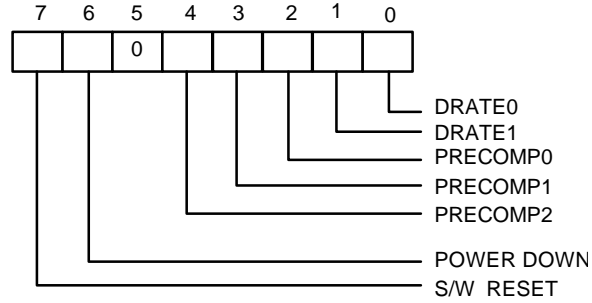
Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:



Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. The data rate of the FDC is programmed by the CC REGISTER for PC-AT and PS/2 Model 30 and PS/2 mode, and not by the DR REGISTER. The real data rate is determined by the most recent write to either of the DR REGISTER or CC REGISTER.



S/W RESET (Bit 7):
This bit is the software reset bit.

POWER-DOWN (Bit 6):
0 FDC in normal mode
1 FDC in power-down mode

PRECOMP2 PRECOMP1 PRECOMP0 (Bit 4, 3, 2):
These three bits select the value of write precompensation. The following tables show the precompensation values for the combination of these bits.

| PRECOM | | | PRECOMPENSATION DELAY |
|--------|---|---|-----------------------|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | Default Delays |
| 0 | 0 | 1 | 41.67 nS |
| 0 | 1 | 0 | 83.34 nS |
| 0 | 1 | 1 | 125.00 nS |
| 1 | 0 | 0 | 166.67 nS |
| 1 | 0 | 1 | 208.33 nS |
| 1 | 1 | 0 | 250.00 nS |
| 1 | 1 | 1 | 0.00 nS (disabled) |

| DATA RATE | DEFAULT PRECOMPENSATION DELAYS |
|-----------|--------------------------------|
| 250 KB/S | 125 nS |
| 300 KB/S | 125 nS |
| 500 KB/S | 125 nS |
| 1 MB/S | 41.67 nS |

DRATE1 DRATE0 (Bit 1, 0):

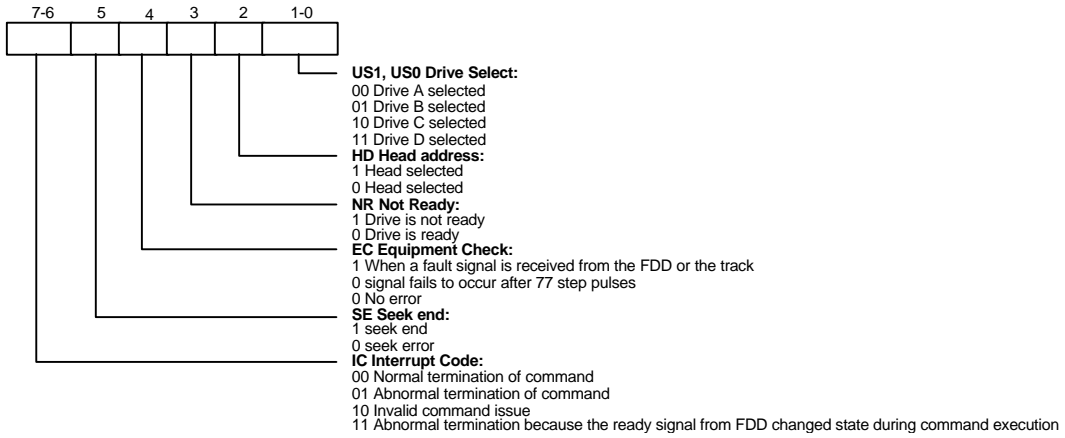
These two bits select the data rate of the FDC and reduced write current control.

- 00 500 KB/S (MFM), 250 KB/S (FM), nRWC = 1.
- 01 300 KB/S (MFM), 150 KB/S (FM), nRWC = 0.
- 10 250 KB/S (MFM), 125 KB/S (FM), nRWC = 0.
- 11 1 MB/S (MFM), Illegal (FM), nRWC = 1.

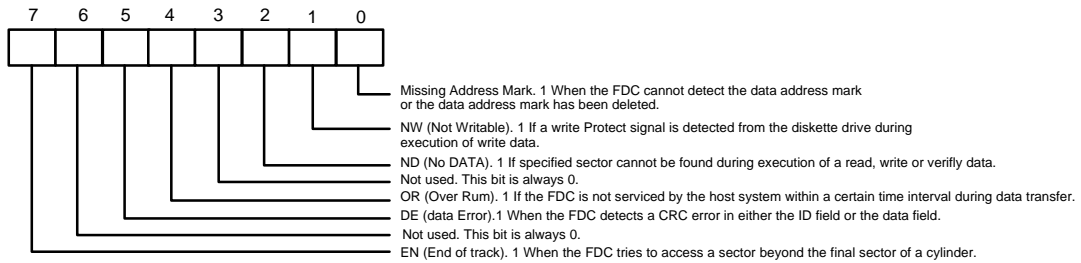
FIFO Register (R/W base address + 5)

The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command. In the FDC87W22, this register defaults to FIFO disabled mode after reset. The FIFO can change its value and enable its operation through the CONFIGURE command.

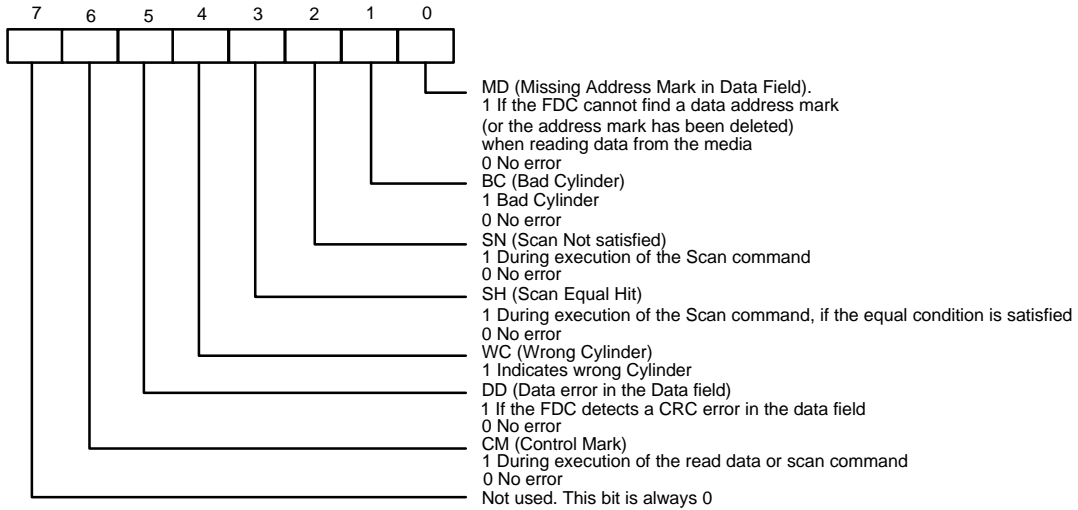
Status Register 0 (ST0)



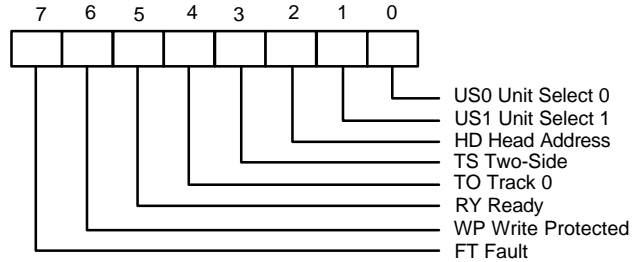
Status Register 1 (ST1)



Status Register 2 (ST2)

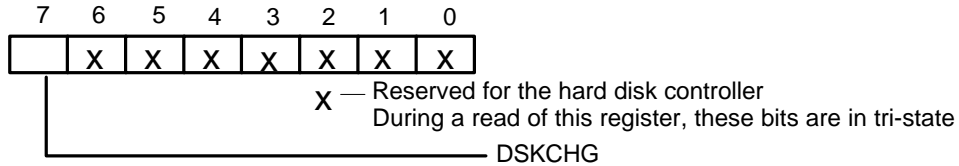


Status Register 3 (ST3)

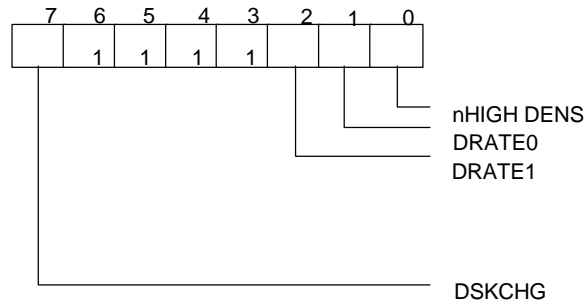


Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit read-only register used for diagnostic purposes. In a PC/XT or AT only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of nDSKCHG, while other bits of the data bus remain in tri-state. Bit definitions are as follows:



In the PS/2 mode, the bit definitions are as follows:



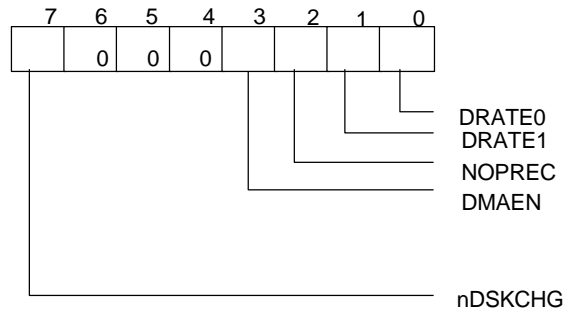
DSKCHG (Bit 7):
This bit indicates the complement of the nDSKCHG input.

Bit 6-3: These bits are always a logic 1 during a read.

DRATE1 DRATE0 (Bit 2, 1):
These two bits select the data rate of the FDC. Refer to the DR register bits 1 and 0 for the settings corresponding to the individual data rates.

nHIGH DENS (Bit 0):
0 500 KB/S or 1 MB/S data rate (high density FDD)
1 250 KB/S or 300 KB/S data rate

In the PS/2 Model 30 mode, the bit definitions are as follows:



DSKCHG (Bit 7):
This bit indicates the status of nDSKCHG input.

Bit 6-4: These bits are always a logic 1 during a read.

DMAEN (Bit 3):

This bit indicates the value of DO REGISTER bit 3.

NOPREC (Bit 2):

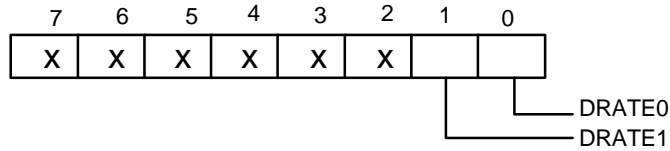
This bit indicates the value of CC REGISTER NOPREC bit.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In the PC/AT and PS/2 mode, the bit definitions are as follows:



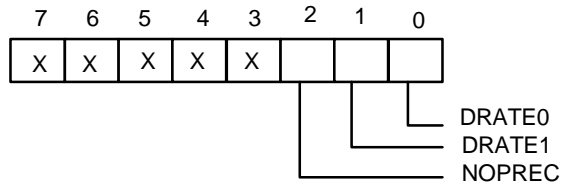
X: Reserved

Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

In the PS/2 Model 30 mode, the bit definitions are as follows:



X: Reserved

Bit 7-3: Reserved. These bits should be set to 0.

NOPREC (Bit 2):

This bit indicates no precompensation. It has no function and can be set by software.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

IDE

The IDE interface is essentially the AT bus ported to the hard disk drive. The hard disk controller resides on the IDE hard disk drive. So the IDE interface provides only chip select

signals and AT bus signals between the IDE hard disk drive and ISA slot. Table 1 shows the IDE registers and their ISA addresses.

Table 1

| I/O ADDRESS OFFSET | REGISTERS | |
|-----------------------|------------------|--------------------|
| | READ | WRITE |
| nCS0 base address + 0 | Data Register | Data Register |
| nCS0 base address + 1 | Error Register | Write-Precomp |
| nCS0 base address + 2 | Sector Count | Sector Count |
| nCS0 base address + 3 | Sector Number | Sector Number |
| nCS0 base address + 4 | Cylinder LOW | Cylinder LOW |
| nCS0 base address + 5 | Cylinder HIGH | Cylinder HIGH |
| nCS0 base address + 6 | SDH Register | SDH Register |
| nCS0 base address + 7 | Status Register | Command Register |
| nCS1 base address + 6 | Alternate Status | Fixed Disk Control |

IDE Decode Description

When the processor selects the addresses which match the ones specified in CR 21, the chip system enables nCS0 = LOW; otherwise,

nCS0 = HIGH. When the processor selects the address which matches the one specified in CR22, the chip system enables nCS1 = LOW; otherwise, nCS1 = HIGH.

UART PORT

Universal Asynchronous Receiver/Transmitter (UART A, UART B)

The UARTs are used to convert parallel data into serial format on the transmit side and convert serial data to parallel format on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to

use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include complete modem control capability and a processor interrupt system that may be software trailed to the computing time required to handle the communication link. The UARTs have a FIFO mode to reduce the number of interrupts presented to the CPU. In each UART, there are 16-byte FIFOs for both receive and transmit mode.

Register Address

TABLE 2 - UART Register Bit Map

| | | BIT NUMBER | | | | |
|-----------------------|--|------------|---|-------------------------------------|------------------------------|------------------------------|
| Register Address Base | | | 0 | 1 | 2 | 3 |
| 8 BDLAB = 0 | Receiver Buffer Register (Read Only) | RBR | RX Data Bit 0 | RX Data Bit 1 | RX Data Bit 2 | RX Data Bit 3 |
| 8 BDLAB = 0 | Transmitter Buffer Register (Write Only) | TBR | TX Data Bit 0 | TX Data Bit 1 | TX Data Bit 2 | TX Data Bit 3 |
| 9 BDLAB = 0 | Interrupt Control Register | ICR | RBR Data Ready Interrupt Enable (ERDRI) | TBR Empty Interrupt Enable (ETBREI) | USR Interrupt Enable (EUSRI) | HSR Interrupt Enable (EHSRI) |
| A | Interrupt Status Register (Read Only) | ISR | "0" if Interrupt Pending | Interrupt Status Bit (0) | Interrupt Status Bit (1) | Interrupt Status Bit (2)** |
| A | UART FIFO Control Register (Write Only) | UFR | FIFO Enable | RCVR FIFO Reset | XMIT FIFO Reset | DMA Mode Select |

| BIT NUMBER | | | | | | |
|-----------------------|-----------------------------|-----|---------------------------------|---------------------------------|----------------------------------|--------------------------|
| Register Address Base | | | 0 | 1 | 2 | 3 |
| B | UART Control Register | UCR | Data Length Select Bit 0 (DLS0) | Data Length Select Bit 1 (DLS1) | Multiple Stop Bits Enable (MSBE) | Parity Bit Enable (PBE) |
| C | Handshake Control Register | HCR | Data Terminal Ready (DTR) | Request to Send (RTS) | Loopback RI Input | IRQ Enable |
| D | UART Status Register | USR | RBR Data Ready (RDR) | Overrun Error (OER) | Parity Bit Error (PBER) | No Stop Bit Error (NSER) |
| E | Handshake Status Register | HSR | CTS Toggling (TCTS) | DSR Toggling (TDSR) | RI Falling Edge (FERI) | DCD Toggling (TDCD) |
| F | User Defined Register | UDR | Bit 0 | Bit 1 | Bit 2 | Bit 3 |
| 8 BDLAB = 1 | Baudrate Divisor Latch Low | BLL | Bit 0 | Bit 1 | Bit 2 | Bit 3 |
| 9 BDLAB = 1 | Baudrate Divisor Latch High | BHL | Bit 8 | Bit 9 | Bit 10 | Bit 11 |

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.

** : These bits are always 0 in 16450 mode.

TABLE 2 - UART Register Bit Map (continued)

| BIT NUMBER | | | | | | |
|-----------------------|--|-----|---------------|---------------|---------------|---------------|
| Register Address Base | | | 4 | 5 | 6 | 7 |
| 8 BDLAB = 0 | Receiver Buffer Register (Read Only) | RBR | RX Data Bit 4 | RX Data Bit 5 | RX Data Bit 6 | RX Data Bit 7 |
| 8 BDLAB = 0 | Transmitter Buffer Register (Write Only) | TBR | TX Data Bit 4 | TX Data Bit 5 | TX Data Bit 6 | TX Data Bit 7 |
| 9 BDLAB = 0 | Interrupt Control Register | ICR | 0 | 0 | 0 | 0 |

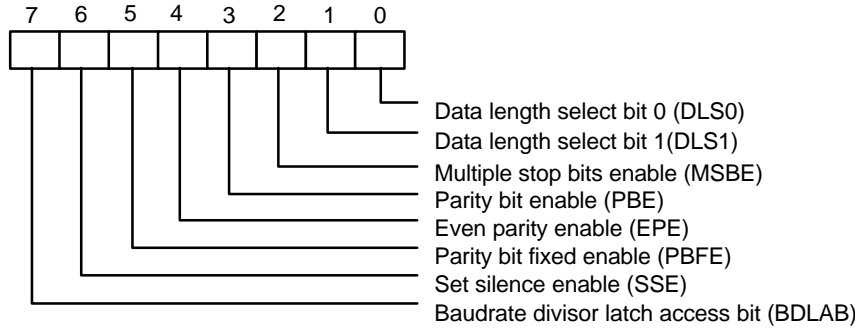
| BIT NUMBER | | | | | | |
|-----------------------|---|-----|----------------------------|--------------------------------|---------------------------------|--|
| Register Address Base | | | 4 | 5 | 6 | 7 |
| A | Interrupt Status Register (Read Only) | ISR | 0 | 0 | FIFOs Enabled ** | FIFOs Enabled ** |
| A | UART FIFO Control Register (Write Only) | UFR | Reserved | Reversed | RX Interrupt Active Level (LSB) | RX Interrupt Active Level (MSB) |
| B | UART Control Register | UCR | Even Parity Enable (EPE) | Parity Bit Fixed Enable (PBFE) | Set Silence Enable (SSE) | Baud rate Divisor Latch Access Bit (BDLAB) |
| C | Handshake Control Register | HCR | Internal Loopback Enable | 0 | 0 | 0 |
| D | UART Status Register | USR | Silent Byte Detected (SBD) | TBR Empty (TBRE) | TSR Empty (TSRE) | RX FIFO Error Indication (RFEI) ** |
| E | Handshake Status Register | HSR | Clear to Send (CTS) | Data Set Ready (DSR) | Ring Indicator (RI) | Data Carrier Detect (DCD) |
| F | User Defined Register | UDR | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
| 8 BDLAB = 1 | Baudrate Divisor Latch Low | BLL | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
| 9 BDLAB = 1 | Baudrate Divisor Latch High | BHL | Bit 12 | Bit 13 | Bit 14 | Bit 15 |

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.

** : These bits are always 0 in 16450 mode.

UART Control Register (UCR) (Read/Write)

The UART Control Register controls and defines the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.



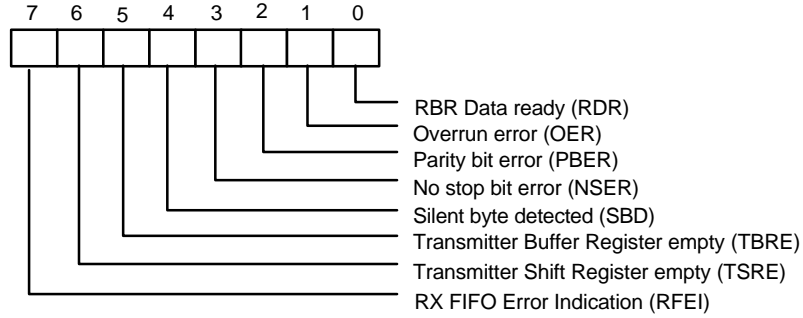
- Bit 7: **BDLAB.** When this bit is set to a logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baudrate generator during a read or write operation. When this bit is reset, the Receiver Buffer Register, the Transmitter Buffer Register, or the Interrupt Control Register can be accessed.
- Bit 6: **SSE.** A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only SOUT is affected by this bit; the transmitter is not affected.
- Bit 5: **PBF E.** When PBE and PBF E of UCR are both set to a logical 1,
(1) if EPE is a logical 1, the parity bit is fixed as a logical 0 to transmit and check.
(2) if EPE is a logical 0, the parity bit is fixed as a logical 1 to transmit and check.
- Bit 4: **EPE.** This bit describes the number of logic 1's in the data word bits and parity bit only when bit 3 is programmed. When this bit is set, an even number of logic 1's are sent or checked. When the bit is reset, an odd number of logic 1's are sent or checked.
- Bit 3: **PBE.** When this bit is set, the position between the last data bit and the stop bit of the SOUT will be stuffed with the parity bit at the transmitter. For the receiver, the parity bit in the same position as the transmitter will be detected.
- Bit 2: **MSBE.** This bit defines the number of stop bits in each serial character that is transmitted or received.
(1) If MSBE is set to a logical 0, one stop bit is sent and checked.
(2) If MSBE is set to a logical 1, and data length is 5 bits, one and a half stop bits are sent and checked.
(3) If MSBE is set to a logical 1, and data length is 6, 7, or 8 bits, two stop bits are sent and checked.
- Bits 0 and 1: **DLS0, DLS1.** These two bits define the number of data bits that are sent or checked in each serial character.

TABLE 3 - WORD LENGTH DEFINITION

| DLS1 | DLS0 | DATA LENGTH |
|------|------|-------------|
| 0 | 0 | 5 bits |
| 0 | 1 | 6 bits |
| 1 | 0 | 7 bits |
| 1 | 1 | 8 bits |

UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of the data transfer during communication.

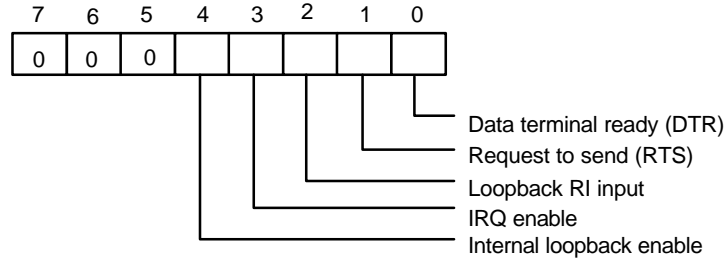


- Bit 7: RFEI. In 16450 mode, this bit is always set to a logic 0. In 16550 mode, this bit is set to a logic 1 when there is at least one parity bit error, no stop bit error or silent byte detected in the FIFO. In 16550 mode, this bit is cleared by reading from the USR if there are no remaining errors left in the FIFO.
- Bit 6: TSRE. In 16450 mode, when TBR and TSR are both empty, this bit will be set to a logical 1. In 16550 mode, if the transmit FIFO and TSR are both empty, it will be set to a logical 1. Other than these two cases, this bit will be reset to a logical 0.
- Bit 5: TBRE. In 16450 mode, when a data character is transferred from TBR to TSR, this bit will be set to a logical 1. If ETREI of ICR is a logical 1, an interrupt will be generated to notify the CPU to write the next data. In 16550 mode, this bit will be set to a logical 1 when the transmit FIFO is empty. It will be reset to a logical 0 when the CPU writes data into TBR or FIFO.
- Bit 4: SBD. This bit is set to a logical 1 to indicate that received data are kept in silent state for a full word time, including start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.
- Bit 3: NSER. This bit is set to a logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.
- Bit 2: PBER. This bit is set to a logical 1 to indicate that the parity bit of received data is wrong. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

- Bit 1: OER. This bit is set to a logical 1 to indicate received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition instead of FIFO full. When the CPU reads USR, it will clear this bit to a logical 0.
- Bit 0: RDR. This bit is set to a logical 1 to indicate received data are ready to be read by the CPU in the RBR or FIFO. After no data are left in the RBR or FIFO, the bit will be reset to a logical 0.

Handshake Control Register (HCR) (Read/Write)

This register controls the pins of the UART used for handshaking peripherals such as modem, and controls the diagnostic mode of the UART.



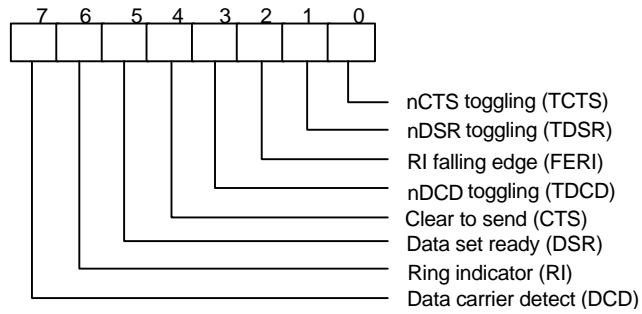
- Bit 4: When this bit is set to a logical 1, the UART enters diagnostic mode by an internal loopback, as follows:
 - (1) SOUT is forced to a logical 1, and SIN is isolated from the communication link instead of the TSR.
 - (2) Modem output pins are set to their inactive state.
 - (3) Modem input pins are isolated from the communication link and connect internally as DTR
- (bit 0 of HCR) → nDSR, RTS (bit 1 of HCR) → nCTS, Loopback RI input (bit 2 of HCR) → nRI and IRQ enable (bit 3 of HCR) → nDCD.

Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.

- Bit 3: The UART interrupt output is enabled by setting this bit to a logic 1. In the diagnostic mode this bit is internally connected to the modem control input nDCD.
- Bit 2: This bit is used only in the diagnostic mode. In the diagnostic mode this bit is internally connected to the modem control input nRI.
- Bit 1: This bit controls the nRTS output. The value of this bit is inverted and output to nRTS.
- Bit 0: This bit controls the nDTR output. The value of this bit is inverted and output to nDTR.

Handshake Status Register (HSR) (Read/Write)

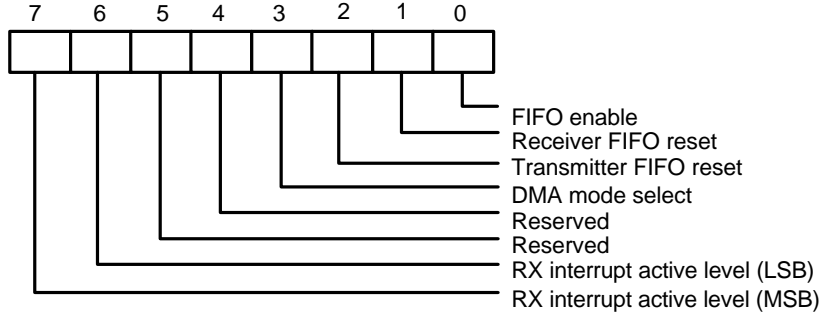
This register reflects the current state of four input pins for handshake peripherals such as a modem and records changes on these pins.



- Bit 7: This bit is the opposite of the nDCD input. This bit is equivalent to bit 3 of HCR in loopback mode.
- Bit 6: This bit is the opposite of the nRI input. This bit is equivalent to bit 2 of HCR in loopback mode.
- Bit 5: This bit is the opposite of the nDSR input. This bit is equivalent to bit 0 of HCR in loopback mode.
- Bit 4: This bit is the opposite of the nCTS input. This bit is equivalent to bit 1 of HCR in loopback mode.
- Bit 3: TDCD. This bit indicates that the nDCD pin has changed state after HSR was read by the CPU.
- Bit 2: FERI. This bit indicates that the nRI pin has changed from low to high state after HSR was read by the CPU.
- Bit 1: TDSR. This bit indicates that the nDSR pin has changed state after HSR was read by the CPU.
- Bit 0: TCTS. This bit indicates that the nCTS pin has changed state after HSR was read by the CPU.

UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.



Bit 6, 7: These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify the CPU to read the data from the FIFO.

TABLE 4 - FIFO TRIGGER LEVEL

| BIT 7 | BIT 6 | RX FIFO INTERRUPT ACTIVE LEVEL (BYTES) |
|-------|-------|--|
| 0 | 0 | 01 |
| 0 | 1 | 04 |
| 1 | 0 | 08 |
| 1 | 1 | 14 |

Bit 4, 5: Reserved

Bit 3: When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if UFR bit 0 = 1.

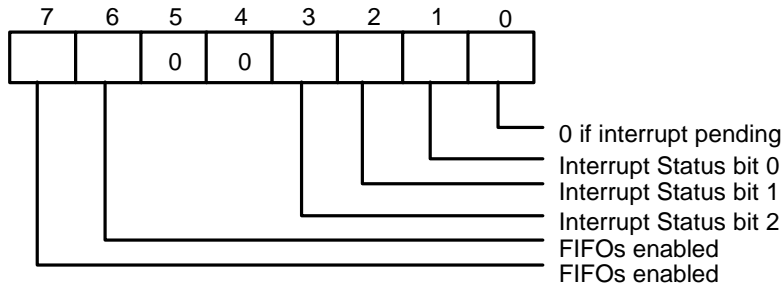
Bit 2: Setting this bit to a logical 1 resets the TX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 1: Setting this bit to a logical 1 resets the RX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 0: This bit enables the 16550 (FIFO) mode of the UART. This bit should be set to a logical 1 before other bits of UFR are programmed.

Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status, which is encoded by different interrupt sources into 3 bits.



Bit 7, 6: These two bits are set to a logical 1 when UFR bit 0 = 1.

Bit 5, 4: These two bits are always logic 0.

Bit 3: In 16450 mode, this bit is 0. In 16550 mode, both bit 3 and 2 are set to a logical 1 when a time-out interrupt is pending.

Bit 2, 1: These two bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to a logical 0.

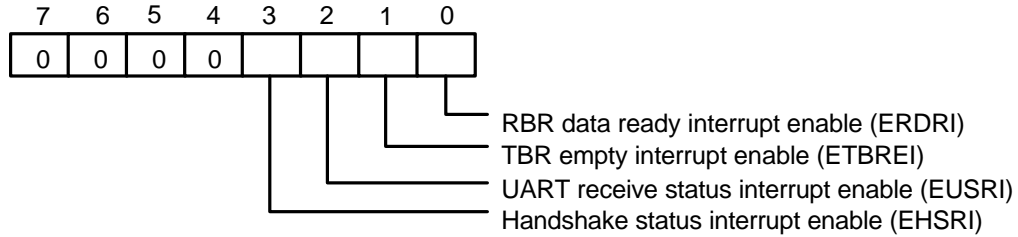
TABLE 5 - INTERRUPT CONTROL FUNCTION

| ISR | | | | INTERRUPT SET AND FUNCTION | | | |
|-------|-------|-------|-------|----------------------------|---------------------|---|---|
| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Interrupt Priority | Interrupt Type | Interrupt Source | Clear Interrupt |
| 0 | 0 | 0 | 1 | - | - | No Interrupt pending | - |
| 0 | 1 | 1 | 0 | First | UART Receive Status | 1. OER = 1 2. PBER = 1 3. NSER = 1 4. SBD = 1 | Read USR |
| 0 | 1 | 0 | 0 | Second | RBR Data Ready | 1. RBR data ready 2. FIFO interrupt active level reached | 1. Read RBR 2. Read RBR until FIFO data under active level |
| 1 | 1 | 0 | 0 | Second | FIFO Data Timeout | Data present in RX FIFO for 4 characters period of time since last access of RX FIFO. | Read RBR |
| 0 | 0 | 1 | 0 | Third | TBR Empty | TBR empty | 1. Write data into TBR 2. Read ISR (if priority is third) |
| 0 | 0 | 0 | 0 | Fourth | Handshake Status | 1. TCTS = 1 2. TDSR = 1 3. FER1 = 1 4. TDCD = 1 | Read HSR |

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

Interrupt Control Register (ICR) (Read/Write)

This 8-bit register allows the five types of controller interrupts to activate the interrupt output signal separately. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Control Register (ICR). A selected interrupt can be enabled by setting the appropriate bits of this register to a logical 1.



Bit 7-4: These four bits are always logic 0.

Bit 3: EHSRI. Setting this bit to a logical 1 enables the handshake status register interrupt.

Bit 2: EUSRI. Setting this bit to a logical 1 enables the UART status register interrupt.

Bit 1: ETBREI. Setting this bit to a logical 1 enables the TBR empty interrupt.

Bit 0: ERDRI. Setting this bit to a logical 1 enables the RBR data ready interrupt.

Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divides it by a divisor from 1 to $2^{16}-1$. The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (refer to CR0C bit7 and CR0C bit6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. In high-speed mode, the data transmission rate can be as high as 1.5M bps.

User-Defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

TABLE 6 - BAUD RATES
BAUD RATE USING 24 MHz TO GENERATE 1.8461 MHz

| Desired Baud Rate | Decimal divisor used to generate 16X clock | Percent error difference between desired and actual |
|-------------------|--|---|
| 50 | 2304 | ** |
| 75 | 1536 | ** |
| 110 | 1047 | 0.18% |
| 134.5 | 857 | 0.099% |
| 150 | 768 | ** |
| 300 | 384 | ** |
| 600 | 192 | ** |
| 1200 | 96 | ** |
| 1800 | 64 | ** |
| 2000 | 58 | 0.53% |
| 2400 | 48 | ** |
| 3600 | 32 | ** |
| 4800 | 24 | ** |
| 7200 | 16 | ** |
| 9600 | 12 | ** |
| 19200 | 6 | ** |
| 38400 | 3 | ** |
| 57600 | 2 | ** |
| 115200 | 1 | ** |
| 230400 | 104* | ** |
| 460800 | 52* | ** |
| 921600 | 26* | ** |
| 1.5M | 1* | 0% |

* Only use in high speed mode (refer to CR0C bit 7 and CR0C bit 6).

** The percentage error for all baud rates, except where indicated otherwise, is 0.16%.

PARALLEL PORT

Printer Interface Logic

The parallel port of the FDC87W22 makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL level. The FDC87W22 supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port

(ECP), Extension FDD mode (EXTFDD), and Extension 2FDD mode (EXT2FDD) on the parallel port. Refer to the configuration registers for more information on disabling, power-down, and on selecting the mode of operation.

Table 7A shows the pin definitions for different modes of the parallel port.

TABLE 7A - Parallel Port Connector and Pin Definition for SPP/EPP/ECP Modes

| HOST CONNECTOR | PIN NUMBER OF FDC87W22 | PIN ATTRIBUTE | SPP | EPP | ECP |
|----------------|------------------------|---------------|---------|---------|---|
| 1 | 19 | O | nSTB | nWrite | nSTB |
| 2-9 | 9-14,16-17 | I/O | PD<0:7> | PD<0:7> | PD<0:7> |
| 10 | 26 | I | nACK | Intr | nACK |
| 11 | 24 | I | BUSY | nWait | BUSY, PeriphAck ² |
| 12 | 27 | I | PE | PE | PEError, nAckReverse ² |
| 13 | 28 | I | SLCT | Select | SLCT |
| 14 | 20 | O | nAFD | nDStrb | nAFD, HostAck ² |
| 15 | 29 | I | nERR | nError | nFault ¹ , nPeriphRequest ² |
| 16 | 21 | O | nINIT | nIntr | nINIT ¹ , nReverseRqst ² |
| 17 | 22 | O | nSLIN | nAStlb | nSLIN ^{1,2} |

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, refer to the IEEE 1284 standard.

TABLE 7B - Parallel Port Connector and Pin Definition for EXT2FDD and EXT-FDD Modes

| Host Connector | Pin Number FDC87W22 | Pin Attribute | SPP | Pin Attribute | EXT2FDD | Pin Attribute | EXT-FDD |
|----------------|---------------------|---------------|-------|---------------|----------|---------------|----------|
| 1 | 19 | O | nSTB | --- | --- | --- | --- |
| 2 | 9 | I/O | PD0 | I | nINDEX2 | I | nINDEX2 |
| 3 | 10 | I/O | PD1 | I | nTRAK02 | I | nTRAK02 |
| 4 | 11 | I/O | PD2 | I | nWP2 | I | nWP2 |
| 5 | 12 | I/O | PD3 | I | nRDATA2 | I | nRDATA2 |
| 6 | 13 | I/O | PD4 | I | nDSKCHG2 | I | nDSKCHG2 |
| 7 | 14 | I/O | PD5 | --- | --- | --- | --- |
| 8 | 15 | I/O | PD6 | OD | nMOA2 | --- | --- |
| 9 | 16 | I/O | PD7 | OD | nDSA2 | --- | --- |
| 10 | 26 | I | nACK | OD | nDSB2 | OD | nDSB2 |
| 11 | 24 | I | BUSY | OD | nMOB2 | OD | nMOB2 |
| 12 | 27 | I | PE | OD | nWD2 | OD | nWD2 |
| 13 | 28 | I | SLCT | OD | nWE2 | OD | nWE2 |
| 14 | 20 | O | nAFD | OD | nRWC2 | OD | nRWC2 |
| 15 | 29 | I | nERR | OD | nNERR2 | OD | nNERR2 |
| 16 | 21 | O | nINIT | OD | nDIR2 | OD | nDIR2 |
| 17 | 22 | O | nSLIN | OD | nSTEP2 | OD | nSTEP2 |

| HOST CONNECTOR | PIN NUMBER FDC87W22 | PIN ATTRI-BUTE | SPP | PIN ATTRI-BUTE | EXTADP MODE | PIN ATTRI-BUTE | JOYSTICK MODE |
|----------------|---------------------|----------------|-------|----------------|-------------|----------------|---------------|
| 1 | 19 | O | nSTB | O | nXWR | O | VDD |
| 2 | 9 | I/O | PD0 | I/O | XD0 | I | JP0 |
| 3 | 10 | I/O | PD1 | I/O | XD1 | I | JP1 |
| 4 | 11 | I/O | PD2 | I/O | XD2 | I | --- |
| 5 | 12 | I/O | PD3 | I/O | XD3 | I | --- |
| 6 | 13 | I/O | PD4 | I/O | XD4 | I | JB0 |
| 7 | 14 | I/O | PD5 | I/O | XD5 | I | JB1 |
| 8 | 15 | I/O | PD6 | I/O | XD6 | I | --- |
| 9 | 16 | I/O | PD7 | I/O | XD7 | I | --- |
| 10 | 26 | I | nACK | I | XDRQ | I | --- |
| 11 | 24 | I | BUSY | I | XIRQ | I | --- |
| 12 | 27 | I | PE | O | XA0 | I | --- |
| 13 | 28 | I | SLCT | O | XA1 | I | --- |
| 14 | 20 | O | nAFD | O | nXRD | O | VDD |
| 15 | 29 | I | nERR | O | XA2 | I | --- |
| 16 | 21 | O | nINIT | O | nXDACK | O | VDD |
| 17 | 22 | O | nSLIN | O | TC | O | VDD |

Enhanced Parallel Port (EPP)

TABLE 8 - PRINTER MODE AND EPP REGISTER ADDRESS

| A2 | A1 | A0 | REGISTER | NOTE |
|----|----|----|--------------------------------|------|
| 0 | 0 | 0 | Data port (R/W) | 1 |
| 0 | 0 | 1 | Printer status buffer (Read) | 1 |
| 0 | 1 | 0 | Printer control latch (Write) | 1 |
| 0 | 1 | 0 | Printer control swapper (Read) | 1 |
| 0 | 1 | 1 | EPP address port (R/W) | 2 |
| 1 | 0 | 0 | EPP data port 0 (R/W) | 2 |
| 1 | 0 | 1 | EPP data port 1 (R/W) | 2 |
| 1 | 1 | 0 | EPP data port 2 (R/W) | 2 |
| 1 | 1 | 1 | EPP data port 2 (R/W) | 2 |

Notes:

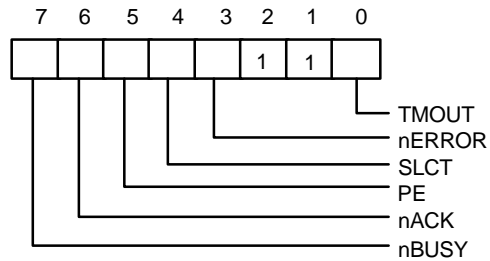
1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Data Swapper

The system microprocessor can read the contents of the printer's data latch by reading the data swapper.

Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the printer status buffer. The bit definitions are as follows:

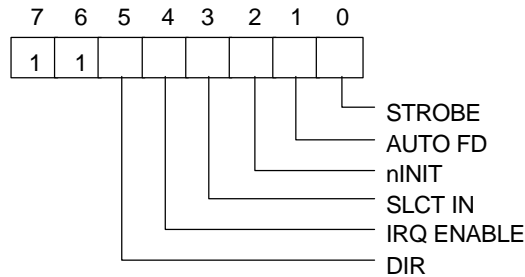


Bit 7: This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.

- Bit 6: This bit represents the current state of the printer's nACK signal. A 0 means the printer has received a character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before nBUSY stops.
- Bit 5: A 1 means the printer has detected the end of paper.
- Bit 4: A 1 means the printer is selected.
- Bit 3: A 0 means the printer has encountered an error condition.
- Bit 1, 2: These two bits are not implemented and are logic one during a read of the status register.
- Bit 0: This bit is valid in EPP mode only. It indicates that a 10 μ S time-out has occurred on the EPP bus. A logic 0 means that no time-out error has occurred; a logic 1 means that a time-out error has been detected. Writing a logic 1 to this bit will clear the time-out status bit; writing a logic 0 has no effect.

Printer Control Latch and Printer Control Swapper

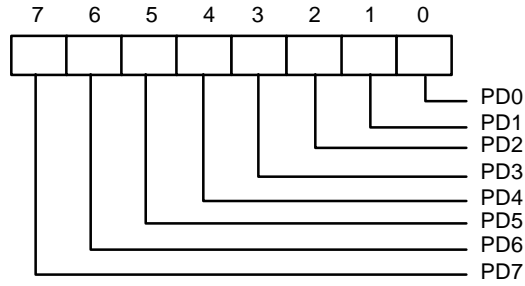
The system microprocessor can read the contents of the printer control latch by reading the printer control swapper. Bit definitions are as follows:



- Bit 7,6: These two bits are a logic one during a read. They can be written.
- Bit 5: Direction control bit
When this bit is a logic 1, the parallel port is in input mode (read); when it is a logic 0, the parallel port is in output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.
- Bit 4: A 1 in this position allows an interrupt to occur when nACK changes from low to high.
- Bit 3: A 1 in this bit position selects the printer.
- Bit 2: A 0 starts the printer (50 microsecond pulse, minimum).
- Bit 1: A 1 causes the printer to line-feed after a line is printed.
- Bit 0: A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

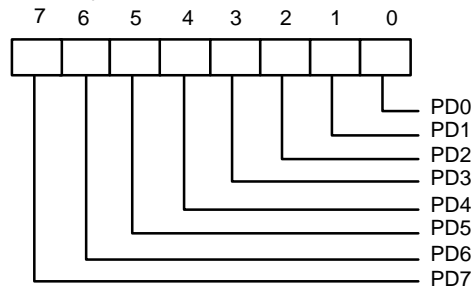


The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of \overline{nIOW} causes an EPP address write cycle to be performed, and the trailing edge of \overline{nIOW} latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of \overline{nIOR} causes an EPP address read cycle to be performed and the data to be output to the host CPU.

EPP Data Port 0-3

These four registers are available only in EPP mode. Bit definitions of each data port are as follows:



When accesses are made to any EPP data port, the contents of DB0-DB7 are buffered (non-inverting) and output to the ports PD0-PD7 during a write operation. The leading edge of \overline{nIOW} causes an EPP data write cycle to be performed, and the trailing edge of \overline{nIOW} latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of \overline{nIOR} causes an EPP read cycle to be performed and the data to be output to the host CPU.

Bit Map of Parallel Port and EPP Registers

| REGISTER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Data Port (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Status Buffer (Read) | nBUSY | nACK | PE | SLCT | nERROR | 1 | 1 | TMOUT |
| Control Swapper (Read) | 1 | 1 | 1 | IRQEN | SLIN | nINIT | nAUTOFD | nSTROBE |
| Control Latch (Write) | 1 | 1 | DIR | IRQ | SLIN | nINIT | nAUTOFD | nSTROBE |
| EPP Address Port (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 0 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 1 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 2 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 3 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |

EPP Pin Descriptions

| EPP NAME | TYPE | EPP DESCRIPTION |
|-----------------|-------------|---|
| nWrite | O | Denotes an address or data read or write operation. |
| PD<0:7> | I/O | Bi-directional EPP address and data bus. |
| Intr | I | Used by peripheral device to interrupt the host. |
| nWait | I | Inactive to acknowledge that data transfer is completed. Active to indicate that the device is ready for the next transfer. |
| PE | I | Paper end; same as SPP mode. |
| Select | I | Printer selected status; same as SPP mode. |
| nDStrb | O | This signal is active low. It denotes a data read or write operation. |
| nError | I | Error; same as SPP mode. |
| nInits | O | This signal is active low. When it is active, the EPP device is reset to its initial operating mode. |
| nAStrb | O | This signal is active low. It denotes an address read or write operation. |

EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. The PDx bus is in the standard or bi-directional mode when no EPP read, write, or address cycle is currently being executed. In this condition all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μ S have elapsed from the start of the EPP cycle to the time nWAIT is de-asserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in Status bit 0.

EPP Operation

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed synchronously.

EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

- a. If the nWait is active low, when the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, the read/write cycle proceeds normally and will be completed when nWait goes inactive high.

- b. If nWait is inactive high, the read/write cycle will not start. It must wait until nWait changes to active low, at which time it will start as described above.

EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it will not terminate until nWait changes from active low to inactive high.

Extended Capabilities Parallel (ECP) Port

This port is software and hardware compatible with existing parallel ports, so it may be used as a standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host to peripheral) and reverse (peripheral to host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port supports run-length-encoded (RLE) decompression (required) in the hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. The hardware support for compression is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

ECP Register and Mode Definitions

| NAME | ADDRESS | I/O | ECP MODES | FUNCTION |
|----------|-----------|-----|-----------|---------------------------|
| data | Base+000h | R/W | 000-001 | Data Register |
| ecpAFifo | Base+000h | R/W | 011 | ECP FIFO (Address) |
| dsr | Base+001h | R | All | Status Register |
| dcr | Base+002h | R/W | All | Control Register |
| cFifo | Base+400h | R/W | 010 | Parallel Port Data FIFO |
| ecpDFifo | Base+400h | R/W | 011 | ECP FIFO (DATA) |
| tFifo | Base+400h | R/W | 110 | Test FIFO |
| cnfgA | Base+400h | R | 111 | Configuration Register A |
| cnfgB | Base+401h | R/W | 111 | Configuration Register B |
| ecr | Base+402h | R/W | All | Extended Control Register |

Note: The base addresses are specified by CR23, which are determined by configuration register or hardware setting.

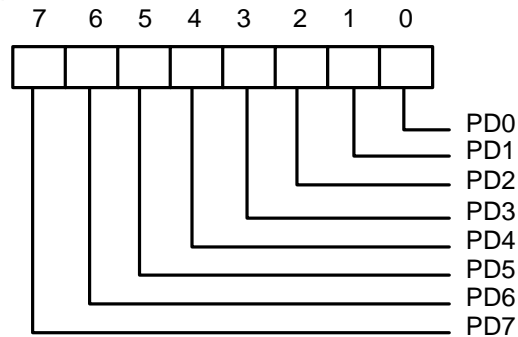
| MODE | DESCRIPTION |
|------|--|
| 000 | SPP mode |
| 001 | PS/2 Parallel Port mode |
| 010 | Parallel Port Data FIFO mode |
| 011 | ECP Parallel Port mode |
| 100 | EPP mode (If this option is enabled in the CR9 and CR0 to select ECP/EPP mode) |
| 101 | Reserved |
| 110 | Test mode |
| 111 | Configuration mode |

Note: The mode selection bits are bit 7-5 of the Extended Control Register.

Data and ecpAFifo Port

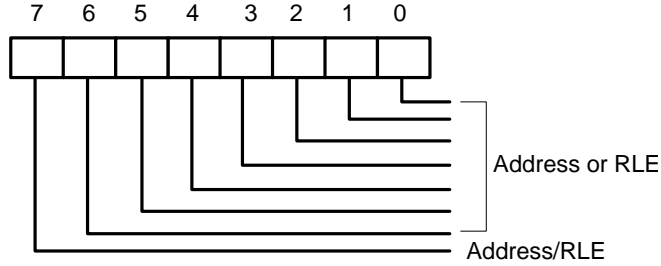
Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input. The contents of this register are output to the PD0-PD7 ports. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:



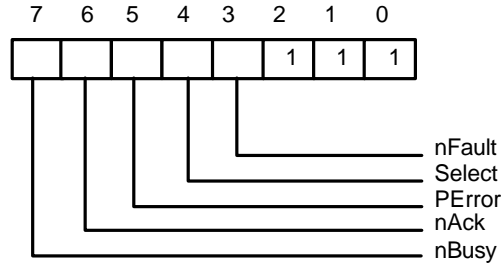
Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is defined only for the forward direction. The bit definitions are as follows:



Device Status Register (DSR)

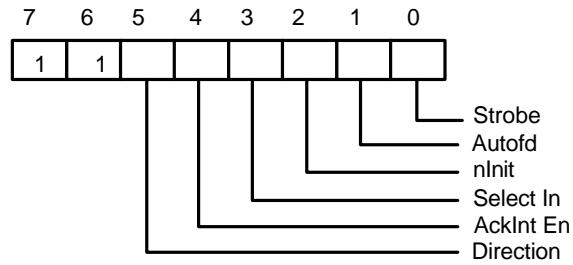
These bits are at low level during a read of the Printer Status Register. The bits of this status register are defined as follows:



- Bit 7: This bit reflects the complement of the Busy input.
- Bit 6: This bit reflects the nAck input.
- Bit 5: This bit reflects the PError input.
- Bit 4: This bit reflects the Select input.
- Bit 3: This bit reflects the nFault input.
- Bit 2-0: These three bits are not implemented and are always logic one during a read.

Device Control Register (DCR)

The bit definitions are as follows:



Bit 6,7: These two bits are logic one during a read and cannot be written.

Bit 5: This bit has no effect and the direction is always out if mode = 000 or mode = 010. Direction is valid in all other modes.

0 The parallel port is in output mode.

1 The parallel port is in input mode.

Bit 4: Interrupt request enable. When this bit is set to a high level, it may be used to enable interrupt requests from the parallel port to the CPU due to a low to high transition on the nACK input.

Bit 3: This bit is inverted and output to the nSLIN output.

0 The printer is not selected.

1 The printer is selected.

Bit 2: This bit is output to the nINIT output.

Bit 1: This bit is inverted and output to the nAFD output.

Bit 0: This bit is inverted and output to the nSTB output.

cFifo (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. The standard parallel port protocol is used by a hardware handshake to the peripheral to transmit bytes written or DMAed from the system to this FIFO. Transfers to the FIFO are byte aligned.

ecpDFifo (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

When the direction bit is 1, data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

tFifo (Test FIFO Mode) Mode = 110

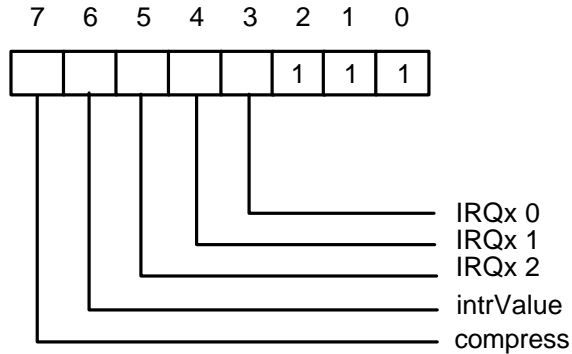
Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

cnfgA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

cnfgB (Configuration Register B) Mode = 111

The bit definitions are as follows:



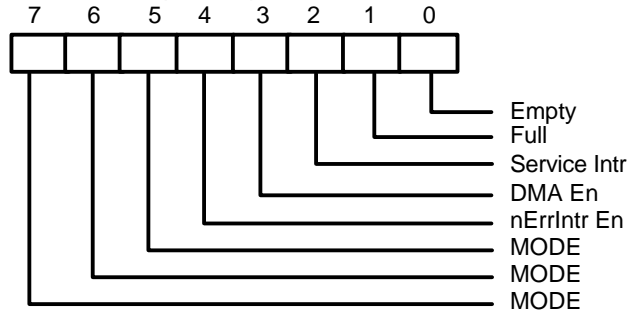
- Bit 7: This bit is read-only. It is at low level during a read. This means that this chip does not support hardware RLE compression.
- Bit 6: Returns the value on the ISA IRQ line to determine possible conflicts.
- Bit 5-3: Reflect the IRQ resource assigned for ECP port.

| cnfgB[5:3] | IRQ resource |
|------------|--|
| 000 | Reflect other IRQ resources selected by PnP register (default) |
| 001 | IRQ7 |
| 010 | IRQ9 |
| 011 | IRQ10 |
| 100 | IRQ11 |
| 101 | IRQ14 |
| 110 | IRQ15 |
| 111 | IRQ5 |

Bit 2-0: These five bits are at high level during a read and can be written.

ecr (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:



Bit 7-5: These bits are read/write and select the mode.

- 000 Standard Parallel Port mode. The FIFO is reset in this mode.
- 001 PS/2 Parallel Port mode. This is the same as 000 except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register.
- 010 Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
- 011 ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. When the direction is 1 (reverse direction) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
- 100 Selects EPP Mode. In this mode, EPP is active if the EPP supported option is selected.
- 101 Reserved.
- 110 Test Mode. The FIFO may be written and read in this mode, but the data will not be transmitted on the parallel port.
- 111 Configuration Mode. The configA and configB registers are accessible at 0x400 and 0x401 in this mode.

Bit 4: Read/Write (Valid only in ECP Mode)

- 1 Disables the interrupt generated on the asserting edge of nFault.
- 0 Enables an interrupt pulse on the high to low edge of nFault. If nFault is asserted (interrupt) an interrupt will be generated and this bit is written from a 1 to 0.

Bit 3: Read/Write

- 1 Enables DMA.
- 0 Disables DMA unconditionally.

Bit 2: Read/Write

- 1 Disables DMA and all of the service interrupts.
- 0 Enables one of the following cases of interrupts. When one of the service interrupts has occurred, the serviceIntr bit is set to a 1 by hardware. This bit must be reset to 0 to re-enable the interrupts. Writing a 1 to this bit will not cause an interrupt.
 - (a) dmaEn = 1:
During DMA this bit is set to a 1 when terminal count is reached.
 - (b) dmaEn = 0 direction = 0:
This bit is set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO.
 - (c) dmaEn = 0 direction = 1:
This bit is set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

Bit 1: Read only

- 0 The FIFO has at least 1 free byte.
- 1 The FIFO cannot accept another byte or the FIFO is completely full.

Bit 0: Read only

- 0 The FIFO contains at least 1 byte of data.
- 1 The FIFO is completely empty.

Bit Map of ECP Port Registers

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | NOTE |
|----------|-------------------------|----------------------|-----------|------------|----------|-------------|--------|--------|------|
| data | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 | |
| ecpAFifo | Addr/RLE | Address or RLE field | | | | | | | 2 |
| dsr | nBusy | nAck | PError | Select | nFault | 1 | 1 | 1 | 1 |
| dcr | 1 | 1 | Direction | ackIntEn | SelectIn | nInit | autofd | strobe | 1 |
| cFifo | Parallel Port Data FIFO | | | | | | | | 2 |
| ecpDFifo | ECP Data FIFO | | | | | | | | 2 |
| tFifo | Test FIFO | | | | | | | | 2 |
| cnfgA | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| cnfgB | compress | intrValue | 1 | 1 | 1 | 1 | 1 | 1 | |
| ecr | MODE | | | nErrIntrEn | dmaEn | serviceIntr | full | empty | |

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

ECP Pin Descriptions

| NAME | TYPE | DESCRIPTION |
|-------------------------|------|--|
| nStrobe (HostClk) | O | The nStrobe registers data or address into the slave on the asserting edge during write operations. This signal handshakes with Busy. |
| PD<7:0> | I/O | These signals contains address or data or RLE data. |
| nAck (PeriphClk) | I | This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutofd in reverse. |
| Busy (PeriphAck) | I | This signal desserts to indicate that the peripheral can accept data. It indicates whether the data lines contain ECP command information or data in the reverse direction. When in reverse direction, normal data are transferred when Busy (PeriphAck) is high and an 8-bit command is transferred when it is low. |
| PError (nAckReverse) | I | This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus. |
| Select (Xflag) | I | Indicates printer on line. |
| nAutoFd (HostAck) | O | Requests a byte of data from the peripheral when it is asserted. This signal indicates whether the data lines contain ECP address or data in the forward direction. When in forward direction, normal data are transferred when nAutoFd (HostAck) is high and an 8-bit command is transferred when it is low. |
| nFault (nPeriphRequest) | I | Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP Mode. |
| nInit (nReverseRequest) | O | This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. |
| nSelectIn (ECPMode) | O | This signal is always deasserted in ECP mode. |

ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits. The following are required:

- Set direction = 0, enabling the drivers.
- Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
- Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
- Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

Mode Switching

Software will execute P1284 negotiation and all operations prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can be changed only in mode 001.

When in extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001.

Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

Data Compression

The FDC87W22 supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Note that the odd (RLE) compression in hardware is not supported. In order to transfer data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

FIFO Operation

The FIFO threshold is set in configuration register 5. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. The DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO

using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and `serviceIntr` is asserted, which will disable the DMA.

Programmed I/O (NON-DMA) Mode

The ECP or parallel port FIFOs can also be operated using interrupt driven programmed I/O. Programmed I/O transfers are to the `ecpDFifo` at 400H and `ecpAFifo` at 000H or from the `ecpDFifo` located at 400H, or to/from the `tFifo` at 400H. The host must set the direction, state, `dmaEn = 0` and `serviceIntr = 0` in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Extension FDD Mode (EXTFDD)

In this mode, the FDC87W22 changes the printer interface pins to FDC input/output pins, allowing the user to install a second floppy disk drive (FDD B) through the DB-25 printer connector. The pin assignments for the FDC input/output pins are shown in Table 7A.

After the printer interface is set to EXTFDD mode, the following occur:

1. Pins `nMOB` and `nDSB` will be forced to inactive state.
2. Pins, `nDSKCHG`, `nRDATA`, `nWP`, `nTRAK0`, `nINDEX` will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

3. Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.
4. If the parallel port is set to EXTFDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

Extension 2FDD Mode (EXT2FDD)

In this mode, the FDC87W22 changes the printer interface pins to FDC input/output pins, allowing the user to install two external floppy disk drives through the DB-25 printer connector to replace internal floppy disk drives A and B. The pin assignments for the FDC input/output pins are shown in Table 7A.

After the printer interface is set to EXTFDD mode, the following occur:

1. Pins `nMOA`, `nDSA`, `nMOB`, and `nDSB` will be forced to inactive state.
2. Pins `nDSKCHG`, `nRDATA`, `nWP`, `nTRAK0`, and `nINDEX` will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.
3. Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.
4. If the parallel port is set to EXT2FDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

Extension Adapter Mode (EXTADP) (Patent Pending)

In this mode, the FDC87W22 redefines the printer interface pins for use as an extension adapter, allowing a pocket peripheral adapter card to be installed through the DB-25 printer connector. The pin assignments for the extension adapter are shown in table 7A.

- XDO-XD7 are the system data bus for the extension adapter.
- XA0-XA2 are the system address bus.
- nXWR and nXRD are the I/O read/write commands with address comparing match or in DMA access mode.
- nXDACK, XTC, and XDRQ are used in conjunction with nPDACKX, TC, and PDRQX to execute a DMA cycle.

The extension adapter can issue a DMA request by setting pin XDRQ high, thus sending the FDC87W22 output to the host system by pin PDRQX. The DMA controller should recognize the DMA request and output a relative DACK to pin nPDACKX of the FDC87W22, which will output the DACK without any change from pin nXDACK to the extension adapter. Once the DMA transfer is completed, a terminal count (TC) should be issued from the DMA controller to pin TC of FDC87W22 and output to the extension adapter via pin XTC. XIRQ is the interrupt request of the extension adapter. The value of XIRQ coming from the extension adapter will directly pass through pin IRQ7 to the host system.

XIRQ and IRQ7, nXDACK and nPDACKX, and XDRQ and PDRQX are three input/output pairs of FDC87W22 pins. Although these pins are defined as DMA and interrupt functions, they can be redefined by users for other specific functions.

Operation

The idea behind EXTADP mode is to treat the parallel port DB-25 connector as an ISA slot, except that its addresses are not issued to the extension adapter. The operation of EXTADP mode is described below:

1. Set the FDC87W22 to EXTADP mode by programming bit 7 of CR7 as low and bit 3 and bit 2 of CR0 as high and low, respectively.
2. The FDC87W22 CR2 is an address register that records the address of the extension adapter. When the desired address is written into CR2, pins nXWR and nXRD of the FDC87W22 will simultaneously go low and the desired address will also appear on the printer data bus PD7-PD0. Users can logically OR these two signals as an initial reset.
3. After the above two steps, every time the host system issues an IOR or IOW command, the FDC87W22 will compare the I/O address with the CR2 register. If the comparison matches, the data, low bits addresses (XA2-XA0), and nXWR/nXRD will be presented on the parallel port DB-25 connector.
4. DMA operations are handled in the same way as item 3, except that the relevant nPDACKX, PDRQX will be active on the DB-25 connector.

Joystick Mode (Patent pending)

The joystick mode allows users to plug a joystick into the parallel port DB-25 connector. The pin definitions are shown in Table 7A.

- Pins nNSTB, nAFD, nNSLIN, and nINIT output high as a voltage supply to the joystick.
- Pins PD5 and PD4 are the button input of the joystick.
- Pins PD1 and PD0 are the X/Y axis paddle input of the joystick.

- There are two one-shot timers (556) inside the FDC87W22 for use with the joystick.

Game Port Decoder

The FDC87W22 provides nGMRD and nGMWR pins that decode game port address as specified in CR1E and I/O read/write commands.

If the host issues nIOR and the specified address, the nGMRD pin is low active; if it issues nIOW and the specified address, the nGMWR pin is low active.

Plug and Play Configuration

A powerful new plug-and-play function has been built into the FDC87W22 to help simplify the task of setting up a computer environment. With appropriate support from BIOS manufacturers, the system designer can freely allocate Winbond I/O devices (i.e., the FDC, PRT, UART, IDE, and game port) in the PC's I/O space (100H - 3FFH). In addition, the FDC87W22 also provides 8 interrupt requests and 3 DMA pairs for designers to assign in interfacing FDCs, UARTs, and PRTs.

Hence this powerful I/O chip offers greater flexibility for system designers.

The PnP feature is implemented through a set of Extended Function Registers (CR1E and CR20 to 29). Details on configuring these registers are given in Section 8. The default values of these PnP-related registers set the system to a configuration compatible with environments designed with previous Winbond I/O chips.

Extended Function Registers

The FDC87W22 provides many configuration registers for setting up different types of configurations. After power-on reset, the state of the hardware setting of each pin will be latched by the relevant configuration register to allow the FDC87W22 to enter the proper operating configuration. To protect the chip from invalid reads or writes, the configuration registers cannot be accessed by the user.

There are four ways to enable the configuration registers to be read or written. HEFRAS (CR0C bit 5) and HEFERE (CR16 bit 0) can be used to select one out of these four methods of entering the Extended Function mode as follows:

| HEFRAS | HEFERE | Address and Value |
|--------|--------|---|
| 0 | 0 | write 88H to the location 250H |
| 0 | 1 | write 89H to the location 250H (power-on default) |
| 1 | 0 | write 86H to the location 3F0H twice |
| 1 | 1 | write 87H to the location 3F0H twice |

First, a specific value must be written once (88H/89H) or twice (86H/87H) to the Extended Functions Enable Register (I/O port address 250H or 3F0H). Second, an index value (00H-17H, 1EH, 20H-29H) must be written to the Extended Functions Index Register (I/O port address 251H or 3F0H) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 252H or 3F1H).

After programming of the configuration register is finished, an additional value should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. In the case of EFER at 250H, this additional value can be any value other than 88H if HEFERE = 0 and 89H if HEFERE = 1. While EFER is at 3F0H, this additional value must be AAH. The designer can also set bit 6 of CR9 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

Extended Functions Enable Registers (EFERs)

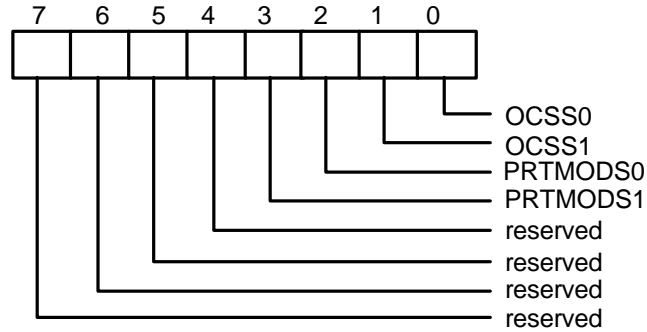
After a power-on reset, the FDC87W22 enters the default operating mode. Before the FDC87W22 enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 250H or 3F0H (as described in the above section).

Extended Function Index Registers (EFIRs), Extended Function Data Registers (EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (0H, 1H, 2H, ..., or 29H) to access Configuration Register 0 (CR0), Configuration Register 1 (CR1), Configuration Register 2 (CR2), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 251H or 3F0H (as described in section 8.0) on PC/AT systems; the EFDRs are read/write registers with port address 252H or 3F1H (as described in section 8.0) on PC/AT systems. The function of each configuration register is described below.

Configuration Register 0 (CR0), default = 00H

When the device is in Extended Function mode and EFIR is 0H, the CR0 register can be accessed through EFDR. The bit definitions for CR0 are as follows:



Bit 7-Bit 4: Reserved.

PRTMOD1 PRTMOD0 (Bit 3, Bit 2):

These two bits and PRTMOD2 (CR9 bit7) determine the parallel port mode of the FDC87W22.

| PRTMODS2 (BIT 7 OF CR9) | PRTMOD1 (BIT 3 OF CR0) | PRTMODS0 (BIT 2 OF CR0) | |
|------------------------------------|-----------------------------------|------------------------------------|----------|
| 0 | 0 | 1 | EXTFDC |
| 0 | 1 | 0 | EXTADP |
| 0 | 1 | 1 | EXT2FDD |
| 1 | 0 | 0 | JOYSTICK |
| 1 | 0 | 1 | EPP/SPP |
| 1 | 1 | 0 | ECP |
| 1 | 1 | 1 | ECP/EPP |

- 01 Extension FDD Mode (EXTFDD), PRTMOD2 = 0
- 10 Extension Adapter Mode (EXTADP), PRTMOD2 = 0
- 11 Extension 2FDD Mode (EXT2FDD), PRTMOD2 = 0
- 00 JOYSTICK Mode, PRTMOD2 = 1
- 01 EPP Mode and SPP Mode, PRTMOD2 = 1
- 10 ECP Mode, PRTMOD2 = 1
- 11 ECP Mode and EPP Mode, PRTMOD2 = 1

OSCS1, OSCS0 (Bit 1, Bit 0):

These two bits and OSCS2 (CR6 bit 6) are used to select one of the FDC87W22's power-down functions. These bits may be programmed in four different ways:

- 00 Default power-on state after power-on reset (OSCS2 = 0).
- 00 OSC on, 24 MHz clock is stopped internally (OSCS2 = 1). Clock can be restarted by clearing OSCS2.
- 01 Immediate power-down (IPD) state, OSCS2 = 0

When bit 0 is 1 and bit 1 is set to 0, the FDC87W22 will stop its oscillator and enter power-down mode immediately. The FDC87W22 will not leave the power-down mode until either a system power-on reset from the MR pin or these two bits are used to program the chip back to power-on state. After leaving the power-down mode, the FDC87W22 must wait 128 mS for the oscillator to stabilize.

- 10 Standby for automatic power-down (APD), OSCS2 = 0

When bit 1 is set to 1 and bit 0 is set to 0, the FDC87W22 will stand by for automatic power-down. A power-down will occur when the following conditions obtain:

- FDC not busy
- FDD motor off
- Interrupt source of line status, modem status, and data ready is inactive (neglecting IER enable/disable)
- Master Reset inactive
- SOUTA and SOUTB in idle state
- SINA and SINB in idle state
- No register read or write to chip

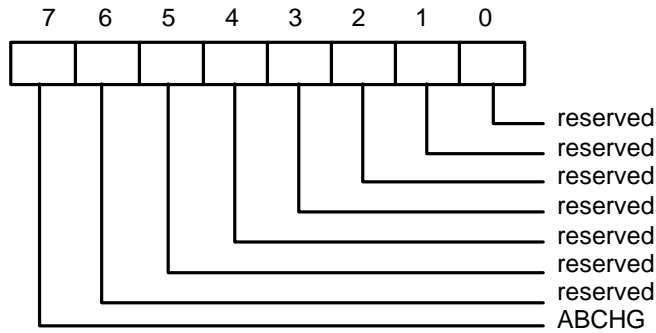
If all of these conditions are met, a counter begins to count down. While the timer is counting down, the FDC87W22 remains in normal operating mode, and if any of the above conditions changes, the counter will be reset. If the set time (set by bit 7 and bit 6 of CR8) elapses without a change in any of the above conditions, bits 1 and 0 will be set to (1, 1) and the chip will enter automatic power-down mode. The oscillator of the FDC87W22 will remain running, but the internal clock will be disabled to save power. Once the above conditions are no longer met, the internal clock will be resupplied and the chip will return to normal operation.

- 11 Automatic power-down (ADP) state, OSCS2 = 0

The FDC87W22 enters this state automatically after the counter described above has counted down. If there is a change in any of the conditions listed above, the FDC87W22 's clock will be restarted and bits 1 and 0 will be set to (1, 0), i.e., standby for automatic power-down. When the clock is restarted, the chip is ready for normal operation, with no need to wait for the oscillator to stabilize.

Configuration Register 1 (CR1), default = 00H

When the device is in Extended Function mode and EFIR is 01H, the CR1 register can be accessed through EFDR. The bit definitions are as follows:



Bit 0-bit 6: Reserved.

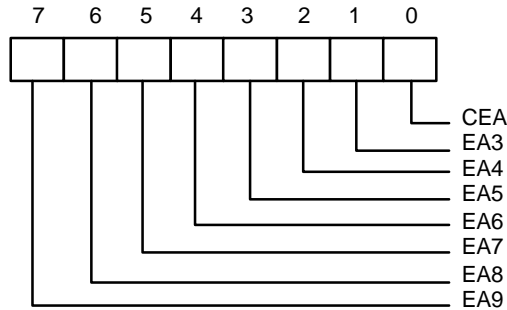
ABCHG (Bit 7):

This bit enables the FDC AB Change Mode. Default to be enabled at power-on reset.

- 0 Drives A and B assigned as usual
- 1 Drive A and drive B assignments exchanged

Configuration Register 2 (CR2), default = 00H

When the device is in Extended Function mode and EFIR is 02H, the CR2 register can be accessed through EFDR. The bit definitions are as follows:

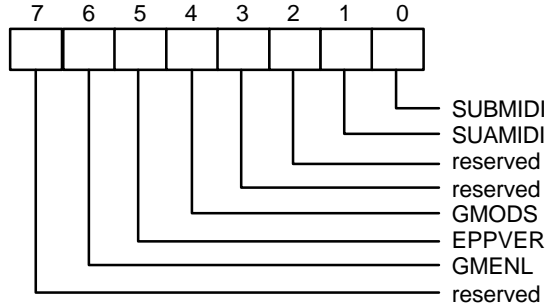


When the FDC87W22 is programmed into extension adapter mode, the contents of this register are a base address for the extension adapter. When base addresses EA3-EA9 are written into CR2, both the nXRD and nXWR pins will be active low simultaneously and an adapter connected to the parallel port can latch the same base address through pins XD1-XD7. After the base address is latched into CR2, a subsequent read/write cycle to this same base address will generate an nXRD or nXWR signal.

If CEA is set to 0, then the FDC87W22 will compare system addresses SA9-SA3 with EA9-EA3 to generate a compare-equal signal for this read/write command to access the Extension adapter. If CEA is set to 1, then only EA9-EA4 are used in this comparison.

Configuration Register 3 (CR3), default = 30H

When the device is in Extended Function mode and EFIR is 03H, the CR3 register can be accessed through EFDR. The bit definitions are as follows:



SUBMIDI (Bit 0):

This bit selects the clock divide rate of UARTB.

- 0 Disables MIDI support, UARTB clock = 24 MHz divided by 13 (default)
- 1 Enables MIDI support, UARTB clock = 24 MHz divided by 12

SUAMIDI (Bit 1):

This bit selects the clock divide rate of UARTA.

- 0 Disables MIDI support, UARTA clock = 24 MHz divided by 13 (default)
- 1 Enables MIDI support, UARTA clock = 24 MHz divided by 12

Bit 2-bit 3: Reserved.

GMODS (Bit 4):

This bit selects the adapter mode or portable mode.

- 0 Selects the portable mode. Pins 41 and 39 will function as PFDCEN and PEXTEN
- 1 Selects the adapter mode. Pins 41 and 39 will function as nGMRD and nGMWR

Note: GMDRQ (CR16 bit 3) has higher precedence over this bit. That is, GMODS selection is only valid when GMGRQ = 0.

EPPVER (Bit 5):

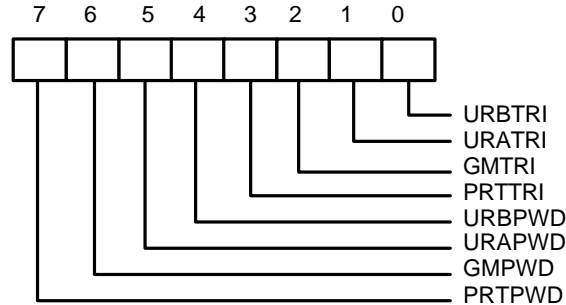
This bit selects the EPP version of parallel port:

- 0 Selects the EPP 1.9 version
- 1 Selects the EPP 1.7 version (default)

Bit 7-bit 6: Reserved.

Configuration Register 4 (CR4), default = 00H

When the device is in Extended Function mode and EFIR is 04H, the CR4 register can be accessed through EFDR. The bit definitions are as follows:



PRTPWD (Bit 7):

- 0 Supplies power to the parallel port (default)
- 1 Puts the parallel port in power-down mode

GMPWD (Bit 6):

- 0 Supplies power to the game port (default)
- 1 Puts the game port in power-down mode

URAPWD (Bit 5):

- 0 Supplies power to COMA (default)
- 1 Puts COMA in power-down mode

URBPWD (Bit 4):

- 0 Supplies power to COMB (default)
- 1 Puts COMB in power-down mode

PRTRRI (Bit 3):

This bit enables or disables the tri-state outputs of parallel port in power-down mode.

- 0 The output pins of the parallel port will not be tri-stated when parallel port is in power-down mode. (default)
- 1 The output pins of the parallel port will be tri-stated when parallel port is in power-down mode.

GMTRI (Bit 2):

This bit enables or disables the tri-state outputs of the game port in power-down mode.

- 0 The output pins of the game port will not be tri-stated when game port is in power-down mode. (default)
- 1 The output pins of the game port will be tri-stated when game port is in power-down mode.

URATRI (Bit 1):

This bit enables or disables the tri-state outputs of UARTA in power-down mode.

- 0 The output pins of UARTA will not be tri-stated when UARTA is in power-down mode.
- 1 The output pins of UARTA will be tri-stated when UARTA is in power-down mode.

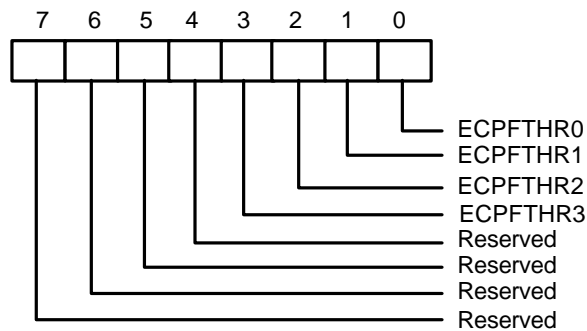
URBTRI (Bit 0):

This bit enables or disables the tri-state outputs of UARTB in power-down mode.

- 0 The output pins of UARTB will not be tri-stated when UARTB is in power-down mode.
- 1 The output pins of UARTB will be tri-stated when UARTB is in power-down mode.

Configuration Register 5 (CR5), default = 00H

When the device is in Extended Function mode and EFIR is 05H, the CR5 register can be accessed through EFDR. The bit definitions are as follows:

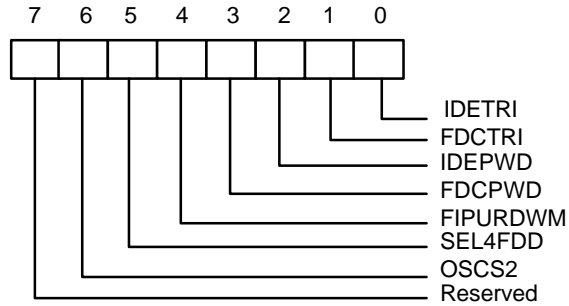


Bit 7-4: Reserved

ECPFTHR3-0 (bit 3-0): These four bits define the FIFO threshold for the ECP mode parallel port. The default value is 0000 after power-up.

Configuration Register 6 (CR6), default = 00H

When the device is in Extended Function mode and EFIR is 06H, the CR6 register can be accessed through EFDR. The bit definitions are as follows:



Bit 7: Reserved

OSCS2 (Bit 6): This bit and OSCS1, OSCS0 (bit 1, 0 of CR0) select one of the FDC87W22's power-down functions. Refer to descriptions of CR0. (Default to be 0)

SEL4FDD (Bit 5): Selects four FDD mode

0 Selects two FDD mode (default, see Table 9A)

1 Selects four FDD mode

nDSA, nDSB, nMOA and nMOB output pins are encoded as show in Table 9B to select four drives.

Table 9A

| DO REGISTER (3F2H) | | | | | | nMOB | nMOA | nDSB | nDSA | DRIVE SELECTED |
|----------------------|-------|-------|-------|-------|-------|------|------|------|------|-------------------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 1 | Bit 0 | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | -- |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | FDD A |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | FDD B |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | -- |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | -- |

Table 9B

| DO REGISTER (3F2H) | | | | | | nMOB | nMOA | nDSB | nDSA | DRIVE SELECTED |
|----------------------|-------|-------|-------|-------|-------|------|------|------|------|-------------------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 1 | Bit 0 | | | | | |
| 0 | 0 | 0 | 0 | X | X | 1 | 1 | x | x | -- |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | FDD A |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | FDD B |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | FDD C |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | FDD D |

FIPURDWN (Bit 4):

This bit controls the internal pull-up resistors of the FDC input pins nRDATA, nINDEX, nTRAK0, nDSKCHG, and nWP.

- 0 The internal pull-up resistors of FDC are turned on. (default)
- 1 The internal pull-up resistors of FDC are turned off.

FDCPWD (Bit 3):

This bit controls the power to the FDC.

- 0 Power is supplied to the FDC. (default)
- 1 Puts the FDC in power-down mode.

IDEPWD (Bit 2):

This bit controls the power of the IDE.

- 0 Power is supplied to the IDE. (default)
- 1 Puts the IDE in power-down mode.

FDCTRI (Bit 1):

This bit enables or disables the tri-state outputs of the FDC in power-down mode.

- 0 The output pins of the FDC will not be tri-stated when FDC is in power-down mode.
- 1 The output pins of the FDC will be tri-stated when FDC is in power-down mode.

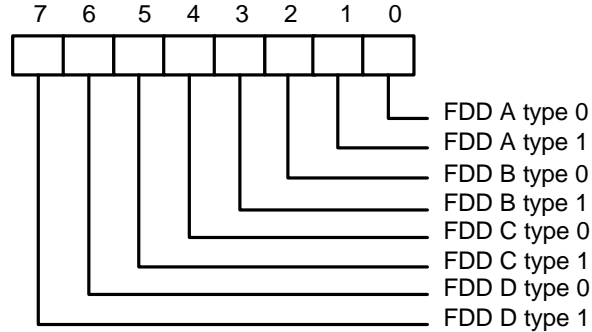
IDETRI (Bit 0):

This bit enables or disables the tri-state outputs of the IDE in power-down mode.

- 0 The output pins of the IDE will not be tri-stated when IDE is in power-down mode.
- 1 The output pins of the IDE will be tri-stated when IDE is in power-down mode.

Configuration Register 7 (CR7), default = 00H

When the device is in Extended Function mode and EFIR is 07H, the CR7 register can be accessed through EFDR. The bit definitions are as follows:



FDD A type 1, 0 (Bit 1, 0):

These two bits select the type of FDD A.

- 00 Selects normal mode. When nRWC = 0, the data transfer rate is 250 Kb/s. When nRWC= 1, the data transfer rate is 500 Kb/s.

Three mode FDD select (EN3MODE = 1):

- 01 nRWC= 0, selects 1.2 MB high-density FDD.
- 10 nRWC= 1, selects 1.44 MB high-density FDD.
- 11 Don't care nRWC, selects 720 KB double-density FDD.

FDD B type 1, 0 (Bit 3, 2):

These two bits select the type of FDD B.

- 00 Selects normal mode. When nRWC = 0, the data transfer rate is 250 Kb/s. When nRWC= 1, the data transfer rate is 500 Kb/s.

Three mode FDD select (EN3MODE = 1):

- 01 nRWC= 0, selects 1.2 MB high-density FDD.
- 10 nRWC = 1, selects 1.44 MB high-density FDD.
- 11 Don't care nRWC, selects 720 KB double-density FDD.

FDD C type 1, 0 (Bit 5, 4):

These two bits select the type of FDD C.

- 00 Selects normal mode. When nRWC = 0, the data transfer rate is 250 kb/s. When nRWC = 1, the data transfer rate is 500 kb/s.

Three mode FDD select (EN 3 MODE = 1):

- 01 nRWC = 0, selects 1.2 MB high-density FDD.
- 10 nRWC = 1, selects 1.44 MB high-density FDD.
- 11 Don't care nRWC, selects 720 KB double-density FDD.

FDD D type 1, 0 (Bit 7, 6):

These two bits select the type of FDD D.

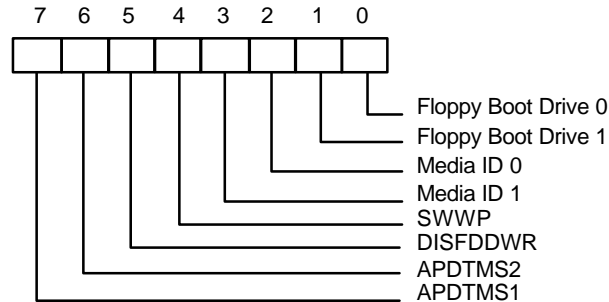
- 00 Selects normal mode. When nRWC = 0, the data transfer rate is 250 Kb/s. When nRWC = 1, the data transfer rate is 500 Kb/s.

Three mode FDD select (EN3MODE = 1):

- 01 nRWC = 0, selects 1.2 MB high-density FDD.
- 10 nRWC = 1, selects 1.44 MB high-density FDD.
- 11 Don't care nRWC, selects 720 KB double-density FDD.

Configuration Register 8 (CR8), default = 00H

When the device is in Extended Function mode and EFIR is 08H, the CR8 register can be accessed through EFDR. The bit definitions are as follows:



APDTMS2 APDTMS1 (Bit 6, 7):

These two bits select the count-down time of the automatic power-down mode counter.

| | |
|----|------------|
| 00 | 4 seconds |
| 01 | 32 seconds |
| 10 | 64 seconds |
| 11 | 4 minutes |

DISFDDWR (Bit 5):

This bit enables or disables FDD write data.

| | |
|---|--|
| 0 | Enables FDD write |
| 1 | Disables FDD write (forces pins nWE, nWD to stay high) |

Once this bit is set high, the FDC operates normally, but because pin nWE is inactive, the FDD will not write data to diskettes. For example, if a diskette is formatted with DISFDDWR = 1, after the format command has been executed, messages will be displayed that appear to indicate that the format is complete. If the diskette is removed from the disk drive and inserted again, however, typing the DIR command will reveal that the contents of the diskette have not been modified and the diskette was not actually reformatted.

This is because as the operating system (e.g., DOS) reads the diskette files, it keeps the files in memory. If there is a write operation, DOS will write data to the diskette and memory simultaneously. When DOS wants to read the diskette, it will first search the files in memory. If DOS finds the file in memory, it will not issue a read command to read the diskette. When DISFDDWR = 1, DOS still writes data to the diskette and memory, but only the data in memory are updated. If a read operation is performed, data are read from memory first, and not from the diskette. The action of removing the diskette from the drive and inserting it again forces the nDSKCHG pin active. DOS will then read the contents of the diskette and will show that the contents have not been modified. The same holds true with write commands.

The disable FDD write function allows users to protect diskettes against computer viruses by ensuring that no data are written to the diskette.

SWWP (Bit 4):

| | |
|---|--|
| 0 | Normal, use nWP to determine whether the FDD is write-protected or not |
| 1 | FDD is always write-protected |

Media ID 1 Media ID 0 (Bit 3, 2):

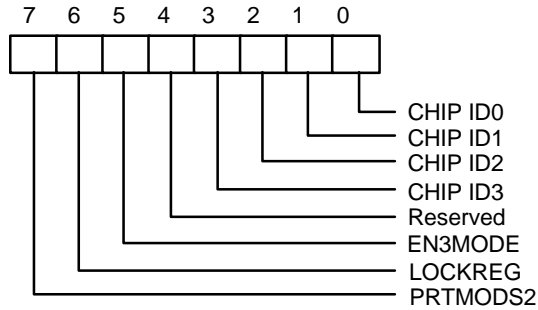
These two bits hold the media ID bit 1, 0 for three mode

Floppy Boot Drive 1 Floppy Boot Drive 0 (bit 1, 0)

These two bits hold the value of floppy boot drive 1 and drive 0 for three mode

Configuration Register 9 (CR9), default = 0AH

When the device is in Extended Function mode and EFIR is 09H, the CR9 register can be accessed through EFDR. The bit definitions are as follows:



PRTMODS2 (Bit 7):

This bit and PRTMODS1, PRTMODS0 (bits 3, 2 of CR0) select the operating mode of the FDC87W22. Refer to the descriptions of CR0.

LOCKREG (Bit 6):

This bit enables or disables the reading and writing of all configuration registers.

- 0 Enables the reading and writing of CR0-CR29
- 1 Disables the reading and writing of CR0-CR29 (locks FDC87W22 extension functions)

EN3MODE (Bit 5):

This bit enables or disables three mode FDD selection. When this bit is high, it enables the read/write 3F3H register.

- 0 Disables 3 mode FDD selection
- 1 Enables 3 mode FDD selection

When three mode FDD function is enabled, the value of nRWC depends on bit 5 and bit 4 of TDR(3F3H). The values of nRWC and their meaning are shown in Table 10.

Table 10

| BIT 5 OF TDR | BIT 4 OF TDR | nRWC | nRWC = 0 | nRWC= 1 |
|---------------------|---------------------|-------------|-----------------|----------------|
| 0 | 0 | Normal | 250K bps | 500K bps |
| 0 | 1 | 0 | 1.2 M FDD | X |
| 1 | 0 | 1 | X | 1.4M FDD |
| 1 | 1 | X | X | X |

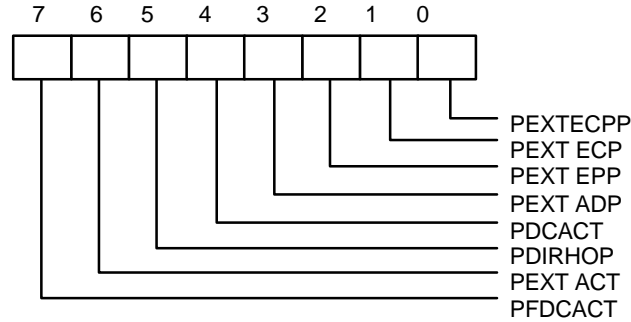
Bit 4: Reserved.

CHIP ID 3, CHIP ID 2, CHIP ID 1, CHIP ID 0 (Bit 3-0):

These four bits are read-only bits that contain chip identification information. The value is 0AH for FDC87W22 during a read.

Configuration Register A (CRA), default = 1FH

When the device is in Extended Function mode and EFIR is 0AH, the CRA register can be accessed through EFDR. The bit definitions are as follows:



PFDCACT (Bit 7):

This bit controls whether PFDCEN (pin 41) is active high or low in portable mode.

- 0 PFDCEN is active low
- 1 PFDCEN is active high

PEXTACT (Bit 6):

This bit controls whether PEXTEN (pin 39) is active high or low in portable mode. This pin can also reflect the mode of the parallel port: EXTADP mode, EPP mode, ECP mode, or ECP/EPP mode, or any combination of these modes.

- 0 PEXTEN is active low
- 1 PEXTEN is active high

Bit 5: Reserved.

PDCACT (Bit 4):

This bit controls whether the PDCIN pin is active high or low.

- 0 PDCIN is active low
- 1 PDCIN is active high

PEXTADP (Bit 3):

This bit controls whether the PEXTEN pin is active in EXTADP mode.

- 0 PEXTEN is not active in EXTADP mode
- 1 PEXTEN is active in EXTADP mode

PEXTEPP (Bit 2):

This bit controls whether the PEXTEN pin is active in EPP mode.

- 0 PEXTEN is not active in EPP mode
- 1 PEXTEN is active in EPP mode

PEXTECP (Bit 1):

This bit controls whether the PEXTEN pin is active in ECP mode.

- 0 PEXTEN is not active in ECP mode
- 1 PEXTEN is active in ECP mode

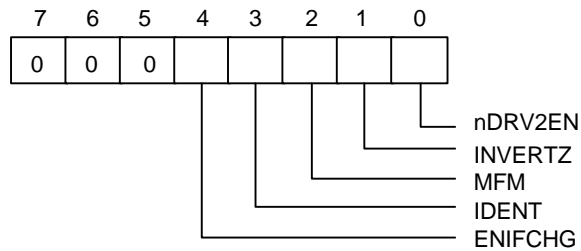
PEXTECPP (Bit 0):

This bit controls whether the PEXTEN pin is active in ECP/EPP mode.

- 0 PEXTEN is not active in ECP/EPP mode
- 1 PEXTEN is active in ECP/EPP mode

Configuration Register B (CR0B), default = 0CH

When the device is in Extended Function mode and EFIR is 0BH, the CRB register can be accessed through EFDR. The bit definitions are as follows:



Bit 7-5: These bits are reserved and are logic 0 during a read.

ENIFCHG (Bit 4):

This bit is active high. When active, it enables host interface mode change, which is determined by IDENT (Bit 3) and MFM (Bit 2).

IDENT (Bit 3):

This bit indicates the type of drive being accessed and changes the level on nRWC (pin 87).

- 0 nRWC will be active low for high data rates (typically used for 3.5" drives)
- 1 nRWC will be active high for high data rates (typically used for 5.25" drives)

When hardware reset or ENIFCHG is a logic 1, IDENT and MFM select one of three interface modes, as shown in Table 11.

Table 11

| IDENT | MFM | INTERFACE |
|-------|-----|---------------|
| 0 | 0 | Model 30 mode |
| 0 | 1 | PS/2 mode |
| 1 | 0 | AT mode |
| 1 | 1 | AT mode |

MFM (Bit 2):

This bit and IDENT select one of the three interface modes (PS/2 mode, Model 30, or PC/AT mode).

INTVERTZ (Bit 1):

This bit determines the polarity of all FDD interface signals.

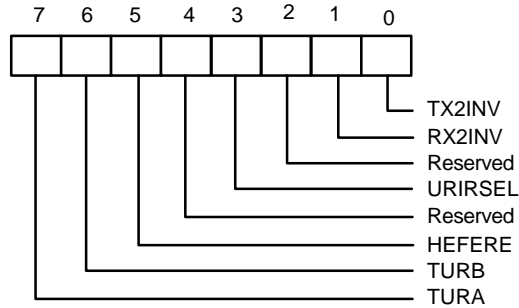
- 0 FDD interface signals are active low
- 1 FDD interface signals are active high

nDRV2EN (Bit 0): PS/2 mode only

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

Configuration Register C (CR0C), default = 28H

When the device is in Extended Function mode and EFIR is 0CH, the CR0C register can be accessed through EFDR. The bit definitions are as follows:



TURA (bit 7):

- 0 The clock source of UART A is 1.8462 MHz (24 MHz divide 13) (default)
- 1 The clock source of UART A is 24 MHz, it can make the baudrate of UART A up to 1.5 MHz

TURB (bit 6):

- 0 The clock source of UART B is 1.8462 MHz (24 MHz divide 13) (default)
- 1 The clock source of UART B is 24 MHz, it can make the baudrate of UART A up to 1.5 MHz

HEFERE (bit 5): This bit combines with HEFRAS (CR16 bit 0) to define how to enable Extended Function Registers.

| HEFRAS | HEFERE | Address and Value |
|--------|--------|--|
| 0 | 0 | write 88H to the location 250H |
| 0 | 1 | write 89H to the location 250H (default) |
| 1 | 0 | write 86H to the location 3F0H twice |
| 1 | 1 | write 87H to the location 3F0H twice |

The default value of HEFERE is 1.

Bit 4: Reserved.

URIRSEL (bit 3):

- 0 Select UART B as IR function.
- 1 Select UART B as normal function.

The default value of URIRSEL is 1.

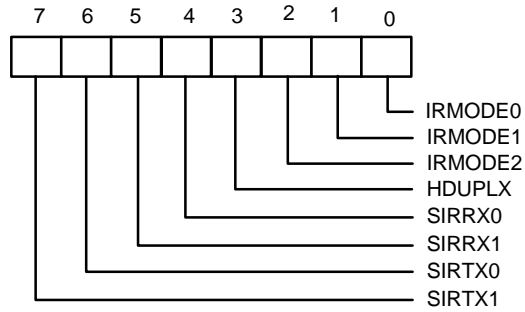
Bit 2: Reserved.

RX2INV (bit 1):

- 0 The SINB pin of UART B function or IRRX pin of IR function in normal condition.
- 1 Inverse the SINB pin of UART B function or IRRX pin of IR function TX2INV (bit 0):
- 0 The SOUTB pin of UART B function or IRTX pin of IR function in normal condition.
- 1 Inverse the SOUTB pin of UART B function or IRTX pin of IR function.

Configuration Register D (CR0D), default = a3H

When the device is in Extended Function mode and EFIR is 0DH, the CR0D register can be accessed through EFDR. The bit definitions are as follows:



SIRTX1 (bit 7): IRTX pin selection bit 1

SIRTX0 (bit 6): IRTX pin selection bit 0

| SIRTX1 | SIRTX0 | IRTX output on pin |
|--------|--------|--------------------|
| 0 | 0 | disabled |
| 0 | 1 | IRTX1 (pin 43) |
| 1 | 0 | IRTX2 (pin 95) |
| 1 | 1 | disabled |

SIRRX1 (bit 5): IRRX pin selection bit 1

SIRRX0 (bit 4): IRRX pin selection bit 0

| SIRRX1 | SIRRX0 | IRRX input on pin |
|--------|--------|-------------------|
| 0 | 0 | disabled |
| 0 | 1 | IRRX1 (pin 42) |
| 1 | 0 | IRRX2 (pin 94) |
| 1 | 1 | disabled |

HDUPLX (bit 3):

| | |
|---|---------------------------------|
| 0 | The IR function is Full Duplex. |
| 1 | The IR function is Half Duplex. |

IRMODE2 (bit 2): IR function mode selection bit 2

IRMODE1 (bit 1): IR function mode selection bit 1

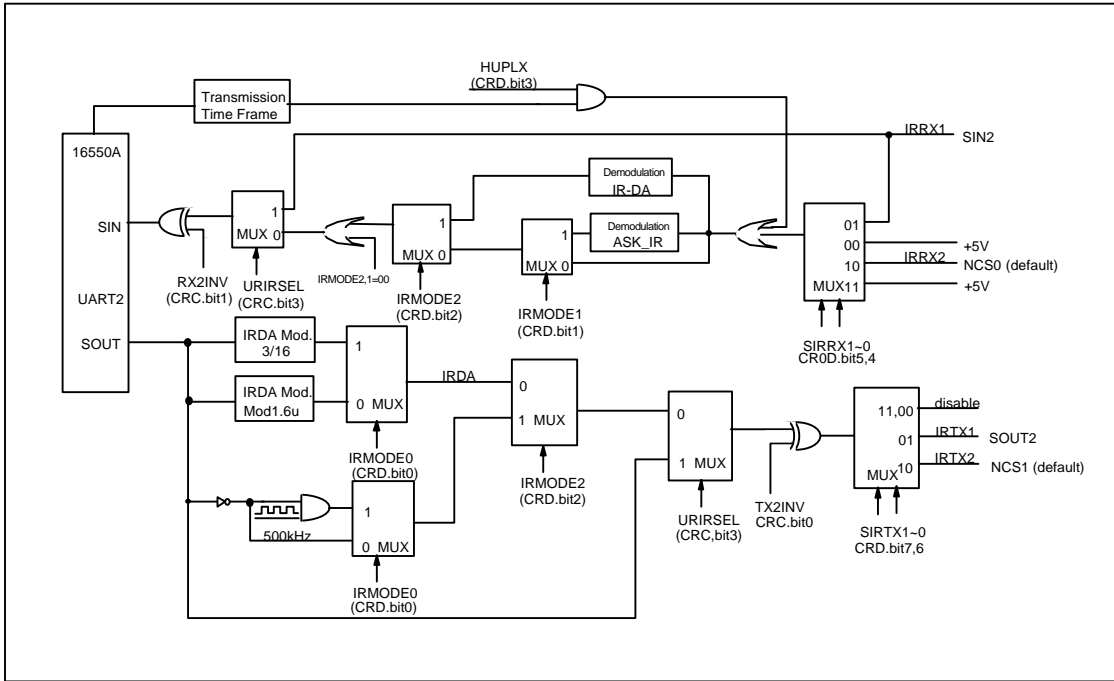
IRMODE0 (bit 0): IR function mode selection bit 0

| IR MODE | IR FUNCTION | IRTX | IRRX |
|---------|-------------|--------------------------------|------------------------|
| 00X | Disable | tri-state | high |
| 010* | IrDA | Active pulse 1.6 μ S | Demodulation into SINB |
| 011* | IrDA | Active pulse 3/16 bit time | Demodulation into SINB |
| 100 | ASK-IR | Inverting IRTX pin | routed to SINB |
| 101 | ASK-IR | Inverting IRTX & 500 kHz clock | routed to SINB |
| 110 | ASK-IR | Inverting IRTX | Demodulation into SINB |
| 111* | ASK-IR | Inverting IRTX & 500 kHz clock | Demodulation into SINB |

Note: The notation is normal mode in the IR function.

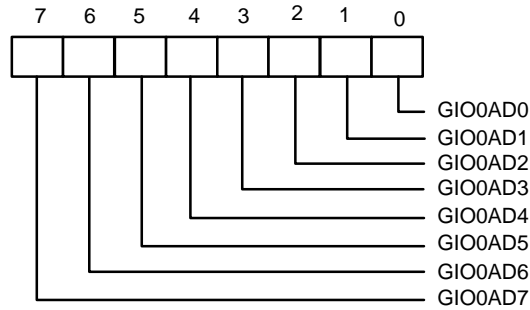
The SIR schematic diagram for registers CRC and CRD is shown below.

Configuration Register E (CR0E), Configuration Register F (CR0F)
 Reserved for testing. Should be kept all 0's.



Configuration Register 10 (CR10), default = 00H

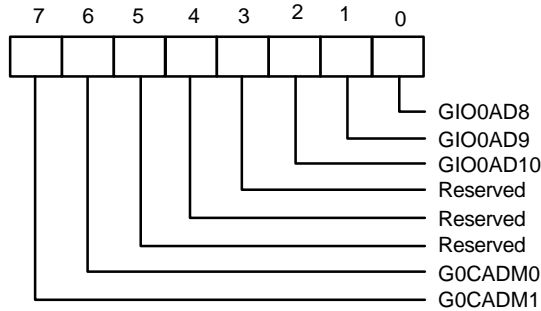
When the device is in Extended Function mode and EFIR is 10H, the CR10 register can be accessed through EFDR. The bit definitions are as follows:



GIO0AD7-GIO0AD0 (bit 7-bit 0): GIOP0 (pin 92) address bit 7 - bit 0.

Configuration Register 11 (CR11), default = 00H

When the device is in Extended Function mode and EFIR is 11H, the CR11 register can be accessed through EFDR. The bit definitions are as follows:



G0CADM1-G0CADM0 (bit 7-bit 6): GIOP0 address bit compare mode selection

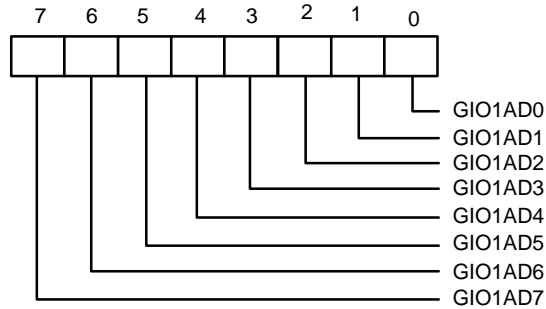
| G0CADM1 | G0CADM0 | GIOP0 pin |
|---------|---------|--|
| 0 | 0 | compare GIO0AD10-GIO0AD0 with SA10-SA0 |
| 0 | 1 | compare GIO0AD10-GIO0AD1 with SA10-SA1 |
| 1 | 0 | compare GIO0AD10-GIO0AD2 with SA10-SA2 |
| 1 | 1 | compare GIO0AD10-GIO0AD3 with SA10-SA3 |

Bit 5-bit 3: Reserved

GIO0AD10-GIO0AD8 (bit 2-bit 0): GIOP0 (pin 92) address bit 10-bit 8

Configuration Register 12 (CR12), default = 00H

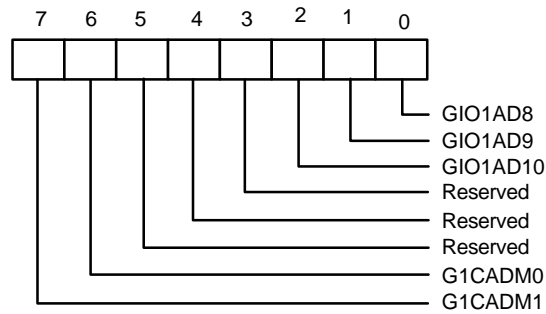
When the device is in Extended Function mode and EFIR is 12H, the CR12 register can be accessed through EFDR. The bit definitions are as follows:



GIO1AD7-GIO1AD0 (bit 7-bit 0): GIOP1 (pin 96) address bit 7-bit 0.

Configuration Register 13 (CR13), default = 00H

When the device is in Extended Function mode and EFIR is 13H, the CR13 register can be accessed through EFDR. The bit definitions are as follows:



G1CADM1-G1CADM0 (bit 7-bit 6): GIOP1 address bit compare mode selection

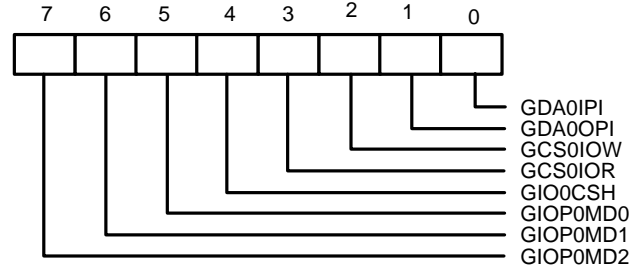
| G1CADM1 | G1CADM0 | GIOP1 pin |
|---------|---------|--|
| 0 | 0 | compare GIO1AD10-GIO1AD0 with SA10-SA0 |
| 0 | 1 | compare GIO1AD10-GIO1AD1 with SA10-SA1 |
| 1 | 0 | compare GIO1AD10-GIO1AD2 with SA10-SA2 |
| 1 | 1 | compare GIO1AD10-GIO1AD3 with SA10-SA3 |

Bit 5- bit 3: Reserved

GIO1AD10-GIO1AD8 (bit 2-it 0): GIOP1 (pin 96) address bit 10-bit 8

Configuration Register 14 (CR14), default = 00H

When the device is in Extended Function mode and EFIR is 14H, the CR14 register can be accessed through EFDR. The bit definitions are as follows:



GIOP0MD2-GIOP0MD0 (bit 7-bit 5): GIOP0 pin mode selection

| GIOP0MD2 | GIOP0MD1 | GIOP0MD0 | GIOP0 pin |
|----------|----------|----------|---|
| 0 | 0 | 0 | Inactive (tri-state) |
| 0 | 0 | 1 | as a data output pin (SD0→GIOP0), when (AEN = L) AND (NIOW = L) AND (SA10-0 = GIO0AD10-0), the value of SD0 will be present on GIOP0 |
| 0 | 1 | 0 | As a data input pin (GIOP0→SD0), when (AEN = L) AND (NIOR = L) AND (SA10-0 = GIO0AD10-0), the value of GIOP0 will be present on SD0 |
| 0 | 1 | 1 | As a data input/output pin (GIOP0↔SD0). When (AEN = L) AND (NIOW = L) AND (SA10-0 = GIO0AD10-0), the value of SD0 will be present on GIOP0 When (AEN = L) AND (NIOR = L) AND (SA10-0 = GIO0AD10-0), the value of GIOP0 will be present on SD0 |
| 1 | X | X | As a Chip Select pin, the pin will be active at (AEN = L) AND (SA10-0 = GIO0AD10-0) OR (NIOR = L) OR (NIOW = L) |

GIO0CSH(bit 4):

- | | |
|---|--|
| 0 | The Chip Select pin will be active LOW when (AEN = L) AND (SA10-0 = GIO0AD10-0) OR (NIOR = L) OR (NIOW = L) |
| 1 | The Chip Select pin will be active HIGH when (AEN = L) AND (SA10-0 = GIO0AD10-0) OR (NIOR = L) OR (NIOW = L) |

GCS0IOR (bit 3): See below.

GCS0IOW (bit 2): See below.

| GCS0IOR | GCS0IOW | |
|---------|---------|--|
| 0 | 0 | GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) |
| 0 | 1 | GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) AND (NIOW = L) |
| 1 | 0 | GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) AND (NIOR = L) |
| 1 | 1 | GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) AND (NIOW = L OR NIOR = L) |

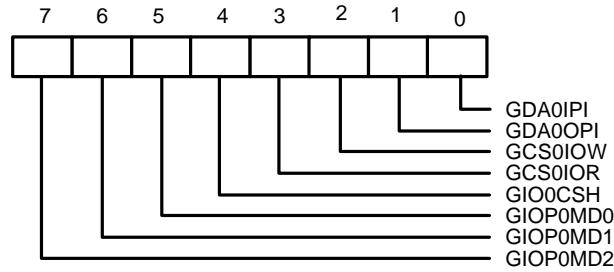
GDA0OPI (bit 1): See below.

GDA0IPI (bit 0): See below.

| GDA0OPI | GDA0IPI | |
|---------|---------|---|
| 0 | 0 | GIOP0 functions as a data pin, and GIOP0→SD0, SD0→GIOP0 |
| 0 | 1 | GIOP0 functions as a data pin, and inverse GIOP0→SD0, SD0→GIOP0 |
| 1 | 0 | GIOP0 functions as a data pin, and GIOP0→SD0, inverse SD0→GIOP0 |
| 1 | 1 | GIOP0 functions as a data pin, and inverse GIOP0→SD0, inverse SD0→GIOP0 |

Configuration Register 15 (CR15), default = 00H

When the device is in Extended Function mode and EFIR is 15H, the CR15 register can be accessed through EFDR. The bit definitions are as follows:



GIOP1MD2-GIOP1MD0 (bit 7-bit 5): GIOP1 pin mode selection

| GIOP1MD2 | GIOP1MD1 | GIOP1MD0 | GIOP1 pin |
|----------|----------|----------|---|
| 0 | 0 | 0 | Inactive (tri-state) |
| 0 | 0 | 1 | As a data output pin (SD1→GIOP1), when (AEN = L) AND (NIOW = L) AND (SA10-0 = GIO1AD10-0), the value of SD1 will be present on GIOP1 |
| 0 | 1 | 0 | As a data input pin (GIOP1→SD1), when (AEN = L) AND (NIOR = L) AND (SA10-0 = GIO1AD10-0), the value of GIOP1 will be present on SD1 |
| 0 | 1 | 1 | As a data input/output pin (GIOP1↔SD1). When (AEN = L) AND (NIOW = L) AND (SA10-0 = GIO1AD10-0), the value of SD1 will be present on GIOP1 When (AEN = L) AND (NIOR = L) AND (SA10-0 = GIO1AD10-0), the value of GIOP1 will be present on SD1 |
| 1 | X | X | As a Chip Select pin, the pin will be active at (AEN = L) AND (SA10-0 = GIO1AD10-0) OR (NIOR = L) OR (NIOW = L) |

GIO1CSH (bit 4):

| | |
|---|--|
| 0 | The Chip Select pin will active LOW when (AEN = L) AND (SA10-0 = GIOAD10-0) OR (NIOR = L) OR (NIOW = L) |
| 1 | The Chip Select pin will active HIGH when (AEN = L) AND (SA10-0 = GIOAD10-0) OR (NIOR = L) OR (NIOW = L) |

GCS1IOR (bit 3): See below.

GCS1IOW (bit 2): See below.

| GCS1IOR | GCS1IOW | |
|---------|---------|--|
| 0 | 0 | GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) |
| 0 | 1 | GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) AND (NIOW = L) |
| 1 | 0 | GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) AND (NIOR = L) |
| 1 | 1 | GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) AND (NIOW = L OR NIOR = L) |

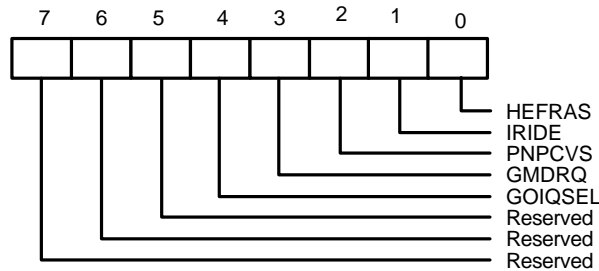
GDA0OPI (bit 1): See below.

GDA1IPI (bit 0): See below.

| GDA1OPI | GDA1IPI | |
|---------|---------|---|
| 0 | 0 | GIOP1 functions as a data pin, and GIOP1→SD1, SD1→GIOP1 |
| 0 | 1 | GIOP1 functions as a data pin, and inverse GIOP1→SD1, SD1→GIOP1 |
| 1 | 0 | GIOP1 functions as a data pin, and GIOP1→SD1, inverse SD1→GIOP1 |
| 1 | 1 | GIOP1 functions as a data pin, and inverse GIOP1→SD1, inverse SD1→GIOP1 |

Configuration Register 16 (CR16), default = 0eH

When the device is in Extended Function mode and EFIR is 16H, the CR16 register can be accessed through EFDR. The bit definitions are as follows:



Bit 7-bit 5: Reserved.

GOIQSEL (bit 4):

- 0 Pins 92, 96 function as IRQ_B, IRQ_A, respectively.
- 1 Pins 92, 96 function as GIO0, GIO1, respectively.

The corresponding power-on setting pin is NRTSB (pin 45).

GMDRQ (bit 3):

- 0 Pins 39, 41 function as DRQ_A, NDACK_A, respectively.
- 1 Pins 39, 41 function as NGMWR, NGMRD, respectively.

The corresponding power-on setting pin is SOUTB (pin 43).

PNPCVS (bit 2):

- 0 PnP-related registers (CR1E, CR20-29) reset to be all 0s.
- 1 Default settings for these registers.

The corresponding power-on setting pin is NRTSA (pin 36).

| PnP register | PNPCVS = 1 | PNPCVS = 0 |
|--------------|------------|------------|
| CR1E | 81H | 00H |
| CR20 | FCH | 00H |
| CR21 | 7CH | 00H |
| CR22 | FDH | 00H |
| CR23 | DEH | 00H |
| CR24 | FEH | 00H |
| CR25 | BEH | 00H |
| CR26 | 23H | 00H |
| CR27 | 65H | 00H |
| CR28 | 43H | 00H |
| CR29 | 62H | 00H |

Note: The new value of PNPCVS must be complementary to the old one to make an effective change. For example, the user must set PNPCVS to 1 first and then reset it to 0 to reset these PnP registers if the present value of PNPCVS is 0.

IRIDE (bit 1):

- 0 Pins 1, 91, 94, 95 function as IDE ports.
- 1 Pins 1, 91, 94, 95 function as IR ports.

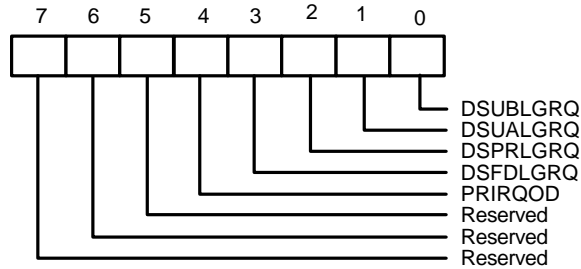
The corresponding power-on setting pin is SOUTA (pin 38).

| Pin | IRIDE = 0 | IRIDE = 1 |
|-----|-----------|-----------|
| 1 | NRSTIDE | IRQ_G |
| 91 | NIDBEN | IRQ_H |
| 94 | NCS0 | IRRX2 |
| 95 | NCS1 | IRTX2 |

HEFRAS (bit 0): Combines with HEFERE (CR0C bit 5) to define how to access Extended Function Registers (refer to CR0C bit 5 description). The corresponding power-on setting pin is NDTRA (pin 35).

Configuration Register 17 (CR17), default = 00H

When the device is in Extended Function mode and EFIR is 17H, the CR17 register can be accessed through EFDR. The bit definitions are as follows:



Bit 7-bit 5: Reserved.

PRIRQOD (bit4):

- 0 Printer IRQ ports are totem-poles in SPP mode and open-drains in ECP/EPP mode.
- 1 Printer IRQ ports are totem-poles in all modes.

DSFDLGRQ (bit 3):

- 0 Enable FDC legacy mode on IRQ and DRQ selections. DO register bit 3 has effect on selecting IRQ.
- 1 Disable FDC legacy mode on IRQ and DRQ selections. DO register bit 3 has no effect on selecting IRQ.

DSPRLGRQ (bit 2):

- 0 Enable PRT legacy mode on IRQ and DRQ selections. DCR bit 4 has effect on selecting IRQ.
- 1 Disable PRT legacy mode on IRQ and DRQ selections. DCR bit 4 has no effect on selecting IRQ.

DSUALGRQ (bit 1):

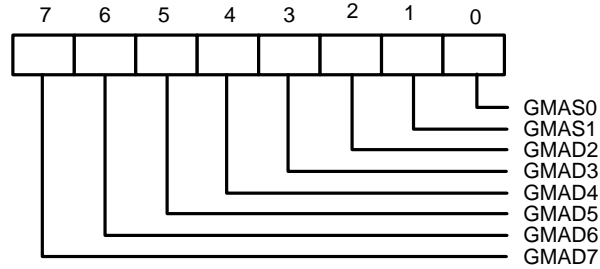
- 0 Enable UART A legacy mode on IRQ selection. MCR bit 3 has effect on selecting IRQ.
- 1 Disable UART A legacy mode on IRQ selection. MCR bit 3 has no effect on selecting IRQ.

DSUBLGRQ (bit 0):

- 0 Enable UART B legacy mode on IRQ selection. MCR bit 3 has effect on selecting IRQ.
- 1 Disable UART B legacy mode on IRQ selection. MCR bit 3 has no effect on selecting IRQ.

Configuration Register 1E (CR1E)

When the device is in Extended Function mode and EFIR is 1EH, the CR1E register can be accessed through EFDR. Default = 81H if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



This register is used to select the base address of Game Chip Select Decoder (GAMECS) from 100H-3F0H on 16-byte boundaries. NCS = 0 and A10 = 0 are required to qualify the GAMECS output.

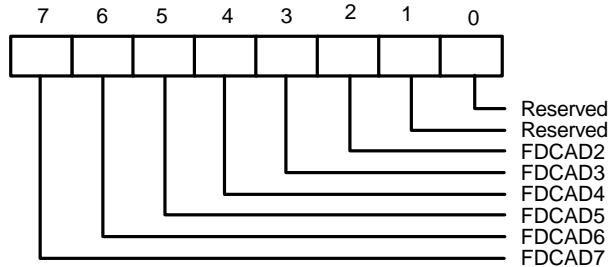
GMAD7-GMAD2 (bit 7-bit 2): match A[9:4].

GMAS1-GMAS0 (bit 1-bit 0): GAMECS configuration.

| | |
|----|--------------------------------|
| 00 | GAMECS disable |
| 01 | 1-byte decode, A[3:0] = 0001b |
| 10 | 8-byte decode, A[3:0] = 0xxx b |
| 11 | 16-byte decode, A[3:0] = xxxxb |

Configuration Register 20 (CR20)

When the device is in Extended Function mode and EFIR is 20H, the CR20 register can be accessed through EFDR. Default = FCH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:

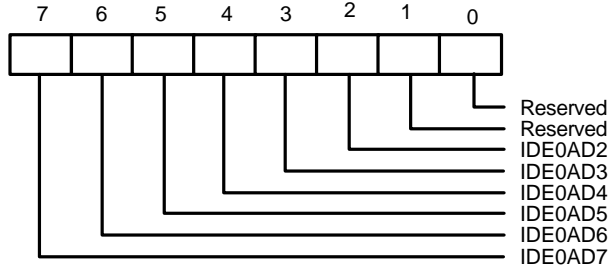


This register is used to select the base address of the Floppy Disk Controller (FDC) from 100H-3F0H on 16-byte boundaries. NCS = 0 and A10 = 0 are required to access the FDC registers. A[3:0] are always decoded as 0xxx.

FDCAD7-FDCAD2 (bit 7-bit 2): match A[9:4]. Bit 7 = 0 and bit 6 = 0 disable this decode.
 Bit 1-bit 0: Reserved, fixed at zero.

Configuration Register 21 (CR21)

When the device is in Extended Function mode and EFIR is 21H, the CR21 register can be accessed through EFDR. Default = 7CH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



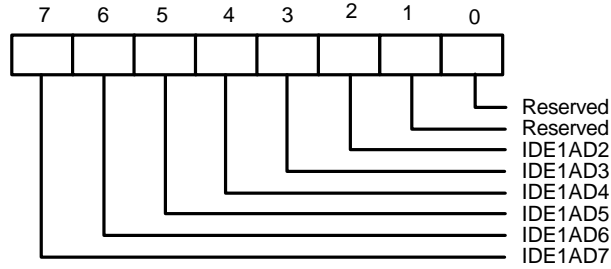
This register is used to select the base address of the IDE Interface Control Registers from 100H-3F0H on 16-byte boundaries. NCS = 0 and A10 = 0 are required to access the IDE registers. A[3:0] are always decoded as 0xxx.

IDE0AD7-IDE0AD2 (bit 7-bit 2): match A[9:4]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 1-bit 0: Reserved, fixed at zero.

Configuration Register 22 (CR22)

When the device is in Extended Function mode and EFIR is 22H, the CR22 register can be accessed through EFDR. Default = FDH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



This register is used to select the base address of the IDE Interface Alternate Status Register from 106H-3F6H on 16-byte boundaries + 6. NCS = 0 and A10 = 0 are required to access the IDE Alternate Status register. A[3:0] must be 0110b.

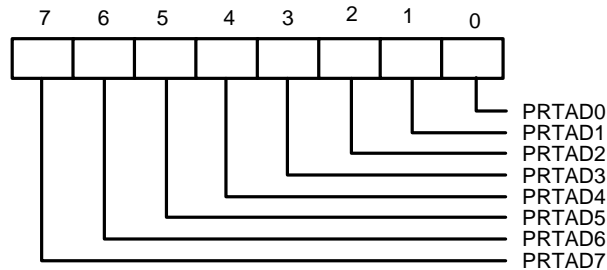
IDE1AD7-IDE1AD2 (bit 7-bit 2): match A[9:4]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 1: Reserved, fixed at zero.

Bit 0: Reserved, fixed at one.

Configuration Register 23 (CR23)

When the device is in Extended Function mode and EFIR is 23H, the CR23 register can be accessed through EFDR. Default = DEH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:

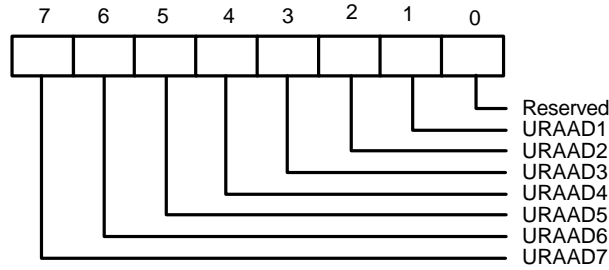


This register is used to select the base address of the parallel port. If EPP is disable, the parallel port can be set from 100H-3FCH on 4-byte boundaries. If EPP is enable, the parallel port can be set from 100H-3F8H on 8-byte boundaries. NCS = 0 and A10 = 0 are required to access the parallel port when in compatible, bi-directional, or EPP modes. A10 is active in ECP mode.

PRTAD7-PRTAD0 (bit 7-bit 0): match A[9:2]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Configuration Register 24 (CR24)

When the device is in Extended Function mode and EFIR is 24H, the CR24 register can be accessed through EFDR. Default = FEH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



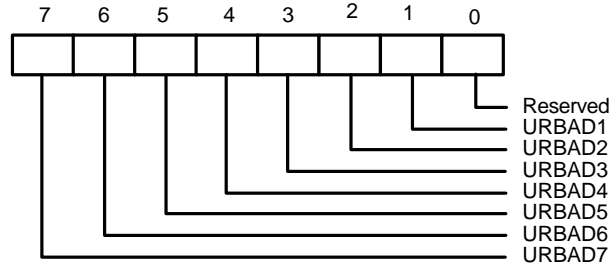
This register is used to select the base address of the UART A from 100H-3F8H on 8-byte boundaries. NCS = 0 and A10 = 0 are required to access the UART A registers. A[2:0] are don't-care conditions.

URAAD7-URAAD1 (bit 7-bit 1): match A[9:3]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 0: Reserved, fixed at zero.

Configuration Register 25 (CR25)

When the device is in Extended Function mode and EFIR is 25H, the CR25 register can be accessed through EFDR. Default = BEH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



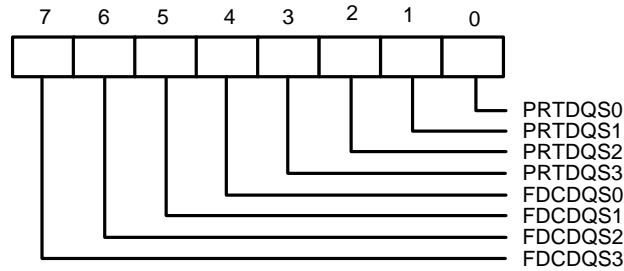
This register is used to select the base address of the UART B from 100H-3F8H on 8-byte boundaries. NCS = 0 and A10 = 0 are required to access the UART B registers. A[2:0] are don't-care conditions.

URBAD7-URBAD1 (bit 7-bit 1): match A[9:3]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 0: Reserved, fixed at zero.

Configuration Register 26 (CR26)

When the device is in Extended Function mode and EFIR is 26H, the CR26 register can be accessed through EFDR. Default = 23H if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



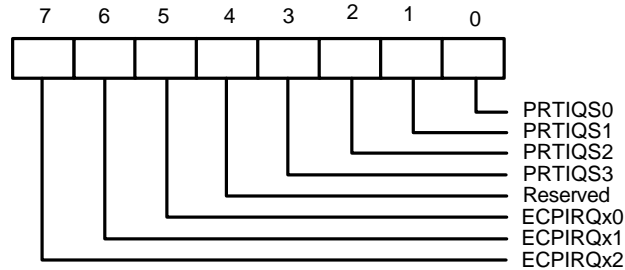
FDCDQS3-FDCDQS0 (bit 7-bit 4): Allocate DMA resource for FDC.

PRTDQS3-PRTDQS0 (bit 3-bit 0): Allocate DMA resource for PRT.

| bit 7- bit4, bit 3 - bit 0 | DMA selected |
|----------------------------|--------------|
| 0000 | None |
| 0001 | DMA_A |
| 0010 | DMA_B |
| 0011 | DMA_C |

Configuration Register 27 (CR27)

When the device is in Extended Function mode and EFIR is 27, the CR27 register can be accessed through EFDR. Default = 05H if CR6 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



ECPIRQx2-ECPIRQx0 (bit7-bit 5): These bits are configurable equivalents to bit[5:3] of cnfgB register in ECP mode except that cnfgB[5:3] are read-only bits. They indicate the IRQ resource assigned for the ECP printer port. It is the software designer's responsibility to ensure that CR27[7:5] and CR27[3:0] are consistent. For example, CR27[7:5] should be filled with 001 (select IRQ 7) if CR27[3:0] are to be programmed as 0101 (select IRQ_E) while IRQ_E is connected to IRQ 7.

| CR27[7:5] | IRQ Resource |
|-----------|---|
| 000 | Reflect other IRQ resources selected by CR27[3:0] (default) |
| 001 | IRQ 7 |
| 010 | IRQ 9 |
| 011 | IRQ 10 |
| 100 | IRQ 11 |
| 101 | IRQ 14 |
| 110 | IRQ 15 |
| 111 | IRQ 5 |

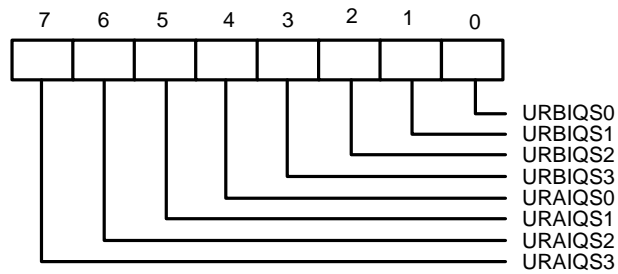
Bit 4: Reserved.

PRTIQS3-PRTIQS0 (bit 3-bit 0): Select IRQ resource for the parallel port. Any unselected IRQ is in tristate.

| CR27[3:0] | IRQ selected |
|-----------|--------------|
| 0000 | None |
| 0001 | IRQ_A |
| 0010 | IRQ_B |
| 0011 | IRQ_C |
| 0100 | IRQ_D |
| 0101 | IRQ_E |
| 0110 | IRQ_F |
| 0111 | IRQ_G |
| 1000 | IRQ_H |

Configuration Register 28 (CR28)

When the device is in Extended Function mode and EFIR is 28, the CR28 register can be accessed through EFDR. Default = 43H if CR6 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:

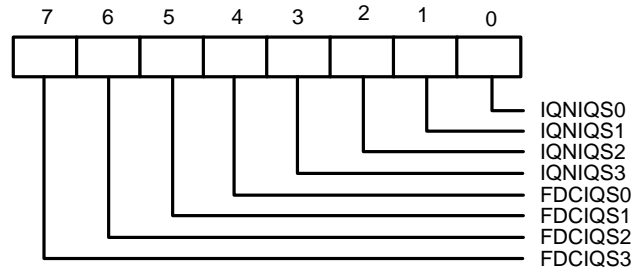


URAIQS3-URAIQS0 (bit 7-bit 4): Allocate interrupt resource for UART A.

URBIQS3-URBIQS0 (bit 3-bit 0): Allocate interrupt resource for UART B.

Configuration Register 29 (CR29)

When the device is in Extended Function mode and EFIR is 29, the CR29 register can be accessed through EFDR. Default = 62H if CR6 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



FDCIQS3-FDCIQS0 (bit 7-bit 4): Allocate interrupt resource for FDC.

IQNIQS3-IQNIQS0 (bit 3-bit 0): Allocate interrupt resource for IRQIN.

Table 12 - Bit Map Configuration Registers

| Register | Power-on Reset Value | D7 | D6 | D5 | D4 |
|----------|------------------------|----------|----------|-----------|----------|
| CR0 | 0000 0000 | 0 | 0 | 0 | 0 |
| CR1 | 0000 0000 | ABCHG | 0 | 0 | 0 |
| CR2 | 0000 0000 | RA9 | RA8 | RA7 | RA6 |
| CR3 | 0011 0000 | 0 | GMENL | EPPVER | GMODS |
| CR4 | 0000 0000 | PRTPWD | GMPWD | URAPWD | URBPWD |
| CR5 | 0000 0000 | 0 | 0 | 0 | 0 |
| CR6 | 0000 0000 | 0 | OSCS2 | SEL4FDD | FIPURDWN |
| CR7 | 0000 0000 | FDD D T1 | FDD D T0 | FDD C T1 | FDD C T0 |
| CR8 | 0000 0000 | APDTMS1 | APDTMS0 | DISFDDWR | SWWP |
| CR9 | 0000 1010 | PRTMODS2 | LOCKREG | EN3MODE | 0 |
| CRA | 0001 1111 | PFDCACT | PEXTACT | PDIRHISOP | PDCHACT |
| CRB | 0000 0000 | 0 | 0 | 0 | ENIFCHG |
| CRC | 0010 1000 | TURA | TURB | HEFERE | 0 |
| CRD | 1010 0011 | SIRTX1 | SIRTX0 | SIRRX1 | SIRRX0 |
| CR10 | 0000 0000 | GIO0AD7 | GIO0AD6 | GIO0AD5 | GIO0AD4 |
| CR11 | 0000 0000 | 0 | 0 | 0 | 0 |
| CR12 | 0000 0000 | GIO1AD7 | GIO1AD6 | GIO1AD5 | GIO1AD4 |
| CR13 | 0000 0000 | 0 | 0 | 0 | 0 |
| CR14 | 0000 0000 | GIOP0MD2 | GIOP0MD1 | GIOP0MD0 | GIO0CSH |
| CR15 | 0000 0000 | GIOP1MD2 | GIOP1MD1 | GIOP1MD0 | GIO1CSH |
| CR16 | 000s ssss ¹ | 0 | 0 | 0 | GOIQSEL |
| CR17 | 0000 0000 | 0 | 0 | 0 | PRIRQOD |
| CR1E | 1000 0001 ² | GMAD7 | GMAD6 | GMAD5 | GMAD4 |
| CR20 | 1111 1100 ² | FDCAD7 | FDCAD6 | FDCAD5 | FDCAD4 |
| CR21 | 0111 1100 ² | IDE0AD7 | IDE0AD6 | IDE0AD5 | IDE0AD4 |
| CR22 | 1111 1101 ² | IDE1AD7 | IDE1AD6 | IDE1AD5 | IDE1AD4 |
| CR23 | 1101 1110 ² | PRTAD7 | PRTAD6 | PRTAD5 | PRTAD4 |
| CR24 | 1111 1110 ² | URAAD7 | URAAD6 | URAAD5 | URAAD4 |
| CR25 | 1011 1110 ² | URBAD7 | URBAD6 | URBAD5 | URBAD4 |
| CR26 | 0010 0011 ² | FD CDQS3 | FD CDQS2 | FD CDQS1 | FD CDQS0 |
| CR27 | 0000 0101 ² | ECPIRQx2 | ECPIRQx1 | ECPIRQx0 | 0 |
| CR28 | 0100 0011 ² | URAIQS3 | URAIQS2 | URAIQS1 | URAIQS0 |
| CR29 | 0110 0010 ² | FDCIQS3 | FDCIQS2 | FDCIQS1 | FDCIQS0 |

Notes:

1. 's' means its value depends on corresponding power-on setting pin.
2. These default values are valid when CR16 bit 2 is 1 during power-on reset; They will be all 0's if CR16 bit 2 is 0.

Table 12 - Bit Map Configuration Registers (continued)

| Register | Power-on Reset Value | D3 | D2 | D1 | D0 |
|----------|------------------------|-----------|-----------|-----------|-----------|
| CR0 | 0000 0000 | PRTMODS1 | PRTMODS0 | OSCS1 | OSCS0 |
| CR1 | 0000 0000 | 0 | 0 | 0 | 0 |
| CR2 | 0000 0000 | RA5 | RA4 | RA3 | CEA |
| CR3 | 0011 0000 | 0 | 0 | SUAMIDI | SUBMIDI |
| CR4 | 0000 0000 | PRTTRI | GMTRI | URATRI | URBTRI |
| CR5 | 0000 0000 | ECPFTHR3 | ECPFTHR2 | ECPFTHR1 | ECPFTHR0 |
| CR6 | 0000 0000 | FDCPWD | IDEPWD | FDCTRI | IDETRI |
| CR7 | 0000 0000 | FDD B T1 | FDD B T0 | FDD A T1 | FDD A T0 |
| CR8 | 0000 0000 | MEDIA 1 | MEDIA 0 | BOOT 1 | BOOT 0 |
| CR9 | 0000 1010 | CHIP ID 3 | CHIP ID 2 | CHIP ID 1 | CHIP ID 0 |
| CRA | 0001 1111 | PEXTADP | PEXTEPP | PEXTECP | PEXTECPP |
| CRB | 0000 0000 | IDENT | MFM | INVERTZ | DRV2EN |
| CRC | 0010 1000 | URIRSEL | 0 | RX2INV | TX2INV |
| CRD | 1010 0011 | HDUPLX | IRMODE2 | IRMODE1 | IRMODE0 |
| CR10 | 0000 0000 | GIO0AD3 | GIO0AD2 | GIO0AD1 | GIO0AD0 |
| CR11 | 0000 0000 | 0 | GIO0AD10 | GIO0AD9 | GIO0AD8 |
| CR12 | 0000 0000 | GIO1AD3 | GIO1AD2 | GIO1AD1 | GIO1AD0 |
| CR13 | 0000 0000 | 0 | GIO1AD10 | GIO1AD9 | GIO1AD8 |
| CR14 | 0000 0000 | GCS0IOR | GCS0IOW | GDA0OPI | GDA0IPI |
| CR15 | 0000 0000 | GCS1IOR | GCS1IOW | GDA1OPI | GDA1IPI |
| CR16 | 000s ssss ¹ | GMDRQ | PNPCVS | IRIDE | HEFRAS |
| CR17 | 0000 0000 | DSFDLGRQ | DSPRLGRQ | DSUALGRQ | DSUBLGRQ |
| CR1E | 1000 0001 ² | GMAD3 | GMAD2 | GMAS1 | GMAS0 |
| CR20 | 1111 1100 ² | FDCAD3 | FDCAD2 | 0 | 0 |
| CR21 | 0111 1100 ² | IDE0AD3 | IDE0AD2 | 0 | 0 |
| CR22 | 1111 1101 ² | IDE1AD3 | IDE1AD2 | 0 | 1 |
| CR23 | 1101 1110 ² | PRTAD3 | PRTAD2 | PRTAD1 | PRTAD0 |
| CR24 | 1111 1110 ² | URAAD3 | URAAD2 | URAAD1 | 0 |
| CR25 | 1011 1110 ² | URBAD3 | URBAD2 | URBAD1 | 0 |
| CR26 | 0010 0011 ² | PRTDQS3 | PRTDQS2 | PRTDQS1 | PRTDQS0 |
| CR27 | 0000 0101 ² | PRTIQS3 | PRTIQS2 | PRTIQS1 | PRTIQS0 |
| CR28 | 0100 0011 ² | URBIQS3 | URBIQS2 | URBIQS1 | URBIQS0 |
| CR29 | 0110 0010 ² | IQNIQS3 | IQNIQS2 | IQNIQS1 | IQNIQS0 |

Notes:

1. 's' means its value depends on corresponding power-on setting pin.

2. These default values are valid when CR16 bit 2 is 1 during power-on reset; They will be all 0's if CR16 bit 2 is 0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
|-----------------------|-----------------|------|
| Power Supply Voltage | -0.5 to 7.0 | V |
| Input Voltage | -0.5 to VDD+0.5 | V |
| Operating Temperature | 0 to +70 | °C |
| Storage Temperature | -55 to+ 150 | °C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(Ta = 0° C to 70° C, VDD = 5V ± 10%, VSS = 0V)

| PARAMETER | SYM. | MIN. | MAX. | UNIT | CONDITIONS |
|--|------------------|------|-----------------------|------|-----------------------------------|
| I/O_{8t} - TTL level bi-directional pin with source-sink capabilities of 8 mA | | | | | |
| Input Low Voltage | V _{IL} | -0.5 | 0.8 | V | |
| Input High Voltage | V _{IH} | 2.0 | V _{DD} + 0.5 | V | |
| Output Low Voltage | V _{OL} | | 0.4 | V | I _{OL} = 8 mA |
| Output High Voltage | V _{OH} | 2.4 | | V | I _{OH} = -8 mA |
| Input High Leakage | I _{LIH} | | +10 | μA | V _{IN} = V _{DD} |
| Input Low Leakage | I _{LIL} | | -10 | μA | V _{IN} = 0V |
| I/O_{12t} - TTL level bi-directional pin with source-sink capabilities of 12 mA | | | | | |
| Input Low Voltage | V _{IL} | -0.5 | 0.8 | V | |
| Input High Voltage | V _{IH} | 2.0 | V _{DD} + 0.5 | V | |
| Output Low Voltage | V _{OL} | | 0.4 | V | I _{OL} = 12 mA |
| Output High Voltage | V _{OH} | 2.4 | | V | I _{OH} = -12 mA |
| Input High Leakage | I _{LIH} | | +10 | μA | V _{IN} = V _{DD} |
| Input Low Leakage | I _{LIL} | | -10 | μA | V _{IN} = 0V |
| I/O_{24t} - TTL level bi-directional pin with source-sink capabilities of 24 mA | | | | | |
| Input Low Voltage | V _{IL} | -0.5 | 0.8 | V | |
| Input High Voltage | V _{IH} | 2.0 | V _{DD} + 0.5 | V | |
| Output Low Voltage | V _{OL} | | 0.4 | V | I _{OL} = 24 mA |
| Output High Voltage | V _{OH} | 2.4 | | V | I _{OH} = -24 mA |

| PARAMETER | SYM. | MIN. | MAX. | UNIT | CONDITIONS |
|--|----------|---------------------|---------------------|---------|---------------------------|
| Input High Leakage | I_{LH} | | +10 | μA | $V_{IN} = V_{DD}$ |
| Input Low Leakage | I_{LL} | | -10 | μA | $V_{IN} = 0V$ |
| OUT_{8t} - TTL level output pin with source-sink capabilities of 8 mA | | | | | |
| Output Low Voltage | V_{OL} | | 0.4 | V | $I_{OL} = 8 \text{ mA}$ |
| Output High Voltage | V_{OH} | 2.4 | | V | $I_{OH} = -8 \text{ mA}$ |
| OUT_{12t} - TTL level output pin with source-sink capabilities of 12 mA | | | | | |
| Output Low Voltage | V_{OL} | | 0.4 | V | $I_{OL} = 12 \text{ mA}$ |
| Output High Voltage | V_{OH} | 2.4 | | V | $I_{OH} = -12 \text{ mA}$ |
| OD₁₂ - Open-drain output pin with sink capabilities of 12 mA | | | | | |
| Output Low Voltage | V_{OL} | | 0.4 | V | $I_{OL} = 12 \text{ mA}$ |
| OD₂₄ - Open-drain output pin with sink capabilities of 24 mA | | | | | |
| Output Low Voltage | V_{OL} | | 0.4 | V | $I_{OL} = 24 \text{ mA}$ |
| IN_t - TTL level input pin | | | | | |
| Input Low Voltage | V_{IL} | -0.5 | 0.8 | V | |
| Input High Voltage | V_{IH} | 2.0 | $V_{DD} + 0.5$ | V | |
| Input High Leakage | I_{LH} | | +10 | μA | $V_{IN} = V_{DD}$ |
| Input Low Leakage | I_{LL} | | -10 | μA | $V_{IN} = 0V$ |
| IN_c - CMOS level input pin | | | | | |
| Input Low Voltage | V_{IL} | -0.5 | $0.3 \times V_{DD}$ | V | |
| Input High Voltage | V_{IH} | $0.7 \times V_{DD}$ | $V_{DD} + 0.5$ | V | |
| Input High Leakage | I_{LH} | | +10 | μA | $V_{IN} = V_{DD}$ |
| Input Low Leakage | I_{LL} | | -10 | μA | $V_{IN} = 0V$ |
| IN_{cs} - CMOS level schmitt-triggered input pin | | | | | |
| Input Low Voltage | V_{IL} | -0.5 | 1.8 | V | |
| Input High Voltage | V_{IH} | 3.0 | $V_{DD} + 0.5$ | V | |
| Input High Leakage | I_{LH} | | +10 | μA | $V_{IN} = V_{DD}$ |
| Input Low Leakage | I_{LL} | | -10 | μA | $V_{IN} = 0V$ |

AC CHARACTERISTICS

FDC: Data rate = 1 MB/500 KB/300 KB/250 KB/sec.

| PARAMETER | SYM. | TEST CONDITIONS | MIN. | TYP. (NOTE 1) | MAX. | UNIT |
|---|------|-----------------|--------------|---------------|--------------|------|
| SA9-SA0, AEN, nDACK, nCS, setup time to nIOR± | TAR | | 25 | | | nS |
| SA9-SA0, AEN, nDACK, hold time for nIOR± | TAR | | 0 | | | nS |
| nIOR width | TRR | | 80 | | | nS |
| Data access time from nIOR± | TFD | CL = 100 pf | | | 80 | nS |
| Data hold from nIOR± | TDH | CL = 100 pf | 10 | | | nS |
| SD to from nIOR± | TDF | CL = 100 pf | 10 | | 50 | nS |
| IRQ delay from nIOR± | TRI | | | | 360/570 /675 | nS |
| SA9-SA0, AEN, nDACK, setup time to nIOW± | TAW | | 25 | | | nS |
| SA9-SA0, AEN, nDACK, hold time for nIOW± | TWA | | 0 | | | nS |
| nIOW width | TWW | | 60 | | | nS |
| Data setup time to nIOW± | TDW | | 60 | | | nS |
| Data hold time from nIOW± | TWD | | 0 | | | nS |
| IRQ delay from nIOW± | TWI | | | | 360/570 /675 | nS |
| DRQ cycle time | TMCY | | 27 | | | μS |
| DRQ delay time nDACK± | TAM | | | | 50 | nS |
| DRQ to nDACK delay | TMA | | 0 | | | nS |
| nDACK width | TAA | | 260/430 /510 | | | nS |
| nIOR delay from nDRQ | TMR | | 0 | | | nS |
| nIOW delay from nDRQ | TMW | | 0 | | | nS |

| PARAMETER | SYM. | TEST CONDITIONS | MIN. | TYP. (NOTE 1) | MAX. | UNIT |
|-------------------------------------|------|-----------------|-----------------------|-----------------|-------------------|------|
| nIOW or nIOR response time from DRQ | TMRW | | | 6/12 /20/24 | | μS |
| TC width | TTC | | 135/ 220 /260 | | | nS |
| RESET width | TRST | | 1.8/3 /3.5 | | | μS |
| nINDEX width | TIDX | | 0.5/ 0.9 /1.0 | | | μS |
| nDIR setup time to nSTEP | TDST | | 1.0/ 1.6 /2.0 | | | μS |
| nDIR hold time from nSTEP | TSTD | | 24/ 40/ 48 | | | μS |
| nSTEP pulse width | TSTP | | 6.8/ 11.5 /13.8 | 7/11.7 /14 | 7.2/11.9 /14.2 | μS |
| nSTEP cycle width | TSC | | Note 2 | Note 2 | Note 2 | μS |
| nWD pulse width | TWDD | | 100/ 185 /225 | 125/210 /250 | 150/235 /275 | μS |
| Write precompensation | TWPC | | 100/ 138 /225 | 125/210 /250 | 150/235 /275 | μS |

Notes:

1. Typical values for T = 25° C and normal supply voltage.
2. Programmable from 2 mS through 32 mS in 2 mS increments.

IDE

| PARAMETER | SYMBOL | MAX. | UNIT |
|---|--------|------|------|
| nCS0, nCS1 delay from SA valid | T1 | 50 | nS |
| DBENL, DBENH delay from AEN, IOCS16, SA | T2 | 50 | nS |
| IDED7 to D7 delay (read cycle) | T4 | 50 | nS |
| D7 to IDED7 delay (write cycle) | T3 | 50 | nS |

UART/Parallel Port

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | MAX. | UNIT |
|--|--------|-----------------|------|------------|-----------|
| Delay from Stop to Set Interrupt | TSINT | | 9/16 | | Baud Rate |
| Delay from nIOR Reset Interrupt | TRINT | 100 pF Loading | | 1 | μS |
| Delay from Initial IRQ Reset to Transmit Start | TIRS | | 1/16 | 8/16 | Baud Rate |
| Delay from to Reset interrupt | THR | 100 pF Loading | | 175 | nS |
| Delay from Initial nIOW to interrupt | TSI | | 9/16 | 16/16 | Baud Rate |
| Delay from Stop to Set Interrupt | TSTI | | | 1/2 | Baud Rate |
| Delay from nIOR to Reset Interrupt | TIR | 100 pF Loading | | 250 | nS |
| Delay from nIOW to Output | TMWO | 100 pF Loading | | 200 | nS |
| Set Interrupt Delay from Modem Input | TSIM | | | 250 | nS |
| Reset Interrupt Delay from nIOR | TRIM | | | 250 | nS |
| Interrupt Active Delay | TIAD | 100 pF Loading | | 25 | nS |
| Interrupt Inactive Delay | TIID | 100 pF Loading | | 30 | nS |
| Baud Divisor | N | 100 pF Loading | | $2^{16}-1$ | |

Extension Adapter Mode

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT |
|----------------------------------|------|------|------|------|------|
| nXRD, nXWR Delay from nIOR, nIOW | tx1 | | | 50 | nS |
| XA<0:2> Delay from SA<0:2> | tx2 | | | 50 | nS |
| XD<0:7> Setup time | tx3 | 50 | | | nS |
| XD<0:7> Hold time | tx4 | 0 | | | nS |
| IRQ & Delay from XIRQ | tx5 | | | 50 | nS |
| DRQX Delay from XDRQ | tx6 | | | 50 | nS |
| nXDACK Delay from nDACKX | tx7 | | | 50 | nS |
| XTC Delay from TC | tx8 | | | 50 | nS |

Parallel Port Mode Parameters

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|---|------|------|------|------|
| PD0-7, nINDEX, nSTROBE, nAUTOFD Delay from nIOW | t1 | | 100 | nS |
| IRQ Delay from nACK, nFAULT | t2 | | 60 | nS |
| IRQ Delay from nIOW | t3 | | 105 | nS |
| IRQ Active Low in ECP and EPP Modes | t4 | 200 | 300 | nS |
| nERROR Active to IRQ Active | t5 | | 105 | nS |

EPP Data or Address Read Cycle Timing Parameters

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|--|------|------|------|------|
| Ax Valid to nIOR Asserted | t1 | 40 | | nS |
| IOCHRDY Deasserted to nIOR Deasserted | t2 | 0 | | nS |
| nIOR Deasserted to Ax Valid | t3 | 10 | 10 | nS |
| nIOR Deasserted to nIOW or nIOR Asserted | t4 | 40 | | |
| nIOR Asserted to IOCHRDY Asserted | t5 | 0 | 24 | nS |
| PD Valid to SD Valid | t6 | 0 | 75 | nS |
| nIOR Deasserted to SD Hi-Z (Hold Time) | t7 | 0 | 40 | μS |
| SD Valid to IOCHRDY Deasserted | t8 | 0 | 85 | nS |
| nWAIT Deasserted to IOCHRDY Deasserted | t9 | 60 | 160 | nS |
| PD Hi-Z to PDBIR Set | t10 | 0 | | nS |
| nWRITE Deasserted to nIOR Asserted | t13 | 0 | | nS |
| nWAIT Asserted to nWRITE Deasserted | t14 | 0 | 185 | nS |
| nWAIT Deasserted to nWRITE Modified | t15 | 60 | 190 | nS |
| nIOR Asserted to PD Hi-Z | t16 | 0 | 50 | nS |
| nWAIT Asserted to PD Hi-Z | t17 | 60 | 180 | nS |
| Command Asserted to PD Valid | t18 | 0 | | nS |
| Command Deasserted to PD Hi-Z | t19 | 0 | | nS |
| nWAIT Deasserted to PD Drive | t20 | 60 | 190 | nS |
| nWRITE Deasserted to Command | t21 | 1 | | nS |
| PBDIR Set to Command | t22 | 0 | 20 | nS |
| PD Hi-Z to Command Asserted | t23 | 0 | 30 | nS |
| nWAIT Asserted to Command Asserted | t24 | 0 | 195 | nS |
| nWAIT Deasserted to Command Deasserted | t25 | 60 | 180 | nS |
| Time out | t26 | 10 | 12 | nS |
| PD Valid to nWAIT Deasserted | t27 | 0 | | nS |
| PD Hi-Z to nWAIT Deasserted | t28 | 0 | | μS |

EPP Data or Address Write Cycle Timing Parameters

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|---|------|------|------|------|
| Ax Valid to nIOW Asserted | t1 | 40 | | nS |
| SD Valid to IOW Asserted | t2 | 10 | | nS |
| nIOW Deasserted to Ax Invalid | t3 | 10 | | nS |
| nWAIT Deasserted to IOCHRDY Deasserted | t4 | 0 | | nS |
| Command Asserted to nWAIT Deasserted | t5 | 10 | | nS |
| nIOW Deasserted to nIOW or nIOR Asserted | t6 | 40 | | nS |
| IOCHRDY Deasserted to nIOW Deasserted | t7 | 0 | 24 | nS |
| nWAIT Asserted to Command Asserted | t8 | 60 | 160 | nS |
| nIOW Asserted to nWAIT Asserted | t9 | 0 | 70 | nS |
| PBDIR Low to nWRITE Asserted | t10 | 0 | | nS |
| nWAIT Asserted to nWRITE Asserted | t11 | 60 | 185 | nS |
| nWAIT Asserted to nWRITE Change | t12 | 60 | 185 | nS |
| nIOW Asserted to PD Valid | t13 | 0 | 50 | nS |
| nWAIT Asserted to PD Invalid | t14 | 0 | | nS |
| PD Invalid to Command Asserted | t15 | 10 | | nS |
| nIOW to Command Asserted | t16 | 5 | 35 | nS |
| nWAIT Asserted to Command Asserted | t17 | 60 | 210 | nS |
| nWAIT Deasserted to Command Deasserted | t18 | 60 | 190 | nS |
| Command Asserted to nWAIT Deasserted | t19 | 0 | 10 | μS |
| Time out | t20 | 10 | 12 | μS |
| Command Deasserted to nWAIT Asserted | t21 | 0 | | nS |
| nIOW Deasserted to nWRITE Deasserted and PD invalid | t22 | 0 | | nS |

Parallel Port FIFO Timing Parameters

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---------------------------------|--------|------|------|------|
| DATA Valid to nSTROBE Active | t1 | 600 | | nS |
| nSTROBE Active Pulse Width | t2 | 600 | | nS |
| DATA Hold from nSTROBE Inactive | t3 | 450 | | nS |
| BUSY Inactive to PD Inactive | t4 | 80 | | nS |
| BUSY Inactive to nSTROBE Active | t5 | 680 | | nS |
| nSTROBE Active to BUSY Active | t6 | | 500 | nS |

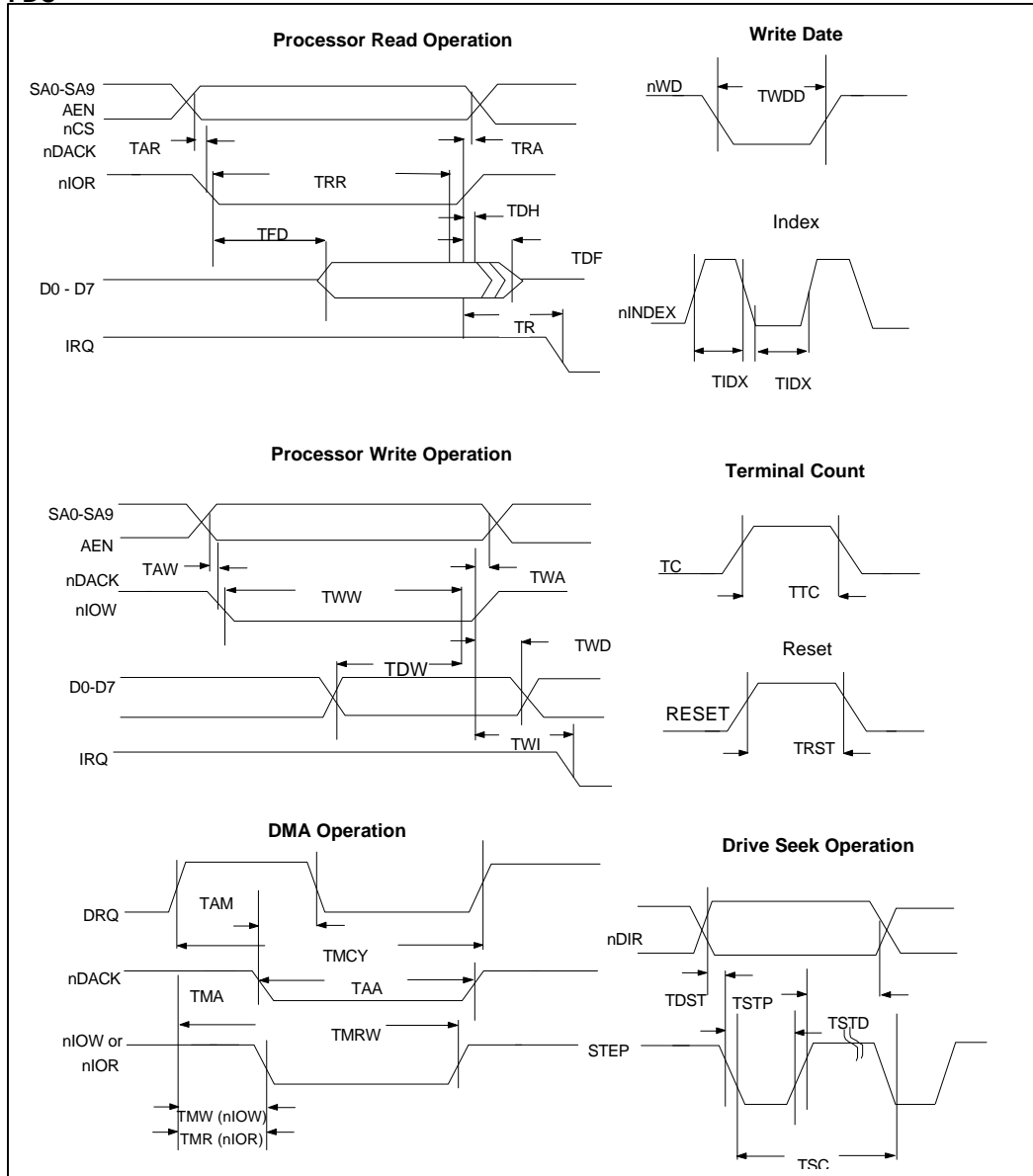
ECP Parallel Port Forward Timing Parameters

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---------------------------------------|--------|------|------|------|
| nAUTOFD Valid to nSTROBE Asserted | t1 | 0 | 60 | nS |
| PD Valid to nSTROBE Asserted | t2 | 0 | 60 | nS |
| BUSY Deasserted to nAUTOFD Changed | t3 | 80 | 180 | nS |
| BUSY Deasserted to PD Changed | t4 | 80 | 180 | nS |
| nSTROBE Deasserted to BUSY Deasserted | t5 | 0 | | nS |
| BUSY Deasserted to nSTROBE Asserted | t6 | 80 | 200 | nS |
| nSTROBE Asserted to BUSY Asserted | t7 | 0 | | nS |
| BUSY Asserted to nSTROBE Deasserted | t8 | 80 | 180 | nS |

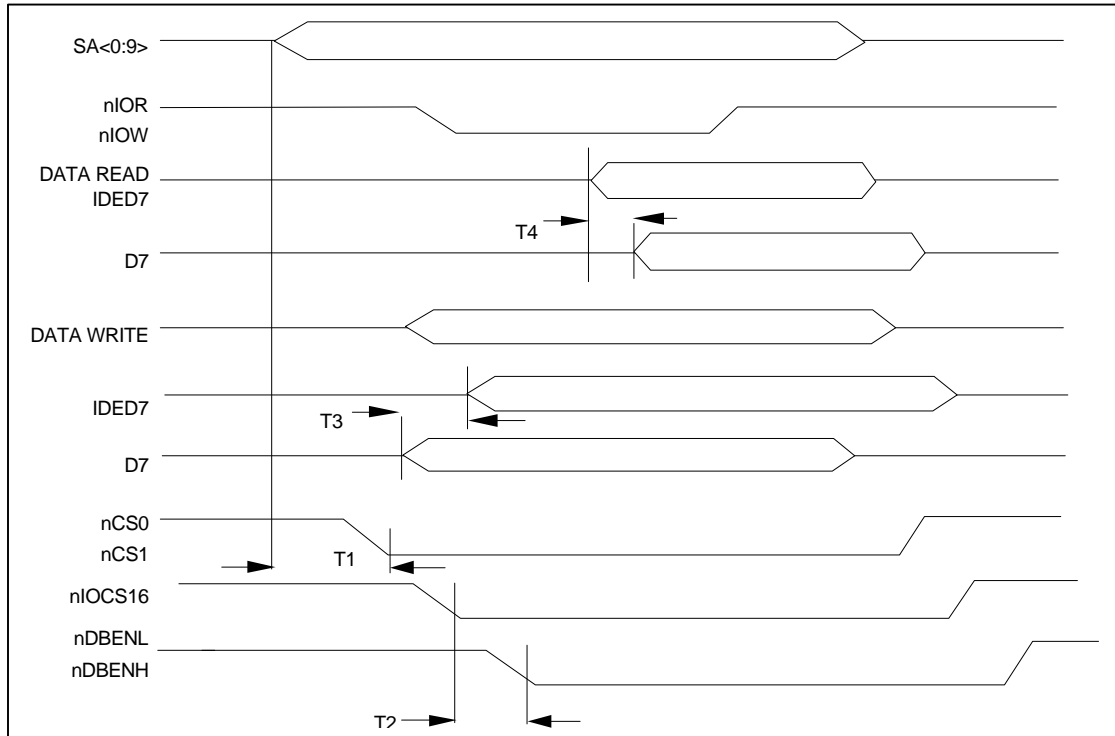
ECP Parallel Port Reverse Timing Parameters

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---------------------------------------|--------|------|------|------|
| PD Valid to nACK Asserted | t1 | 0 | | nS |
| nAUTOFD Deasserted to PD Changed | t2 | 0 | | nS |
| nAUTOFD Asserted to nACK Asserted | t3 | 0 | | nS |
| nAUTOFD Deasserted to nACK Deasserted | t4 | 0 | | nS |
| nACK Deasserted to nAUTOFD Asserted | t5 | 80 | 200 | nS |
| PD Changed to nAUTOFD Deasserted | t6 | 80 | 200 | nS |

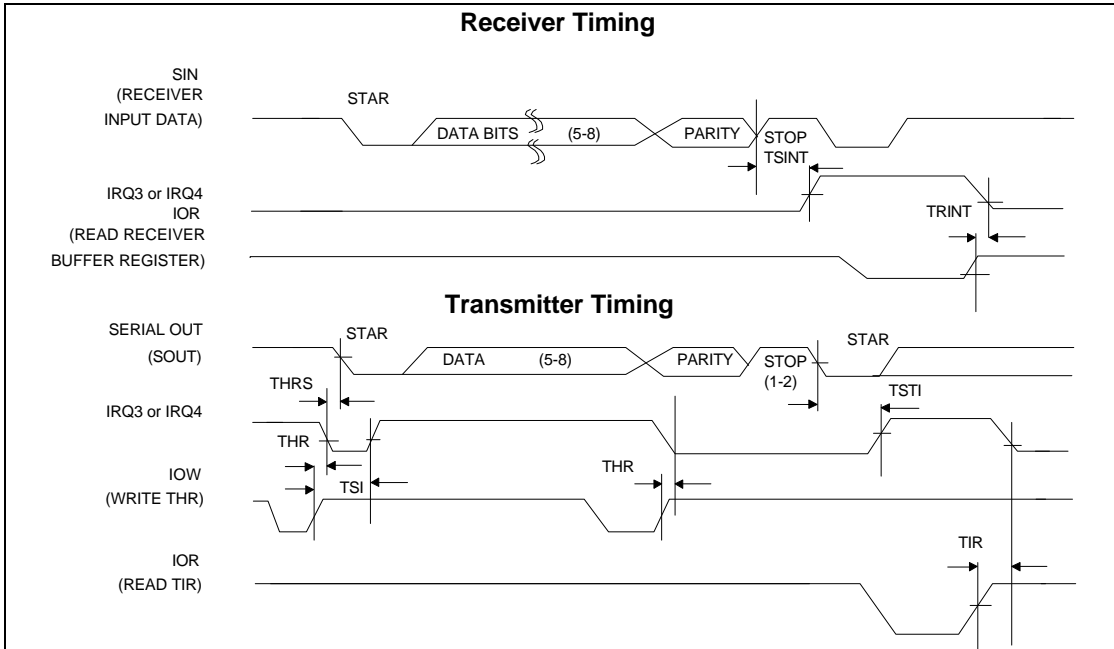
TIMING WAVEFORMS
FDC



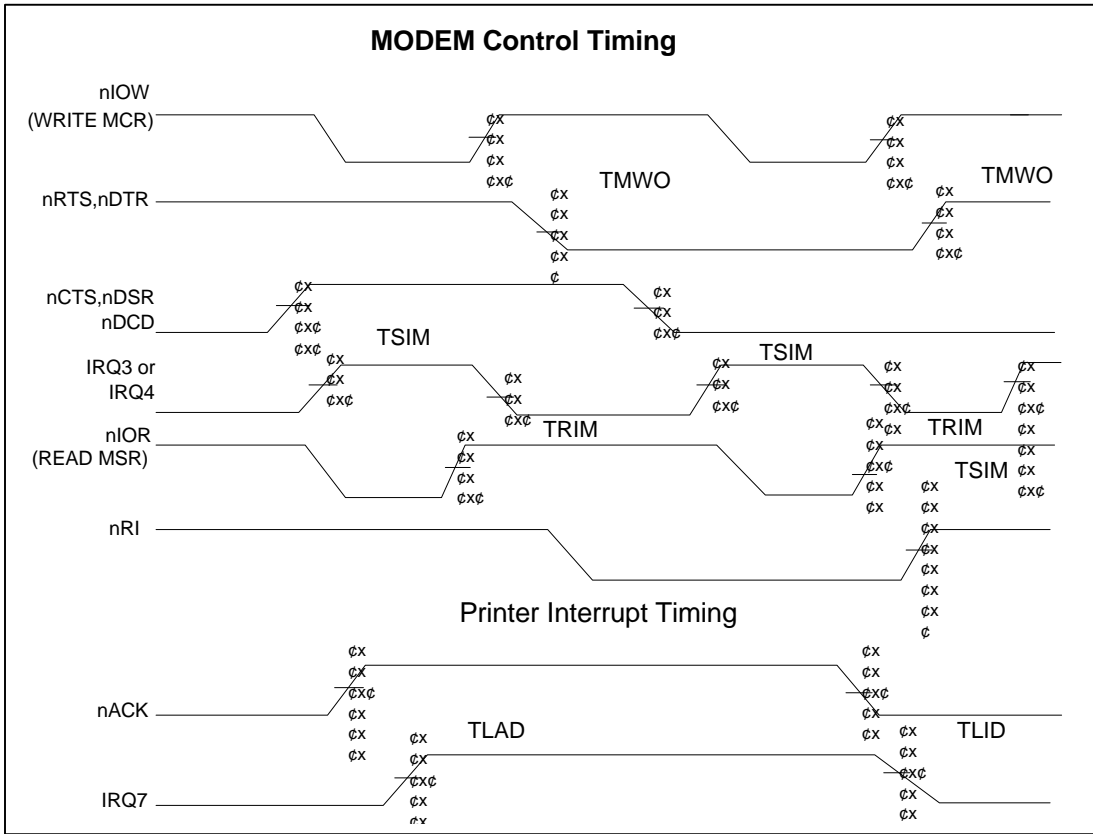
IDE



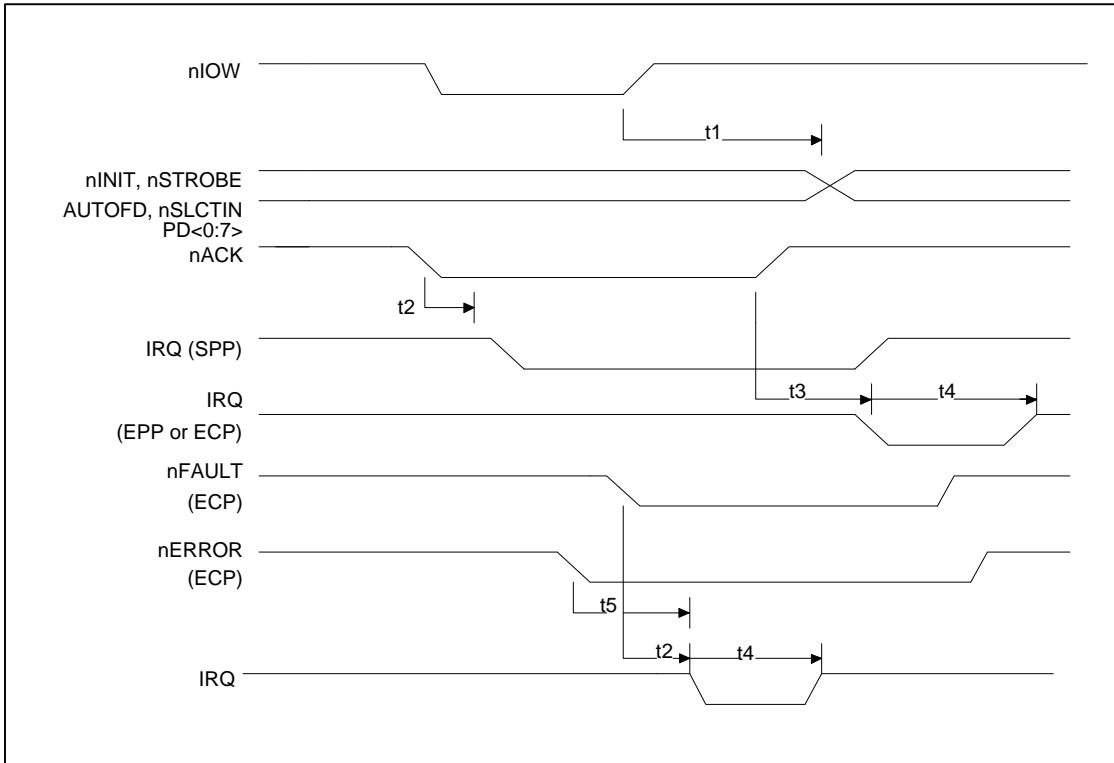
UART/Parallel



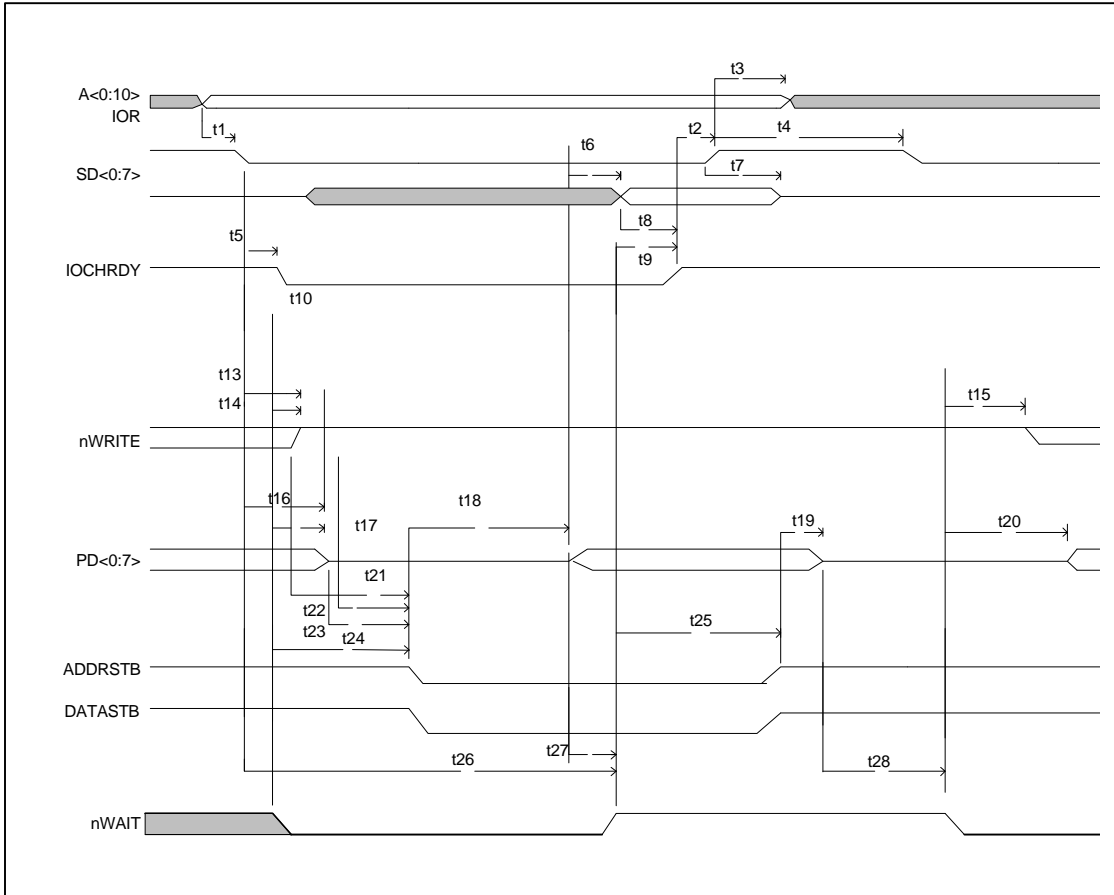
Modem Control Timing



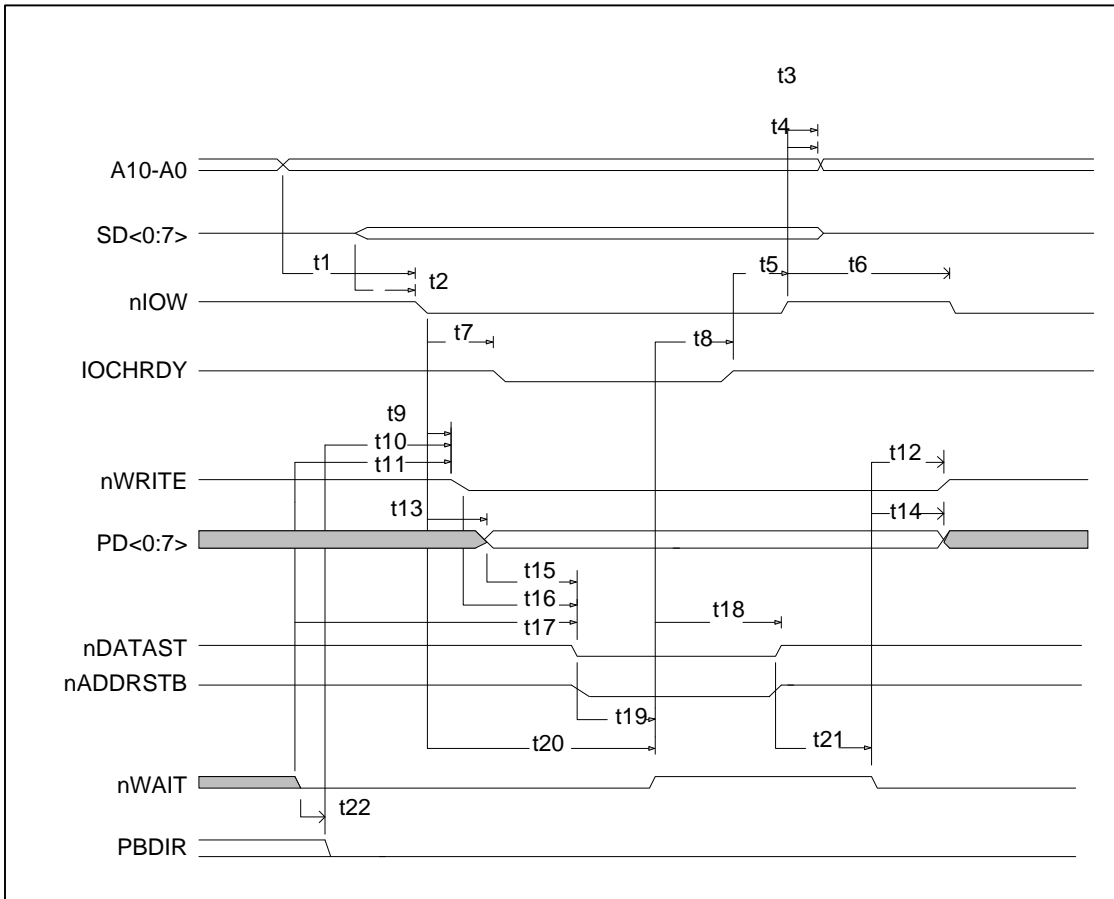
**Parallel Port
Parallel Port Timing**



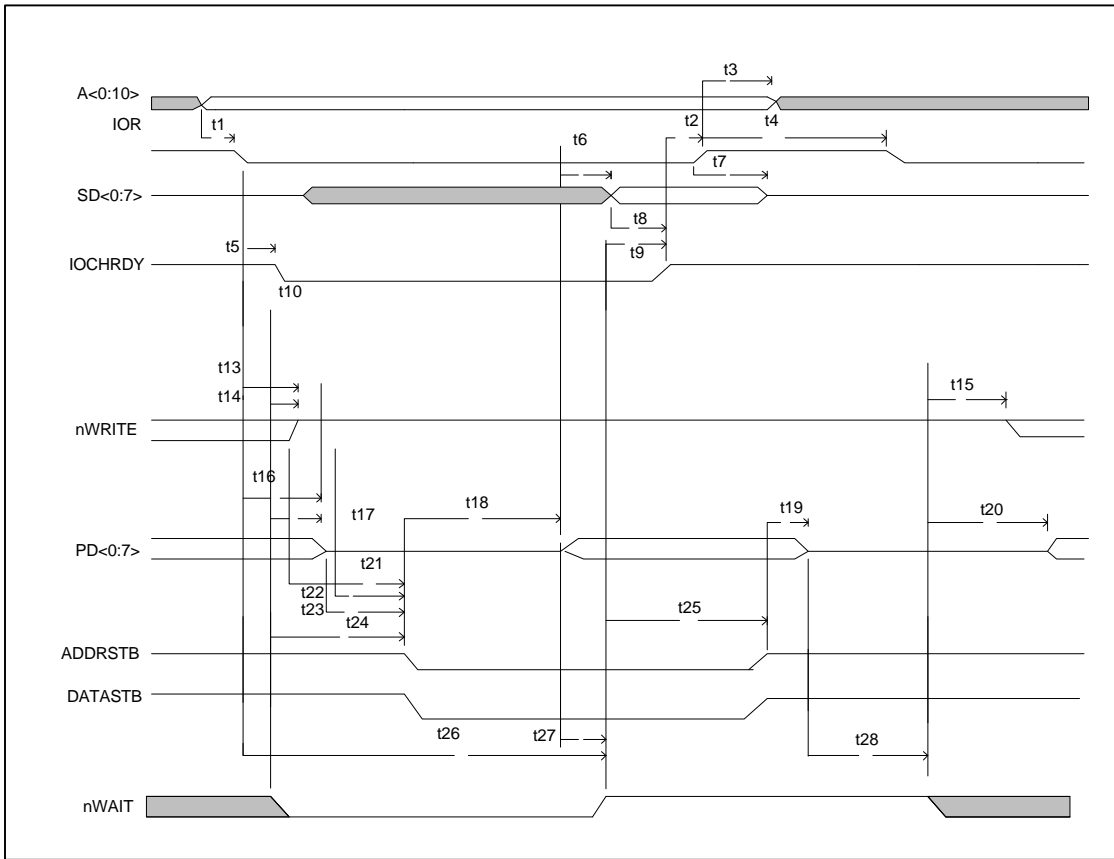
EPP Data or Address Read Cycle (EPP Version 1.9)



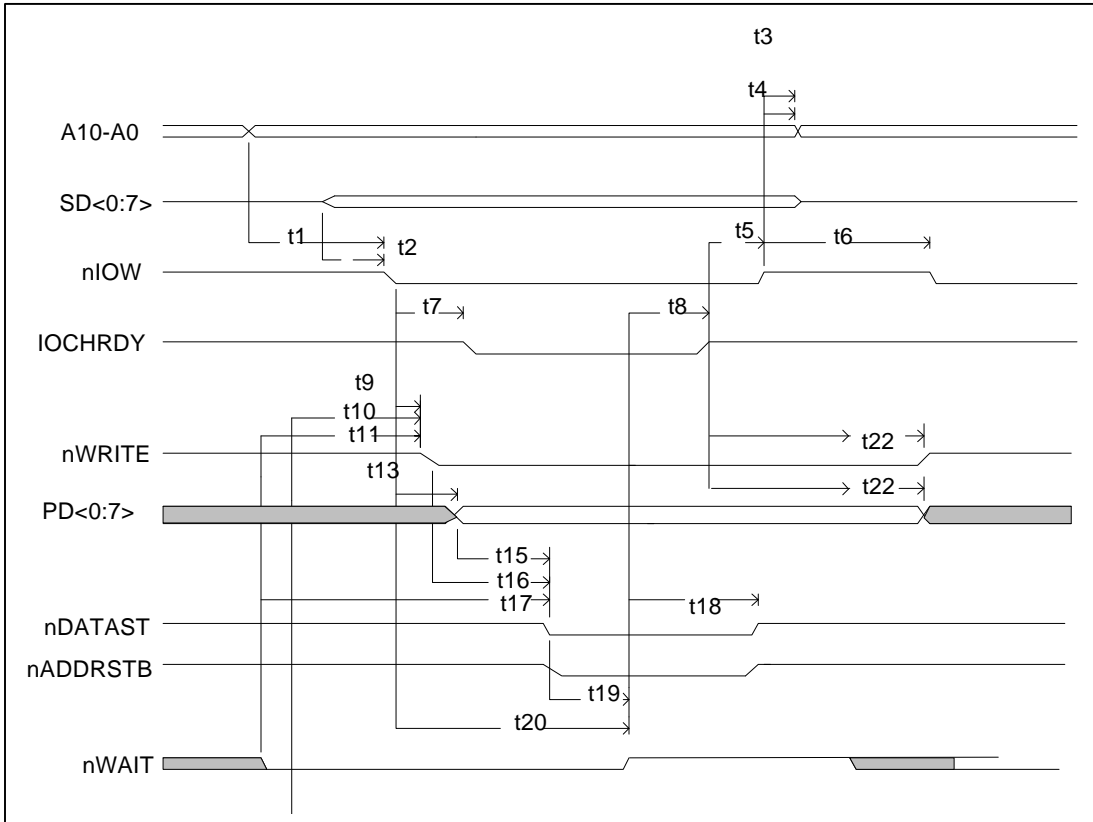
EPP Data or Address Write Cycle (EPP Version 1.9)



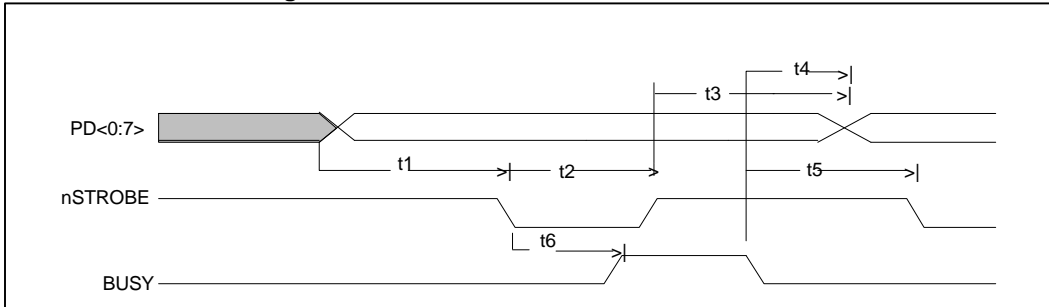
EPP Data or Address Read Cycle (EPP Version 1.7)



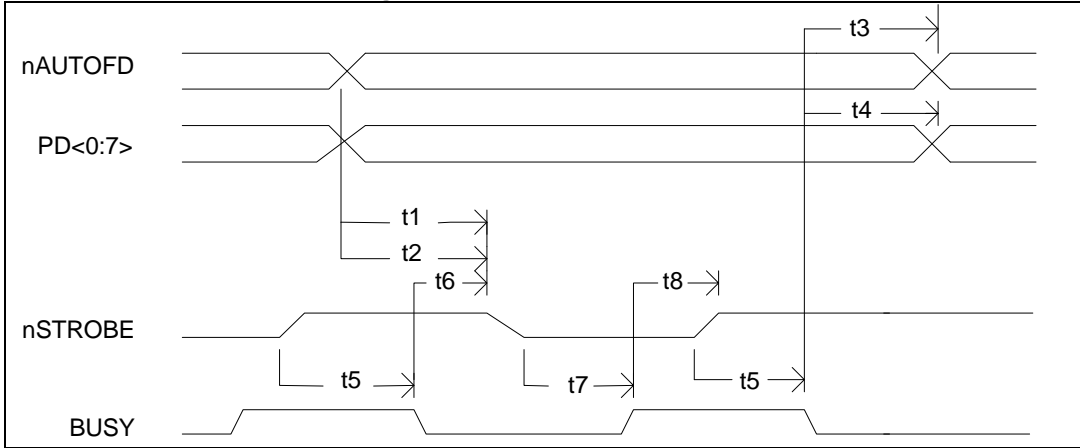
EPP Data or Address Write Cycle (EPP Version 1.7)



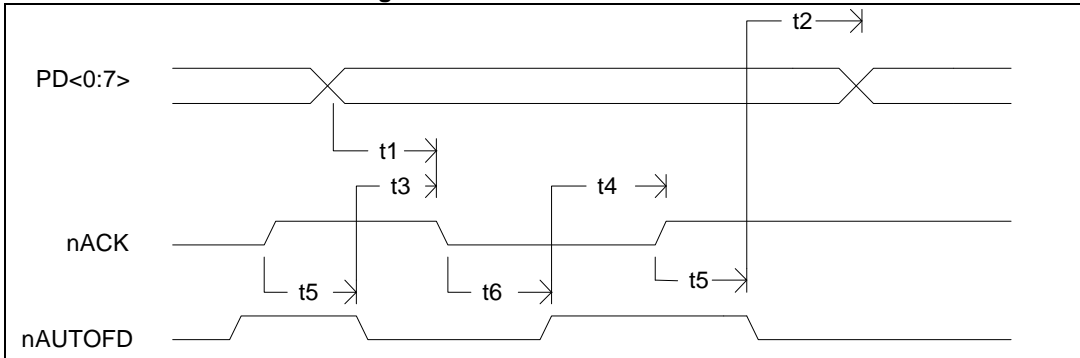
Parallel Port FIFO Timing



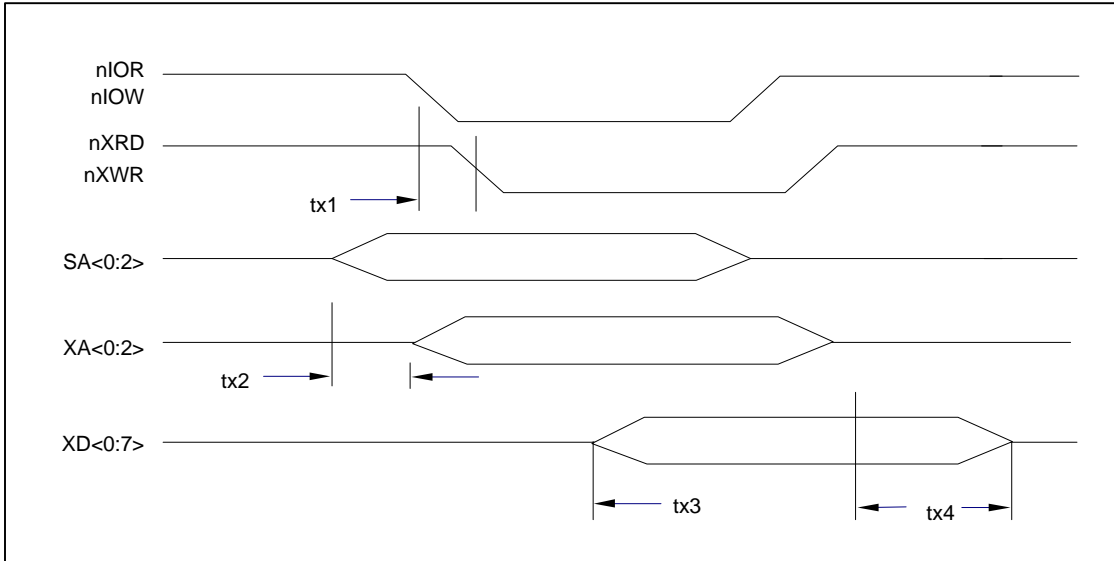
ECP Parallel Port Forward Timing



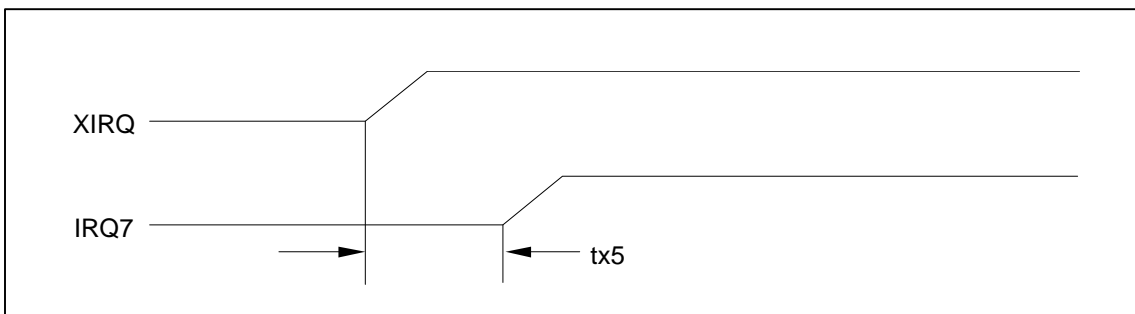
ECP Parallel Port Reverse Timing



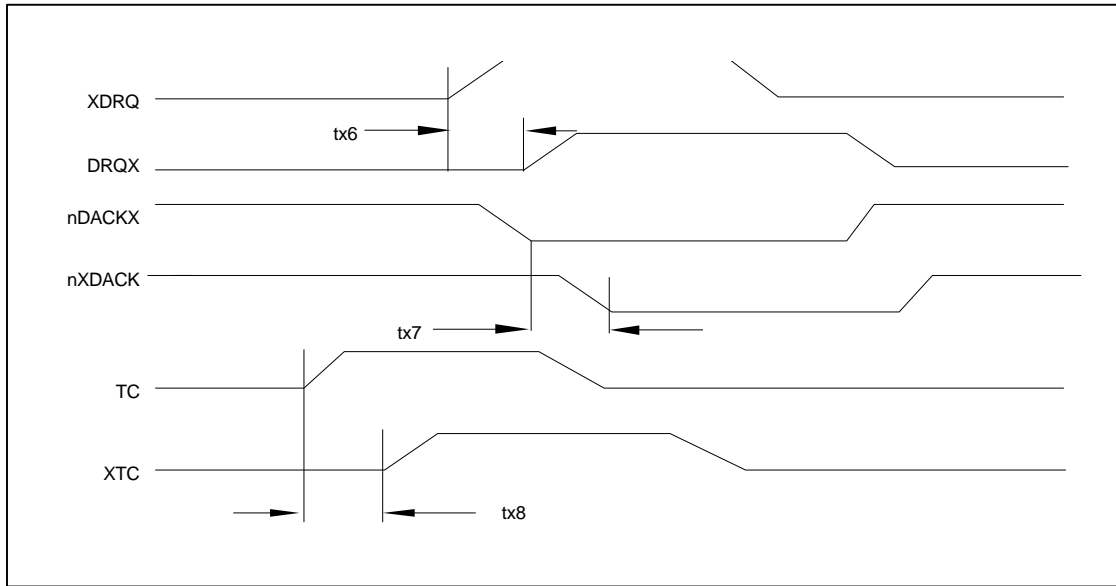
Extension Adapter Mode Command Cycle



Extension Adapter Mode Interrupt Cycle

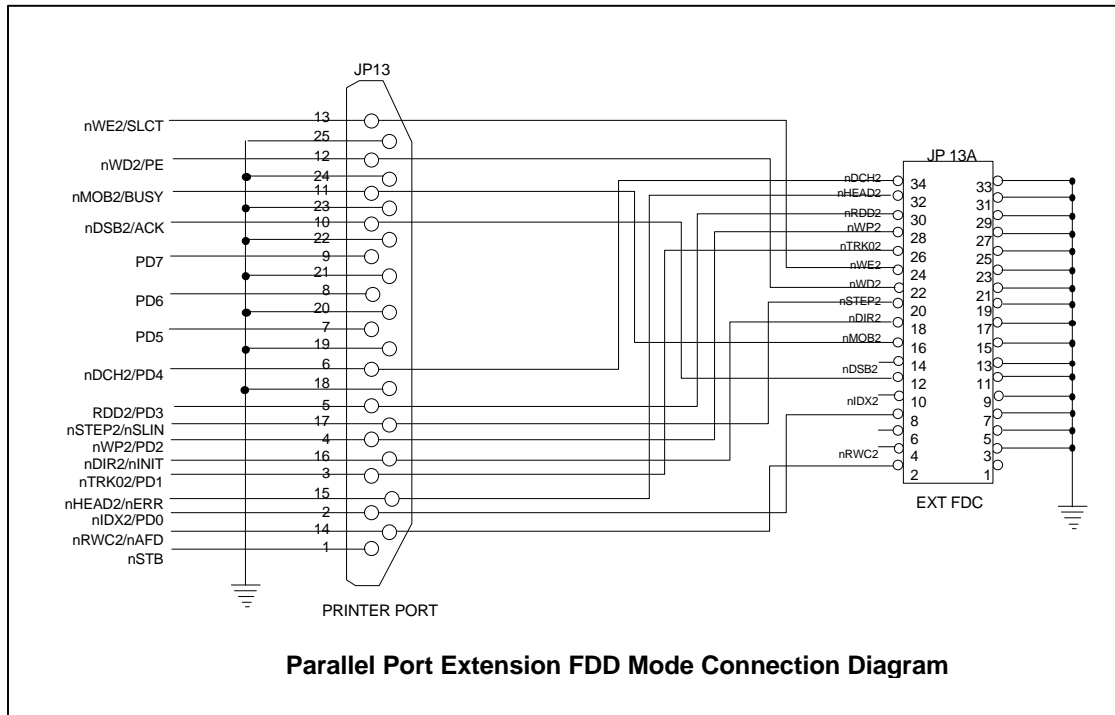


Extension Adapter Mode DMA Cycle

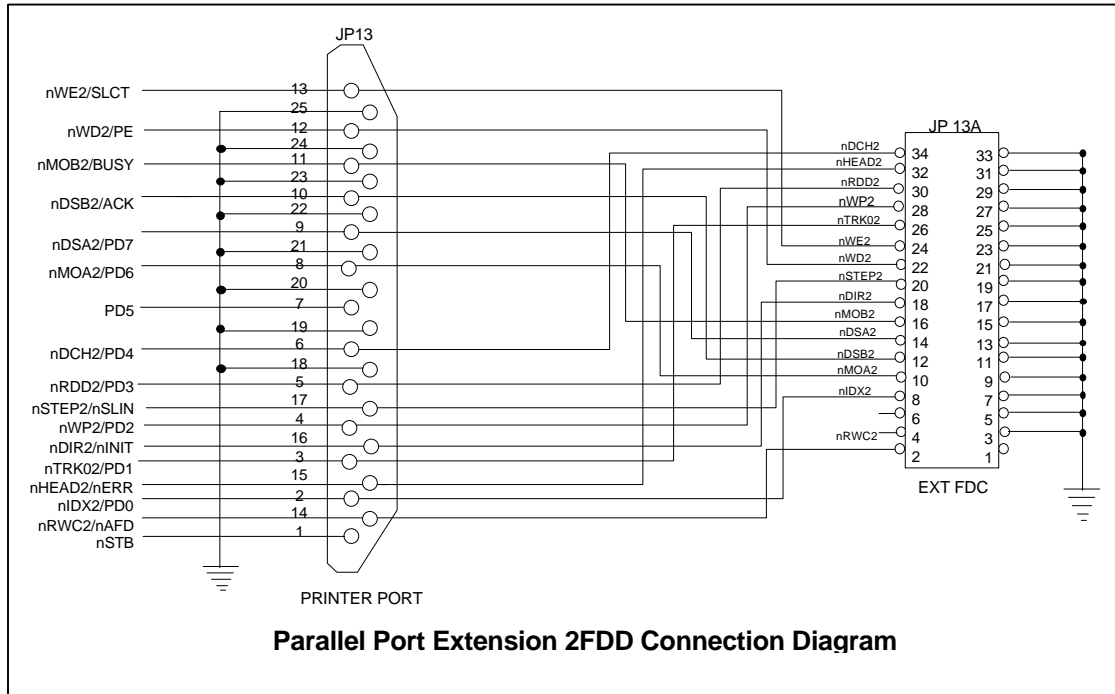


APPLICATION CIRCUITS

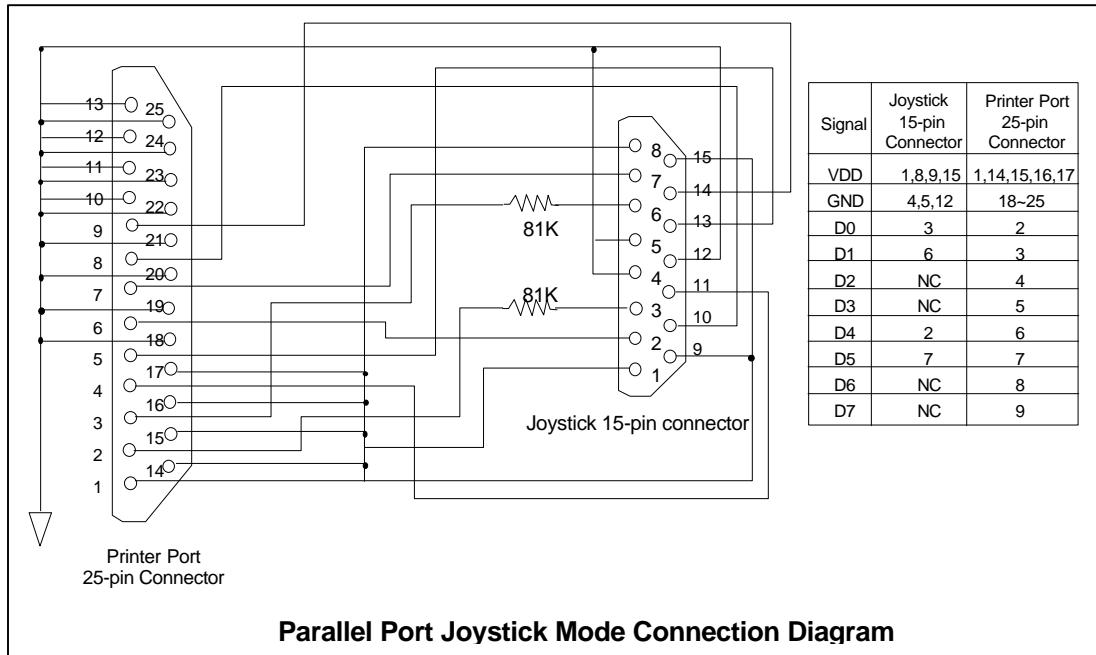
Parallel Port Extension FDD



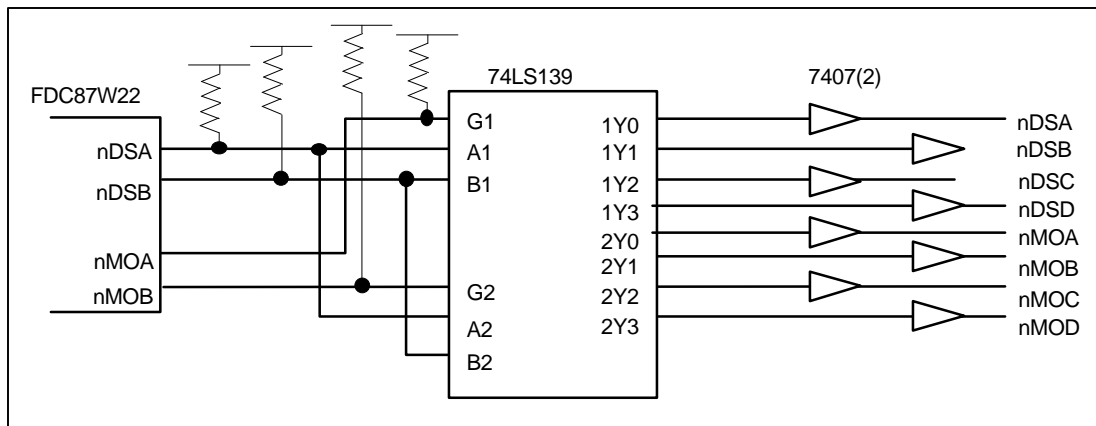
Parallel Port Extension 2FDD



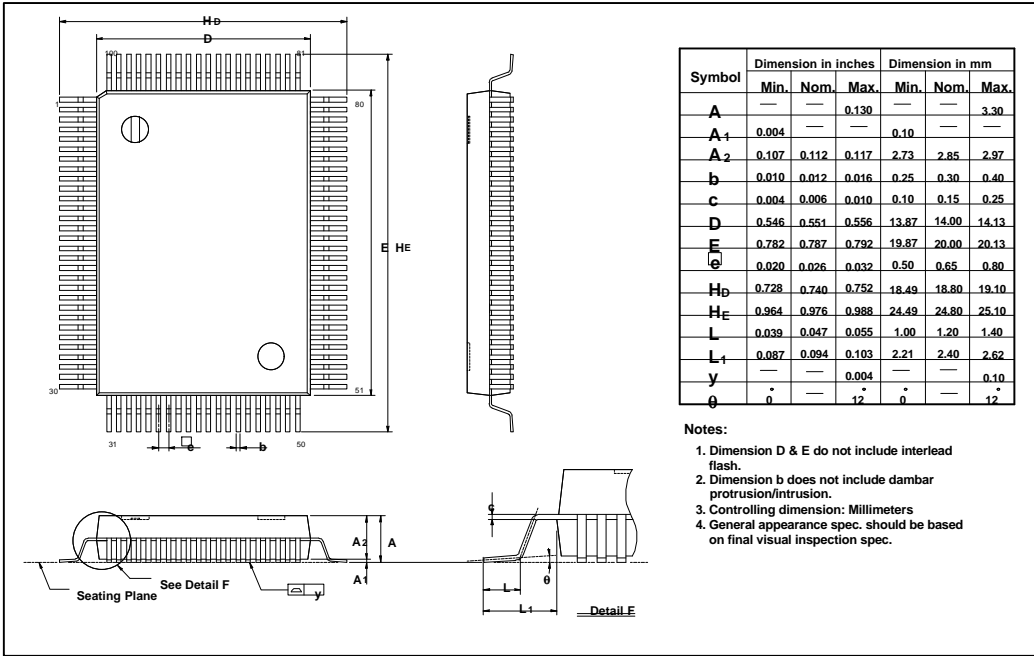
Parallel Port Joystick Mode



Four FDD Mode



**PACKAGE DIMENSIONS
(100 Pin QFP)**



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