EMC1428

1°C Multiple Temperature Sensor with HW Thermal Shutdown & Hottest of Thermal Zones

PRODUCT FEATURES

Datasheet

General Description

The EMC1428 is a high accuracy, low cost, System Management Bus (SMBus) temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to CPU diodes requiring the BJT or transistor model) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

Additionally, the EMC1428 provides a hardware programmable system shutdown feature that is programmed at part power-up via a single TRIP_SET voltage channel that cannot be masked or corrupted through the SMBus.

Each device provides ±1° accuracy for external diode temperatures and ±2°C accuracy for the internal diode temperature. The EMC1428 monitors up to eight temperature channels (up to seven external and one internal).

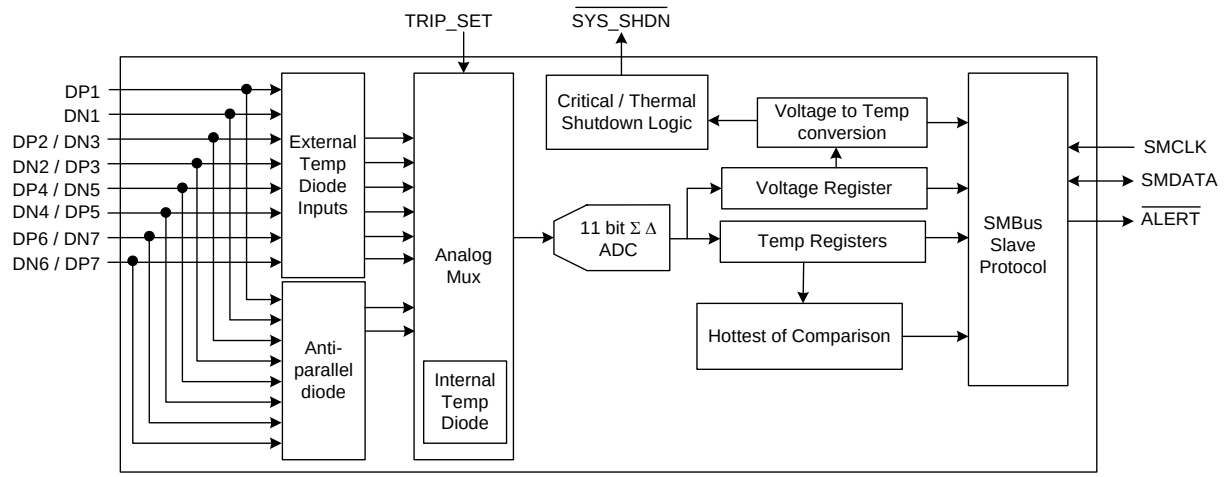
Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded Applications

Features

- Hardware Thermal Shutdown
  - triggers dedicated $\overline{\text{SYS\_SHDN}}$ pin
  - hardware configured range 65°C to 127°C in 1°C steps
  - cannot be disabled or modified by software
- Designed to support 45nm, 65nm, and 90nm CPU diodes
- Supports diodes requiring the BJT or transistor model
- Resistance Error Correction (up to 100 Ohms)
- Up to seven External Temperature Monitors
  - ±1°C Accuracy (60°C < T_{DIODE} < 100°C)
  - 0.125°C Resolution
  - Supports up to 2.2nF filter capacitor
  - Anti-parallel diodes for extra diode support and compact design
- Internal Temperature Monitor
  - ±2°C accuracy
- 3.3V Supply Voltage
- Available in a 16 pin 4mm x 4mm QFN lead-free RoHS Compliant package
- Programmable temperature limits for $\overline{\text{ALERT}}$

Block Diagram



ORDER NUMBERS:

ORDERING NUMBER	PACKAGE	FEATURES	DIODE MODES SUPPORTED	SMBUS ADDRESS
EMC1428-1-AP	16 pin QFN (Lead-Free RoHS Compliant)	Up to 7 external diodes. “Hottest Of” temperature comparison. Hardware set Critical / Thermal shutdown, ALERT output	Intel CPU and 3904	1001_100(r/w)
EMC1428-6-AP	16 pin QFN (Lead-Free RoHS Compliant)	Up to 7 external diodes. “Hottest Of” temperature comparison. Hardware set Critical / Thermal shutdown, ALERT output	Intel CPU and 3904	1001_101(r/w)

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Chapter 1 Pin Description

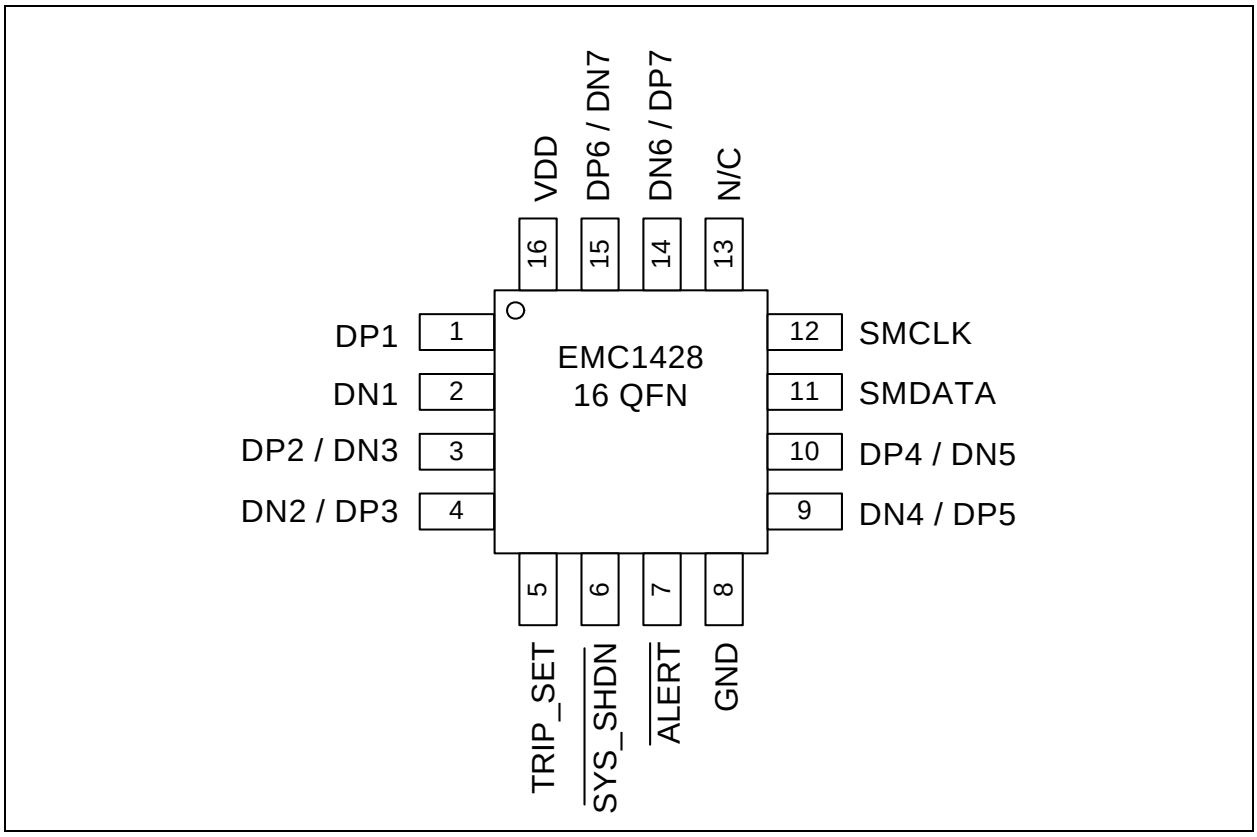

Figure 1.1 EMC1428 Pin Diagram

Table 1.1 EMC1428 Pin Description

PIN NUMBER	NAME	FUNCTION	TYPE
1	DP1	DP1 - External Diode 1 positive (anode) connection.	AIO
2	DN1	External Diode 1 negative (cathode) connection.	AIO
3	DP2 / DN3	External Diode 2 positive (anode) connection and External Diode 3 negative (cathode) connection	AIO
4	DN2 / DP3	External diode 2 negative (cathode) connection and External Diode 3 positive (anode) connection	AIO
5	TRIP_SET	Voltage input to set Critical / Thermal Shutdown temperature	AIO
6	$\overline{\text{SYS\_SHDN}}$	Active low System Shutdown output signal - requires pull-up resistor.	OD (5V)

Table 1.1 EMC1428 Pin Description (continued)

PIN NUMBER	NAME	FUNCTION	TYPE
7	$\overline{\text{ALERT}}$	Active low interrupt - requires pull-up resistor.,	OD (5V)
8	GND	Ground Connection	Power
9	DN4 / DP5	External diode 4 negative (cathode) connection and External Diode 5 positive (anode) connection	AIO
10	DP4 / DN5	External Diode 4 positive (anode) connection and External Diode 5 negative (cathode) connection	AIO
11	SMDATA	SMBus Data input/output	DIOD (5V)
12	SMCLK	SMBus Clock input	DI (5V)
13	N/C	Not used - connect to Ground - see EMC1428 Anomaly Sheet	n/a
14	DN6 / DP7	External diode 6 negative (cathode) connection and External Diode 7 positive (anode) connection	AIO
15	DP6 / DN7	External Diode 6 positive (anode) connection and External Diode 7 negative (cathode) connection	AIO
16	VDD	Power supply	Power

The pin types are described below. All pins labelled (5V) are 5V tolerant:

Table 1.2 Pin Type

PIN TYPE	FUNCTION
Power	Used to supply either VDD or GND to the device
DI	5V tolerant digital input
OD	5V tolerant Open drain digital output. Requires a pull-up resistor
DIOD	5V tolerant bi-directional digital input / open-drain output. Requires a pull-up resistor.
AIO	Analog input / output used for external diodes or analog inputs

Chapter 2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.3 to 4.0	V
Voltage on 5V Tolerant pins	-0.3 to 5.5	V
Voltage on any other pin to Ground	-0.3 to V_{DD} +0.3	V
Operating Temperature Range	-40 to +125	°C
Storage Temperature Range	-55 to +150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for QFN-16		
Thermal Resistance (θ_{j-a})	40	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

2.2 Electrical Specifications

Table 2.2 Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply Current	I_{DD}		450	600	uA	1 conversion / sec, dynamic averaging disabled
Supply Current	I_{DD}		900	1200	uA	4 conversions / sec, dynamic averaging enabled

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Internal Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	0°C < T_A < 100°C
				±2	°C	-40°C < T_A < 125°C
Temperature Resolution			0.125		°C	
External Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	+40°C < T_{DIODE} < +110°C 0°C < T_A < 110°C
			±0.5	±2	°C	-40°C < T_{DIODE} < 127°C
Temperature Resolution			0.125		°C	
Conversion Time all Channels	t_{CONV}		190		ms	default settings
Capacitive Filter	C_{FILTER}		2.2	2.7	nF	Connected across external diode
Resistance Error Correction	R_{SERIES}			100	Ω	In series with DP and DN lines
TRIP_SET Measurement						
Decoded Temperature Accuracy	T_{SET}			0.5	°C	R_{SET} = 1% resistor (see Note 2.1)
$\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK} = 8mA
Leakage Current	I_{LEAK}			±5	uA	powered or unpowered T_A < 85°C
Power Up Timing						
First conversion ready	t_{CONV_f}			300	ms	Time after power up before all channels updated with valid data
SMBus delay	t_{SMB_d}			15	ms	Delay before SMBus communications should be sent by host

Note 2.1 If a 1% resistor is used for RSET, then it is guaranteed to decode as shown in Table 4.1.

2.3 SMBus Electrical Characteristics

Table 2.3 SMBus Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0		V_{DD}	V	5V Tolerant
Input Low Voltage	V_{IL}	-0.3		0.8	V	5V Tolerant
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Powered or unpowered T_A < 85°C
Hysteresis			420		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current	I_{OL}	8.2		15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns f_{SMB} > 100kHz
Clock/Data Rise time	t_{RISE}			1000	ns	Min = 20+0.1C_{LOAD} ns f_{SMB} ≤ 100kHz
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 3 System Management Bus Interface Protocol

3.1 System Management Bus Interface Protocol

The EMC1428 communicate with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1.

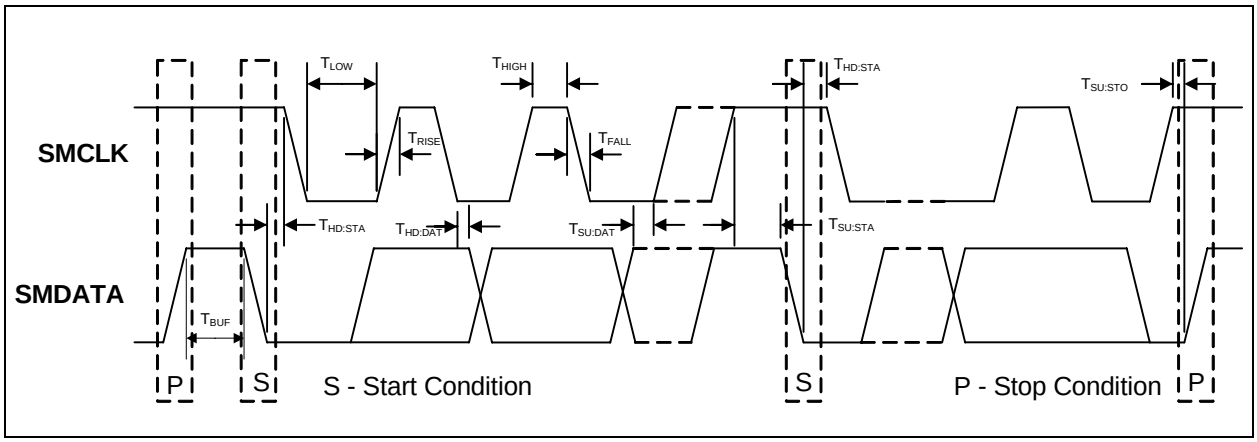

Figure 3.1 SMBus Timing Diagram

The EMC1428 are SMBus 2.0 compatible and support Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 3.1.

Table 3.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST

Attempting to communicate with the EMC1428 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

3.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 3.2:

Table 3.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
0 -> 1	1001_100	0	0	XXh	0	XXh	0	1 -> 0

3.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3.3.

Table 3.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
0-> 1	1001_100	0	0	XXh	0	0 -> 1	1001_100	1	0	XXh	1	1 -> 0

3.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 3.4.

Table 3.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
0 -> 1	1001_100	0	0	XXh	0	1 -> 0

3.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 3.5.

Table 3.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
0 -> 1	1001_100	1	0	XXh	1	1 -> 0

3.6 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 000_1100b. All devices with active interrupts will respond with their client address as shown in Table 3.6.

Table 3.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
0 -> 1	0001_100	1	0	1001_100	1	1 -> 0

The EMC1428 will respond to the ARA in the following way:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

APPLICATION NOTE: The ARA does not clear the Status Register and if the MASK bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

3.7 SMBus Address

The EMC1428-1 devices respond to the 7-bit slave address 1001_100xb.

The EMC1428-6 will respond to the 7-bit slave address 1001_101xb.

Note: Other addresses are available. Contact SMSC for more information.

3.8 SMBus Timeout

The EMC1428 support SMBus Timeout. If the clock line is held low for longer than 30ms, the device will reset its SMBus protocol. This function can be disabled by clearing the TIMEOUT bit in the Conversion Rate Register (see Section 5.5).

Chapter 4 Product Description

The EMC1428 is an SMBus temperature sensor with Hardware Critical / Thermal Shutdown support. The EMC1428 monitors up to seven (7) external diodes and one internal diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1428 and using that data to control the speed of one or more fans.

The EMC1428 device has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when measured temperatures meet or exceed user programmable limits. This allows the EMC1428 to be used as an independent thermal watchdog to warn the host of temperature hot spots without constant monitoring by the host.

The second level of monitoring asserts the $\overline{\text{SYS\_SHDN}}$ pin when the External Diode 1 temperature meets or exceeds a hardware specified threshold temperature. Additionally, any of the external diode channels can be configured to assert the $\overline{\text{SYS\_SHDN}}$ pin when the measured temperature meets or exceeds user programmable limits.

Because the EMC1428 automatically corrects for temperature errors due to series resistance in temperature diode lines, there is greater flexibility in where external diodes are positioned and better measurement accuracy than previously available devices without resistance error correction. As well, the automatic beta detection feature means that there is no need to program the device according to which type of diode is present. Therefore, the device can power up ready to operate for any system configuration including those diodes that require the BJT or transistor model.

Figure 4.1 shows a system level block diagram of the EMC1428.

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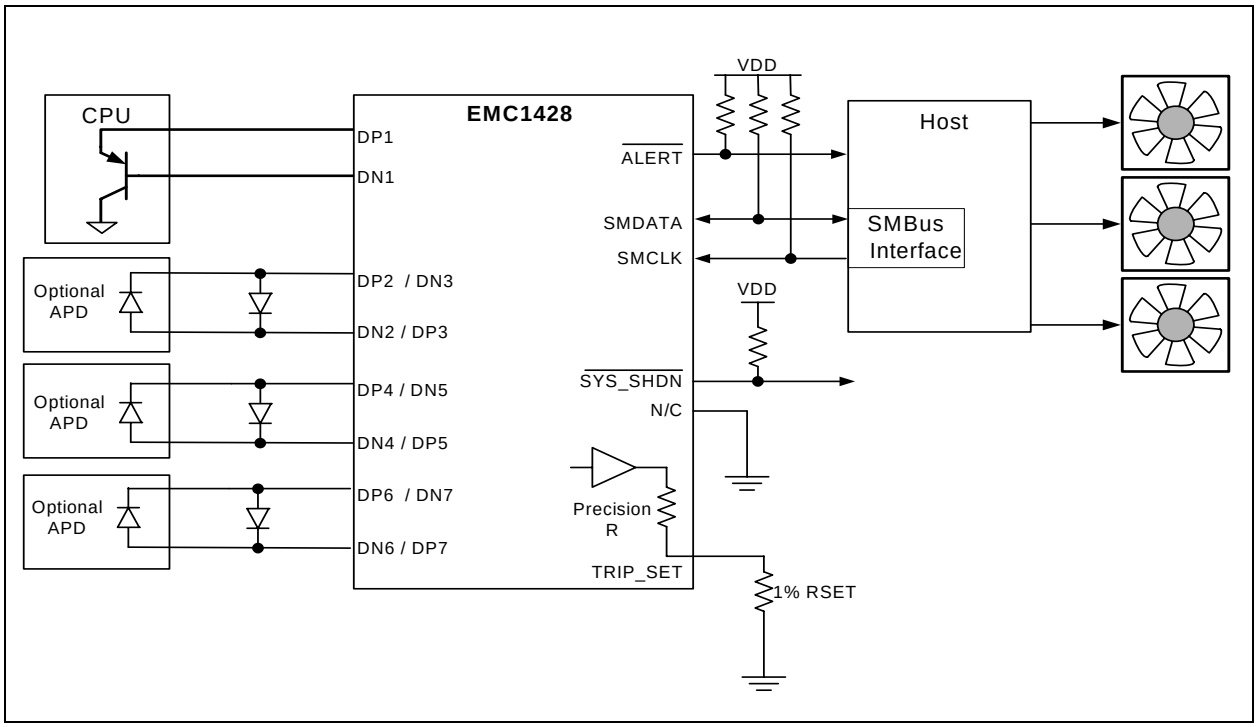


Figure 4.1 System Diagram for EMC1428

4.1 ALERT Output

The ALERT pin is an open drain output and has two modes of operation: interrupt mode and comparator Mode. The mode of the ALERT output is selected via the ALERT / COMP bit in the Configuration Register.

4.1.1 ALERT Pin Interrupt Mode

When configured to operate in interrupt mode, the ALERT pin asserts low when an out of limit measurement (≥ high limit or < low limit) is detected on any diode or when a diode fault is detected. The ALERT pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the ALERT pin will remain asserted until the appropriate status bits are cleared. Each channel is subject to the fault queue (see Section 5.14).

The ALERT pin can be masked by setting the MASK bit. Once the ALERT pin has been masked, it will be de-asserted and remain de-asserted until the MASK bit is cleared by the user. Any interrupt conditions that occur while the ALERT pin is masked will update the Status Register normally.

The ALERT pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more ALERT outputs can be hard-wired together.

4.1.2 ALERT Pin Comparator Mode

When the ALERT pin is configured to operate in comparator mode it will be asserted if any of the measured temperatures meets or exceeds the respective high limit or drops below the respective low limit. The ALERT pin will remain asserted until all temperatures drop below the corresponding high limit minus the THERM Hysteresis value.

When the ALERT pin is asserted in comparator mode, the corresponding status bits will be set. Reading these bits will not clear them until the ALERT pin is deasserted. Once the ALERT pin is deasserted, the status bits will be automatically cleared.

The MASK bit will not block the ALERT pin in this mode, however the individual channel masks (see Section 5.13) will prevent the respective channel from asserting the ALERT pin. In addition, each channel is subject to the fault queue (see Section 5.14).

4.2 SYS_SHDN Output

The SYS_SHDN output is asserted independently of the ALERT output and cannot be masked. If the External Diode 1 temperature exceeds the Hardware Critical / Thermal Shutdown Limit for the programmed number of consecutive measurements, then the SYS_SHDN pin is asserted.

The Hardware Critical / Thermal Shutdown Limit is defined by the TRIP_SET pin as described in Section 4.3.

In addition to External Diode 1 channel triggering the SYS_SHDN pin when the measured temperature exceeds to the Hardware Critical / Thermal Shutdown Limit, each of the temperature measurement channels can be configured to assert the SYS_SHDN pin when they exceed the corresponding THERM Limit.

When the SYS_SHDN pin is asserted, it will not release until the External Diode 1 temperature drops below the Hardware Thermal Shutdown Limit minus 10°C and all other measured temperatures drop below the THERM Limit minus the THERM Hysteresis value (when linked to SYS_SHDN).

The External Diode 1 channel and any software enabled channels are subject to the fault queue such that the error must exceed the threshold for one to four consecutive measurements before the SYS_SHDN pin is asserted.

Figure 4.2 shows a block diagram of the interaction between the input channels and the SYS_SHDN pin.

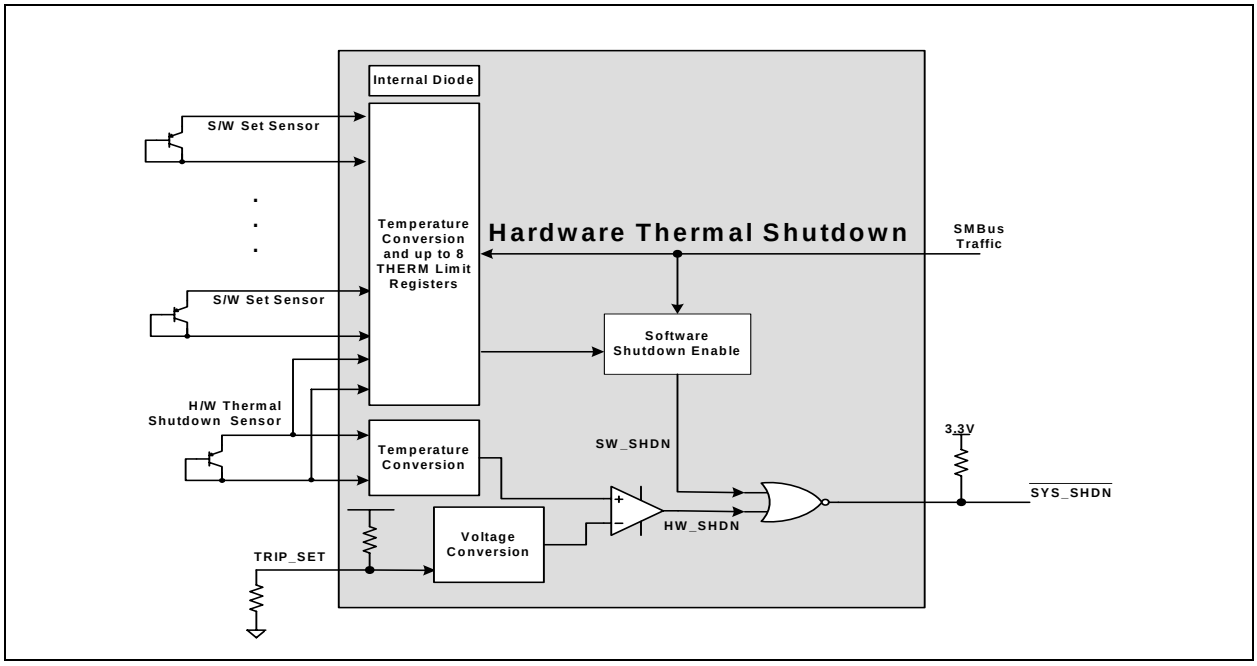


Figure 4.2 Block Diagram of Hardware Thermal Shutdown

4.3 TRIP_SET Pin

The EMC1428's TRIP_SET pin is an input to the Critical / Thermal Shutdown logic block which sets the Critical / Thermal shutdown temperature. The system designer creates a voltage level at this input through a simple resistor connected to GND as shown in Figure 4.3. The value of this resistor is used to create an input voltage on the TRIP_SET pin which is translated into a temperature ranging from 65°C to 127°C as enumerated in Table 4.1.

APPLICATION NOTE: Current only flows when the TRIP_SET pin is being monitored. At all other times, the internal reference voltage is removed and the TRIP_SET pin will be pulled down to ground.

APPLICATION NOTE: The TRIP_SET pin circuitry is designed to use a 1% resistor externally. Using a 1% resistor will result in the Thermal / Critical Shutdown temperature being decoded correctly. If a 5% resistor is used, then the Thermal / Critical Shutdown temperature may be decoded with as much as ±1°C error.

APPLICATION NOTE: Note that an open condition on the TRIP_SET pin will be decoded as a minimum temperature threshold level.

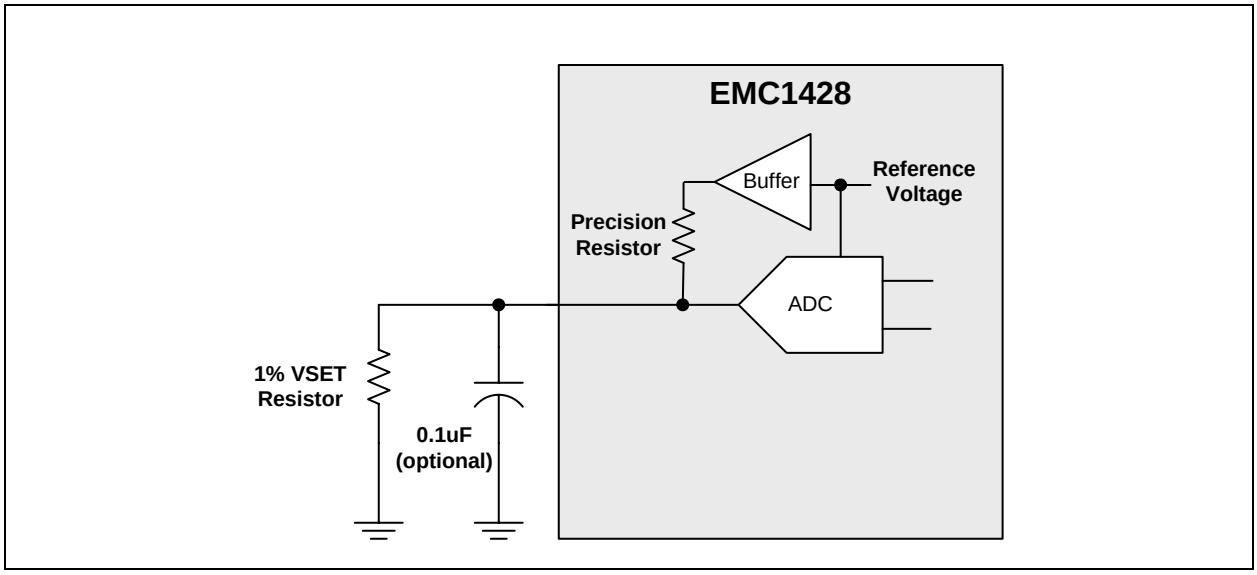


Figure 4.3 Vset Circuit

Table 4.1 V_{TRIP} Resistor Settings

TEMP (°C)	RSET (Ω)	TEMP (°C)	RSET (Ω)
65	0.0	97	1240.0
66	28.7	98	1330.0
67	48.7	99	1400.0
68	69.8	100	1500.0
69	90.9	101	1580.0
70	113.0	102	1690.0
71	137.0	103	1820.0
72	158.0	104	1960.0
73	182.0	105	2050.0
74	210.0	106	2210.0
75	237.0	107	2370.0
76	261.0	108	2550.0
77	294.0	108	2740.0
78	324.0	110	2940.0
79	348.0	111	3160.0
80	383.0	112	3480.0
81	412.0	113	3740.0

Table 4.1 V_{TRIP} Resistor Settings (continued)

TEMP (°C)	RSET (Ω)	TEMP (°C)	RSET (Ω)
82	453.0	114	4120.0
83	487.0	115	4530.0
84	523.0	116	4990.0
85	562.0	117	5490.0
86	604.0	118	6040.0
87	649.0	119	6810.0
88	698.0	120	7870.0
89	750.0	121	9090.0
90	787.0	122	10700.0
91	845.0	123	12700.0
92	909.0	124	15800.0
93	953.0	125	20500.0
94	1020.0	126	29400.0
95	1100.0	127	49900.0
96	1150.0	65	Open

4.4 Consecutive Alerts

The EMC1428 contains multiple consecutive alert counters. One set of counters applies to the $\overline{\text{ALERT}}$ pin and the second set of counters applies to the $\overline{\text{SYS\_SHDN}}$ pin. Each temperature measurement channel has a separate consecutive alert counter for each of the interrupt conditions (High, Low, Diode fault). All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding status bit is set or pin is asserted.

See Section 5.14 for more details on the consecutive alert function.

4.5 Temperature Monitoring

The EMC1428 can monitor the temperature of up to seven (7) externally connected diodes as well as the internal or ambient temperature. Each channel is configured with the following features enabled or disabled based on user settings and system requirements.

4.5.1 Resistance Error Correction

The EMC1428 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of series resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU, and resistance in the printed circuit board traces and package leads. Resistance error correction in the EMC1428 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

4.5.2 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. As well, it is not constant over changes in temperature. The variation in beta causes an error in temperature reading that is proportional to absolute temperature. Compensating for this error is also known as implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC1428 corrects for this beta variation to eliminate any error which would normally be induced. It automatically detects the appropriate beta setting to use.

4.5.3 Digital Averaging

To reduce the effect of noise and temperature spikes on the reported temperature, all of the external diode channels use digital averaging. This averaging acts as a running average using the previous four measured values.

The default setting is to have digital averaging disabled for all channels. It can be enabled for each channel individually by the Filter Control Register (see Section 5.24).

4.5.4 “Hottest Of” Comparison

At the end of every measurement cycle, the EMC1428 compares all of the user selectable External Diode channels to determine which of these channels is reporting the hottest temperature. The hottest temperature is stored in the Hottest Temperature Registers and the appropriate status bit in the Hottest Status Register is set. As an optional feature, the EMC1428 can also flag an event if the hottest temperature channel changes. For example, suppose that External Diode channels 1, 3, and 4 are programmed to be compared in the “Hottest Of” Comparison. If the External Diode 1 channel reports the hottest temperature of the three, its temperature is copied into the Hottest Temperature Registers (in addition to the External Diode 1 Temperature registers) and it is flagged in the Hottest Status bit. If, on the next measurement, the External Diode 3 channel temperature has increased such that it is now the hottest temperature, the EMC1428 can flag this event as an interrupt condition and assert the $\overline{\text{ALERT}}$ pin.

4.5.5 Conversion Rates

The EMC1428 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in Section 5.5. The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 5.7.

4.5.6 Dynamic Averaging

Dynamic averaging causes the EMC1428 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Section 5.5). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 4x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in Table 4.2 for EMC1428.

Table 4.2 Supply Current vs. Conversion Rate for EMC1428

CONVERSION RATE	AVERAGE SUPPLY CURRENT		AVERAGING FACTOR (BASED ON 11-BIT OPERATION)	
	DYNAMIC AVERAGING ENABLED (DEFAULT)	DYNAMIC AVERAGING DISABLED	DYNAMIC AVERAGING ENABLED (DEFAULT)	DYNAMIC AVERAGING DISABLED
1 / sec	715uA	450uA	4x	1x
2 / sec	750uA	550uA	2x	1x
4 / sec (default)	900uA	815uA	1x	1x
Continuous (see Table 5.8)	950uA	950uA	0.5x	0.5x

4.6 Diode Connections

The diode connection for the External Diode 1 channel is determined based on the selected device. For the EMC1428, this channel can support a diode-connected transistor (such as a 2N3904) or a substrate transistor (such as those found in an CPU or GPU) as shown in Figure 4.4. Anti-parallel diodes are not supported on the External Diode 1 channel.

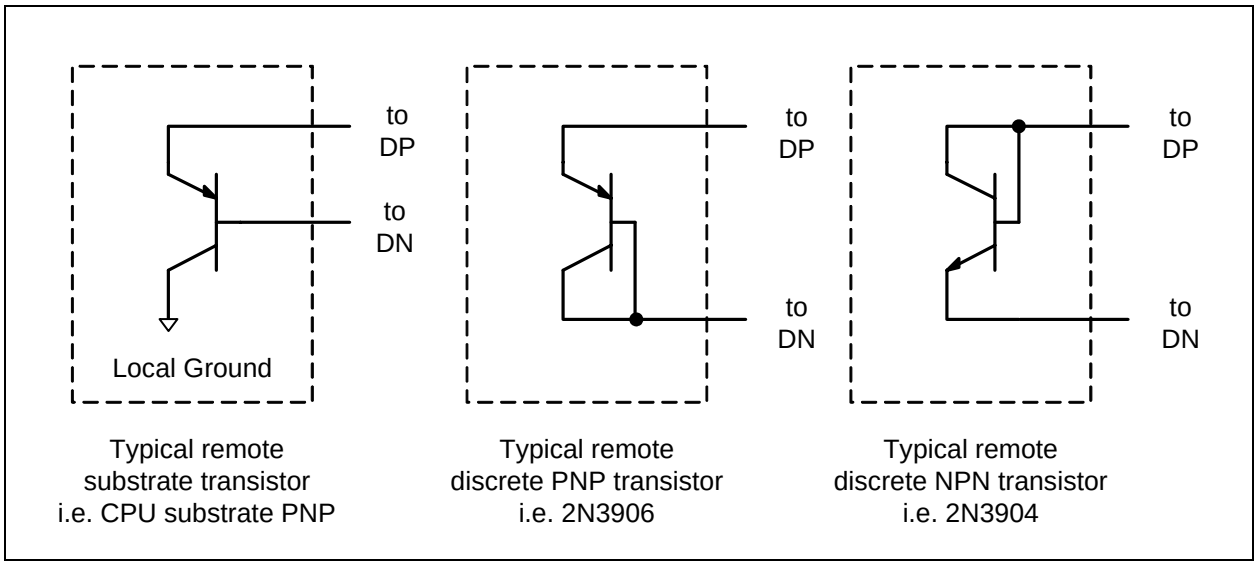


Figure 4.4 Diode Connections

4.6.1 Diode Faults

The EMC1428 actively detects an open and short condition on each measurement channel. When a diode fault is detected, the temperature data MSByte is forced to a value of 80h and the FAULT bit is set in the Status Register. When an external diode channel is configured to operate in APD mode, the circuitry will detect independent open fault conditions, however a short condition will be shared between the APD channels.

Chapter 5 Register Description

The registers shown in Table 5.1 are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 5.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode	00h	Page 27
01h	R	External Diode 1 Data High Byte	Stores the integer data for the External Diode 1	00h	Page 27
02h	R-C	Status	Stores the status bits for the Internal Diode and External Diodes	00h	Page 28
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h)	00h	Page 29
04h	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 0Ah)	06h (4/sec)	Page 29
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh)	55h (85°C)	Page 30
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch)	00h (0°C)	Page 30
07h	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for the External Diode 1 (mirrored at register 0Dh)	55h (85°C)	Page 30
08h	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for the External Diode 1 (mirrored at register 0Eh)	00h (0°C)	Page 30
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h)	00h	Page 29
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 04h)	06h (4/sec)	Page 29
0Bh	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h)	55h (85°C)	Page 30
0Ch	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h)	00h (0°C)	Page 30
0Dh	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for the External Diode 1 (mirrored at register 07h)	55h (85°C)	Page 30

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
0Eh	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for the External Diode 1 (mirrored at register 08h)	00h (0°C)	Page 30
10h	R	External Diode 1 Data Low Byte	Stores the fractional data for the External Diode 1	00h	Page 27
13h	R/W	External Diode 1 High Limit Low Byte	Stores the fractional portion of the high limit for the External Diode 1	00h	Page 30
14h	R/W	External Diode 1 Low Limit Low Byte	Stores the fractional portion of the low limit for the External Diode 1	00h	Page 30
15h	R/W	External Diode 2 High Limit High Byte	Stores the integer portion of the high limit for External Diode 2	55h (85°C)	Page 30
16h	R/W	External Diode 2 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 2	00h (0°C)	Page 30
17h	R/W	External Diode 2 High Limit Low Byte	Stores the fractional portion of the high limit External Diode 2	00h	Page 30
18h	R/W	External Diode 2 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 2	00h	Page 30
19h	R/W	External Diode 1 THERM Limit	Stores the 8-bit critical temperature limit for the External Diode 1	55h (85°C)	Page 33
1Ah	R/W	External Diode 2 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 2	55h (85°C)	Page 33
1Bh	R-C	External Diode Fault	Stores status bits indicating which external diode detected a diode fault	00h	Page 34
1Ch	R	TRIP_SET Voltage	Voltage measured on the TRIP_SET pin to determine the Critical / Thermal shutdown threshold	00h	Page 35
1Dh	R/W	SYS_SHDN Configuration	Controls which software channels, if any, are linked to the SYS_SHDN pin	00h	Page 35
1Eh	R	Hardware Thermal Shutdown Limit	When read, returns the selected Hardware Thermal Shutdown Limit	N/A	Page 36
1Fh	R/W	Interrupt Mask Register	Controls the masking of individual channels	F0h	Page 36
20h	R/W	Internal Diode THERM Limit	Stores the 8-bit critical temperature limit for the Internal Diode	55h (85°C)	Page 33
21h	R/W	THERM Hysteresis	Stores the 8-bit hysteresis value that applies to all THERM limits	0Ah (10°C)	Page 33
22h	R/W	Consecutive ALERT	Controls the number of out-of-limit conditions that must occur before the status bit is asserted	70h	Page 37
23h	R	External Diode 2 Data High Byte	Stores the integer data for External Diode 2	00h	Page 27

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
24h	R	External Diode 2 Data Low Byte	Stores the fractional data for External Diode 2	00h	Page 27
25h	R	External Diode 1 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 1	08h	Page 38
26h	R/W	External Diode 2 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 2	08h	Page 38
29h	R	Internal Diode Data Low Byte	Stores the fractional data for the Internal Diode	00h	Page 27
2Ah	R	External Diode 3 High Byte	Stores the integer data for External Diode 3	00h	Page 27
2Bh	R	External Diode 3 Low Byte	Stores the fractional data for External Diode 3	00h	Page 27
2Ch	R/W	External Diode 3 High Limit High Byte	Stores the integer portion of the high limit for External Diode 3	55h (85°C)	Page 30
2Dh	R/W	External Diode 3 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 3	00h (0°C)	Page 30
2Eh	R/W	External Diode 3 High Limit Low Byte	Stores the fractional portion of the high limit for External Diode 3	00h	Page 30
2Fh	R/W	External Diode 3 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 3	00h	Page 30
30h	R/W	External Diode 3 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 3	55h (85°C)	Page 33
32h	R	Hottest Diode High Byte	Stores the integer data for the hottest temperature	00h	Page 39
33h	R	Hottest Diode Low Byte	Stores the fractional data for the hottest temperature	00h	Page 39
34h	R-C	Hottest Status	Status bits indicating which external diode is hottest	00h	Page 40
35h	R-C	High Limit Status	Status bits for the High Limits	00h	Page 40
36h	R-C	Low Limit Status	Status bits for the Low Limits	00h	Page 41
37h	R	THERM Limit Status	Status bits for the THERM Limits	00h	Page 41
39h	R/W	REC Configuration	Controls REC for all channels	00h	Page 42
3Ah	R/W	Hottest Config	Controls which external diode channels are used in the “hottest of “comparison	00h	Page 42
3Bh	R/W	Channel Config	Controls which channels are enabled	00h	Page 43
40h	R/W	Filter Control	Controls the digital filter setting for the External Diode 1 channel	00h	Page 44

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
41h	R	External Diode 4 Data High Byte	Stores the integer data for the External Diode 4 channel	00h	Page 27
42h	R	External Diode 4 Data Low Byte	Stores the fractional data for the External Diode 4 channel	00h	Page 27
43h	R	External Diode 5 Data High Byte	Stores the integer data for the External Diode 5 channel	00h	Page 27
44h	R	External Diode 5 Data Low Byte	Stores the fractional data for the External Diode 5 channel	00h	Page 27
45h	R	External Diode 6 Data High Byte	Stores the integer data for the External Diode 6 channel	00h	Page 27
46h	R	External Diode 6 Data Low Byte	Stores the fractional data for the External Diode 6 channel	00h	Page 27
47h	R	External Diode 7 Data High Byte	Stores the integer data for the External Diode 7 channel	00h	Page 27
48h	R	External Diode 7 Data Low Byte	Stores the fractional data for the External Diode 7 channel	00h	Page 27
50h	R/W	External Diode 4 High Limit High Byte	Stores the integer data for the high limit for the External Diode 4 channel	55h (85°C)	Page 30
51h	R/W	External Diode 4 Low Limit High Byte	Stores the integer data for the low limit for the External Diode 4 channel	00h (0°C)	Page 30
52h	R/W	External Diode 4 HIgh Limit Low Byte	Stores the fractional data for the low limit for the External Diode 4 channel	00h	Page 30
53h	R/W	External Diode 4 Low Limit Low Byte	Stores the fractional data for the low limit for the External Diode 4 channel	00h	Page 30
54h	R/W	External Diode 5 High Limit High Byte	Stores the integer data for the high limit for the External Diode 5 channel	55h (85°C)	Page 30
55h	R/W	External Diode 5 Low Limit High Byte	Stores the integer data for the low limit for the External Diode 5 channel	00h (0°C)	Page 30
56h	R/W	External Diode 5 HIgh Limit Low Byte	Stores the fractional data for the low limit for the External Diode 5 channel	00h	Page 30
57h	R/W	External Diode 5 Low Limit Low Byte	Stores the fractional data for the low limit for the External Diode 5 channel	00h	Page 30
58h	R/W	External Diode 6 High Limit High Byte	Stores the integer data for the high limit for the External Diode 6 channel	55h (85°C)	Page 30

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
59h	R/W	External Diode 6 Low Limit High Byte	Stores the integer data for the low limit for the External Diode 6 channel	00h (0°C)	Page 30
5Ah	R/W	External Diode 6 HIgh Limit Low Byte	Stores the fractional data for the low limit for the External Diode 6 channel	00h (0°C)	Page 30
5Bh	R/W	External Diode 6 Low Limit Low Byte	Stores the fractional data for the low limit for the External Diode 6 channel	00h (0°C)	Page 30
5Ch	R/W	External Diode 7 High Limit High Byte	Stores the integer data for the high limit for the External Diode 7 channel	55h (85°C)	Page 30
5Dh	R/W	External Diode 7 Low Limit High Byte	Stores the integer data for the low limit for the External Diode 7 channel	00h (0°C)	Page 30
5Eh	R/W	External Diode 7 HIgh Limit Low Byte	Stores the fractional data for the low limit for the External Diode 7 channel	00h	Page 30
5Fh	R/W	External Diode 7 Low Limit Low Byte	Stores the fractional data for the low limit for the External Diode 7 channel	00h	Page 30
64h	R/W	External Diode 4 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 4	55h (85°C)	Page 30
65h	R/W	External Diode 5 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 5	55h (85°C)	Page 30
66h	R/W	External Diode 6 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 6	55h (85°C)	Page 30
67h	R/W	External Diode 7 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 7	55h (85°C)	Page 30
71h	R/W	External Diode 4 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 4	08h	Page 38
72h	R/W	External Diode 6 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 6	08h	Page 38
FDh	R	Product ID - EMC1428	Stores a fixed value that identifies each product	29h	Page 44
FEh	R	Manufacturer ID	Stores a fixed value that represents SMSC	5Dh	Page 44
FFh	R	Revision	Stores a fixed value that represents the revision number	01h	Page 44

5.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal 'shadow' register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

5.2 Temperature Data Registers

Table 5.2 Temperature Data Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R	Internal Diode High Byte	Sign	64	32	16	8	4	2	1	00h
29h	R	Internal Diode Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
01h	R	External Diode 1 High Byte	Sign	64	32	16	8	4	2	1	00h
10h	R	External Diode 1 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
23h	R	External Diode 2 High Byte	Sign	64	32	16	8	4	2	1	00h
24h	R	External Diode 2 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
2Ah	R	External Diode 3 High Byte	Sign	64	32	16	8	4	2	1	00h
2Bh	R	External Diode 3 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
41h	R	External Diode 4 High Byte	Sign	64	32	16	8	4	2	1	00h
42h	R	External Diode 4 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
43h	R	External Diode 5 High Byte	Sign	64	32	16	8	4	2	1	00h
44h	R	External Diode 5 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
45h	R	External Diode 6 High Byte	Sign	64	32	16	8	4	2	1	00h
46h	R	External Diode 6 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
47h	R	External Diode 7 High Byte	Sign	64	32	16	8	4	2	1	00h
48h	R	External Diode 7 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

All temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits. The data format is standard 2's complement from -64°C to 127.875°C as shown in Table 5.3.

Table 5.3 Temperature Data Format

TEMPERATURE (°C)	BINARY	HEX (AS READ BY REGISTERS)
Diode Fault	1000_0000_000b	80_00h
-64	1100_0000_000b	C0_00h
-63.875	1100_0000_001b	C0_20h
-1	1111_1111_000b	FF_00h
-0.125	1111_1111_111b	FF_E0h
0	0000_0000_000b	00_00h
0.125	0000_0000_001b	00_20h
1	0000_0001_000b	01_00h
63	0011_1111_000b	3F_00h
64	0100_0000_000b	40_00h
127	0111_1111_000b	7F_00h
127.875	0111_1111_111b	7F_E0h

5.3 Status Register

Table 5.4 Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
02h	R	Status	BUSY	HOT TEST	-	HIGH	LOW	FAULT	SW_ SYS	HWSD	00h

The Status Register reports general error conditions. To identify specific channels, refer to Section 5.9, Section 5.18, Section 5.19, and Section 5.20. The individual Status Register bits (except HOTTEST) are cleared when the appropriate High Limit, Low Limit, or THERM Limit register has been read or cleared.

Bit 7 - BUSY - This bit indicates that the ADC is currently converting. This bit does not cause the ALERT pin to be asserted.

Bit 6 - HOTTEST - This bit is set if the REM_HOT bit (see Section 5.23) is set and the hottest channel changes. This bit is cleared when the register is read.

Bit 4 - HIGH - This bit is set when any of the temperature channels meets or exceeds its programmed high limit. See the High Limit Status Register for specific channel information (Section 5.18). When set, this bit will assert the ALERT pin.

Bit 3 - LOW - This bit is set when any of the temperature channels drops below its programmed low limit. See the Low Limit Status Register for specific channel information (Section 5.19). When set, this bit will assert the ALERT pin.

Bit 2 - FAULT - This bit is asserted when a diode fault is detected on any of the external diode channels. See the External Diode Fault Register for specific channel information (Section 5.9). When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 1 - SW_SYS - This bit is set when any of the external diode channels meet or exceed the respected THERM Limits. See the Therm Status Register for specific channel information (Section 5.20)

Bit 0 - HWSD - This bit is set when the External Diode 1 Temperature meets or exceeds the Hardware Critical / Thermal Shutdown Limit. When set, this bit will assert the $\overline{\text{SYS\_SHDN}}$ pin. This bit is cleared when read if the $\overline{\text{SYS\_SHDN}}$ pin has been released.

5.4 Configuration Register

Table 5.5 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
03h	R/W	Config	MASK_ ALL	-	ALERT /COMP	-	-	-	DAVG_ DIS	-	00h
09h											

The Configuration Register controls the basic operation of the device. This register is fully accessible at either address.

Bit 7 - MASK_ALL - Masks the $\overline{\text{ALERT}}$ pin from asserting.

- '0' (default) - The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set the $\overline{\text{ALERT}}$ pin will be asserted.
- '1' - The $\overline{\text{ALERT}}$ pin is masked. It will not be asserted for any interrupt condition. The Status Registers will be updated normally.

Bit 5 - ALERT/COMP - Controls the operation of the $\overline{\text{ALERT}}$ pin.

- '0' (default) - The $\overline{\text{ALERT}}$ pin acts as described in Section 4.1.1.
- '1' - The $\overline{\text{ALERT}}$ pin acts in comparator mode as described in Section 4.1.2. In this mode the MASK_ALL bit is ignored.

Bit 1 - DAVG_DIS - Disables the dynamic averaging feature on all temperature channels (see Section 4.5.6).

- '0' (default) - The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in Table 4.2.
- '1' - The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates (i.e. more conversions per second), this averaging factor will be reduced as shown in Table 4.2.

5.5 Conversion Rate Register

Table 5.6 Conversion Rate Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
04h	R/W	Conversion Rate	-	-	-	-		CONV[2:0]			06h (4/sec)
0Ah											

The Conversion Rate Register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

Bits 3-0 - CONV[3:0] - Determines the conversion rate as shown in Table 5.7.

Table 5.7 Conversion Rate

CONV[2:0]			CONVERSIONS / SECOND
2	**1**	**0**	
1	0	0	1
1	0	1	2
1	1	0	4 (default)
1	1	1	Continuous
All Others			4

The actual conversion rate for Continuous conversions will depend on the number of diode channels enabled and is shown in Table 5.8.

Table 5.8 Maximum Conversion Rate Per Temperature Channels

NUMBER OF EXTERNAL DIODE CHANNELS	MAX CONVERSION RATE
4	12 / sec
5	11 / sec
6	10 / sec
7	9 / sec

5.6 Limit Registers

Table 5.9 Temperature Limit Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
05h	R/W	Internal Diode High Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
0Bh											
06h	R/W	Internal Diode Low Limit	Sign	64	32	16	8	4	2	1	00h (0°C)
0Ch											
07h	R/W	External Diode 1 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
0Dh											

Table 5.9 Temperature Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
13h	R/W	External Diode 1 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
08h 0Eh	R/W	External Diode 1 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
14h	R/W	External Diode 1 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
15h	R/W	External Diode 2 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
16h	R/W	External Diode 2 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
17h	R/W	External Diode 2 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
18h	R/W	External Diode 2 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
2Ch	R/W	External Diode 3 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
2Dh	R/W	External Diode 3 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
2Eh	R/W	External Diode 3 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
2Fh	R/W	External Diode 3 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
50h	R/W	External Diode 4 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)

Table 5.9 Temperature Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
51h	R/W	External Diode 4 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
52h	R/W	External Diode 4 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
53h	R/W	External Diode 4 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
54h	R/W	External Diode 5 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
55h	R/W	External Diode 5 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
56h	R/W	External Diode 5 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
57h	R/W	External Diode 5 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
58h	R/W	External Diode 6 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
59h	R/W	External Diode 6 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
5Ah	R/W	External Diode 6 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
5Bh	R/W	External Diode 6 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
5Ch	R/W	External Diode 7 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)

Table 5.9 Temperature Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
5Dh	R/W	External Diode 7 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
5Eh	R/W	External Diode 7 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
5Fh	R/W	External Diode 7 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

The device contains both high and low limits for all temperature channels. If the measured temperature meets or exceeds the high limit, then the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted. Likewise, if the measured temperature is less than the low limit, the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted.

The limit registers with multiple addresses are fully accessible at either address.

5.7 Therm Hysteresis Register

Table 5.10 Therm Hysteresis Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
21h	R/W	THERM Hysteresis	-	64	32	16	8	4	2	1	0Ah (10°C)

The THERM Hysteresis is used in conjunction with the THERM Limit Registers to assert the $\overline{\text{SYS\_SHDN}}$ pin. In addition, the THERM Hysteresis Register is used with the High Limit Registers when the ALERT pin is configured to act as a comparator (see Section 4.1.2).

5.8 Therm Limit Registers

Table 5.11 Therm Limit Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
19h	R/W	External Diode 1 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
1Ah	R/W	External Diode 2 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
20h	R/W	Internal Diode THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)

Table 5.11 Therm Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
30h	R/W	External Diode 3 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
64h	R/W	External Diode 4 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
65h	R/W	External Diode 5 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
66h	R/W	External Diode 6 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
67h	R/W	External Diode 7 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)

The THERM Limit Registers are used to set the threshold for the software inputs to the Critical / Thermal Shutdown circuitry. If the measured channel is linked to the Critical / Thermal Shutdown circuitry and meets or exceeds this limit, then the $\overline{\text{SYS\_SHDN}}$ pin will be asserted.

5.9 External Diode Fault Register

Table 5.12 External Diode Fault Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Bh	R-C	External Diode Fault	E7FLT	E6FLT	E5FLT	E4FLT	E3FLT	E2FLT	E1FLT	-	00h

The External Diode Fault Register indicates which of the external diodes caused the FAULT bit in the Status Register to be set. These bits are cleared when read if the error condition has been removed.

Bit 7 - E7FLT - This bit is set if the External Diode 7 channel reported a diode fault.

Bit 6 - E6FLT - This bit is set if the External Diode 6 channel reported a diode fault.

Bit 5 - E5FLT - This bit is set if the External Diode 5 channel reported a diode fault.

Bit 4 - E4FLT - This bit is set if the External Diode 4 channel reported a diode fault.

Bit 3 - E3FLT - This bit is set if the External Diode 3 channel reported a diode fault.

Bit 2 - E2FLT - This bit is set if the External Diode 2 channel reported a diode fault.

Bit 1 - E1FLT - This bit is set if the External Diode 1 channel reported a diode fault.

5.10 TRIP_SET Reading Register

Table 5.13 TRIP_SET Reading Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Ch	R	TRIP_SET Reading	752.9	376.5	188.2	94.12	47.1	23.53	11.76	5.88	00h

The TRIP_SET Reading Register stores the voltage measured on the TRIP_SET pin. The bit weighting represents mV above 0V.

5.11 Software Thermal Shutdown Configuration Register

Table 5.14 Software Thermal Shutdown Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Dh	R/W	Software Thermal Shutdown Configuration	E7 SYS	E6 SYS	E5 SYS	E4 SYS	E3 SYS	E2 SYS	E1 SYS	INT SYS	00h

The Software Thermal Shutdown Configuration Register controls whether any of the software channels will assert the $\overline{\text{SYS\_SHDN}}$ pin. If a channel is enabled, the temperature is compared against the corresponding THERM Limit. If the measured temperature meets or exceeds the THERM Limit, then the $\overline{\text{SYS\_SHDN}}$ pin is asserted. This functionality is in addition to the Hardware Shutdown circuitry.

Bits 7-1 - ExSYS - configures the External Diode X channel to assert the $\overline{\text{SYS\_SHDN}}$ pin based on it's respective THERM Limit (see Section 5.20 for details on the ExTHERM status bits).

- '0' (default) - the External Diode X channel is not linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature meets or exceeds it's THERM Limit, the ExTHERM status bit is set but the $\overline{\text{SYS\_SHDN}}$ pin is not asserted.
- '1' - the External Diode X channel is linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature meets or exceeds it's THERM Limit, the ExTHERM status bit is set and the $\overline{\text{SYS\_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below it's THERM Limit minus the THERM Hysteresis.

Bit 0 - INTSYS - configures the Internal Diode channel to assert the $\overline{\text{SYS\_SHDN}}$ pin based on it's respective THERM Limit (see Section 5.20 for details on the ITHERM status bit).

- '0' (default) - the Internal Diode channel is not linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature meets or exceeds it's THERM Limit, the ITHERM status bit is set but the $\overline{\text{SYS\_SHDN}}$ pin is not asserted.
- '1' - the Internal Diode channel is linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature meets or exceeds it's THERM Limit, the ITHERM status bit is set and the $\overline{\text{SYS\_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below it's THERM Limit minus the THERM Hysteresis.

5.12 Hardware Critical / Thermal Shutdown Limit Register

Table 5.15 Hardware Thermal Shutdown Limit Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Eh	R	Hardware Thermal Shutdown Limit	-	64	32	16	8	4	2	1	N/A

This read only register returns the Hardware Thermal Shutdown Limit selected by the TRIP_SET voltage. The data represents the hardware set temperature in °C. See Table 5.2 for the data format.

When the External Diode 1 Temperature meets or exceeds this limit, the $\overline{\text{SYS\_SHDN}}$ pin is asserted and will remain asserted until the External Diode 1 Temperature drops below this limit minus 10°C.

5.13 Channel Interrupt Mask Register

Table 5.16 Channel Interrupt Mask Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Fh	R/W	Channel Mask	E7_ MSK	E6_ MSK	E5_ MSK	E4_ MSK	E3_ MSK	E2_ MSK	E1_ MSK	INT_ MSK	F0h

The Channel Interrupt Mask Register controls individual channel masking. When a channel is masked, the $\overline{\text{ALERT}}$ pin will not be asserted when the masked channel reads a diode fault or out of limit error. The channel mask does not mask the $\overline{\text{SYS\_SHDN}}$ pin.

Bits 7-4 - Ex_MSK - Prevents the $\overline{\text{ALERT}}$ pin from being asserted when the External Diode X channel is out of limit or reports a diode fault. If the EXT6_APD bit is not set (see Section 5.23), then the EXT7_MSK bit is ignored. Likewise, if the EXT4_APD bit is not set, then the EXT5_MSK bit is ignored.

- '0' - The External Diode X channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.
- '1' (default) - The External Diode X channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

Bits 3-1- Ex_MSK - Prevents the $\overline{\text{ALERT}}$ pin from being asserted when the External Diode X channel is out of limit or reports a diode fault. If the EXT2_APD bit is not set (see Section 5.23), then the EXT3_MSK bit is ignored.

- '0' - (default) The External Diode X channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.
- '1' - The External Diode X channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

Bit 0 - INT_MSK- Prevents the $\overline{\text{ALERT}}$ pin from being asserted when the Internal Diode temperature is out of limit.

- '0' (default) - The Internal Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit.
- '1' - The Internal Diode channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit.

5.14 Consecutive ALERT Register

Table 5.17 Consecutive ALERT Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
22h	R/W	Consecutive ALERT	TIME OUT	CTHERM2	CTHERM1	CTHERM0	CALRT2	CALRT1	CALRT0	-	70h

The Consecutive ALERT Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the interrupt status registers are asserted.

Each out of limit error and diode fault condition has its own counter associated with it. Each counter is incremented whenever the corresponding channel exceeds the appropriate limit. Additionally, each counter is reset if the condition has been removed. (i.e. if External Diode 1 exceeds its high limit, it will increment the high counter. If, on the next measurement, it experiences a diode fault, the high limit counter will be reset and the diode fault counter will be incremented).

When the ALERT pin is configured as an interrupt and the consecutive alert counter reaches its programmed value then the STATUS bit(s) for that channel and the error condition will be set to '1' and the $\overline{\text{ALERT}}$ pin will be asserted. Measurements will continue normally.

When the $\overline{\text{ALERT}}$ pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature meets or exceeds the High Limit. Additionally, once the consecutive alert counter reaches the programmed limit, the $\overline{\text{ALERT}}$ pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the THERM Hysteresis value.

For example, if the CALRT[2:0] bits are set for 4 consecutive alerts on an EMC1428 device, the high limits are set at 70°C, and none of the channels are masked, then the status bits will be asserted after the following four measurements:

1. Internal Diode reads 71°C and both external diodes read 69°C. Consecutive alert counter for INT is incremented to 1.
2. Both the Internal Diode and the External Diode 1 read 71°C and External Diode 2 reads 68°C. Consecutive alert counter for INT is incremented to 2 and for EXT1 is set to 1.
3. The External Diode 1 reads 71°C and both the Internal Diode and External Diode 2 read 69°C. Consecutive alert counter for INT and EXT2 are cleared and EXT1 is incremented to 2.
4. The Internal Diode reads 71°C and both external diodes read 71°C. Consecutive alert counter for INT is set to 1, EXT2 is set to 1, and EXT1 is incremented to 3.
5. The Internal Diode reads 71°C and both the external diodes read 71°C. Consecutive alert counter for INT is incremented to 2, EXT2 is set to 2, and EXT1 is incremented to 4. The HIGH status bit are set for EXT1 and the $\overline{\text{ALERT}}$ pin is asserted. The EXT1 counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

Bit 7 - TIMEOUT - Determines whether the SMBus Timeout function is enabled.

- '0' (default) - The SMBus Timeout feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol.
- '1' - The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than 30ms, then the device will reset the SMBus protocol.

Bits 6-4 CTHRM[2:0] - Determines the number of consecutive measurements that must exceed the corresponding THERM Limit and Hardware Thermal Shutdown Limit before the $\overline{\text{SYS\_SHDN}}$ pin is asserted. All temperature channels use this value to set the respective counters. The consecutive THERM counter is incremented whenever any of the measurements exceed the corresponding THERM Limit or if the External Diode 1 measurement meets or exceeds the Hardware Thermal Shutdown Limit.

If the temperature drops below the THERM limit or Hardware Thermal Shutdown Limit, then the counter is reset. If the programmed number of consecutive measurements exceed the THERM Limit or Hardware Thermal Shutdown Limit, and the appropriate channel is linked to the SYS_SHDN pin, then the SYS_SHDN pin will be asserted low.

Once the SYS_SHDN pin is asserted, the consecutive THERM counter will not reset until the corresponding temperature drops below the appropriate limit minus the corresponding hysteresis.

The bits are decoded as shown in Table 5.18. The default setting is 4 consecutive out of limit conversions.

Bits 3-1 - CALRT[2:0] - Determine the number of consecutive measurements that must have an out of limit condition or diode fault before the STATUS bits is asserted. All temperature channels use this value to set the respective counters. The bits are decoded as shown in Table 5.18. The default setting is 1 consecutive out of limit conversion.

APPLICATION NOTE: If one of the fault queues is not cleared and the CALRT[2:0] (or CTHRM[2:0]) bits are updated, the update won't take affect until fault queue is cleared. All the fault queues are independent so those that are empty will be updated immediately.

Table 5.18 Consecutive Alert Settings

2	1	0	NUMBER OF CONSECUTIVE OUT OF LIMIT MEASUREMENTS
0	0	0	1 (default for CALRT[2:0])
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHRM[2:0])
All Others			1 (CALRT[2:0]), 4 (CTHRM[2:0])

5.15 Beta Configuration Register

Table 5.19 Beta Configuration Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
25h	R	External Diode 1 Beta Configuration	-	-	-	-	AUTO1	BETA1[2:0]			08h
26h	R/W	External Diode 2 Beta Configuration	-	-	-	-	AUTO2	BETA2[2:0]			08h
71h	R/W	External Diode 4 Beta Configuration	-	-	-	-	AUTO4	BETA4[2:0]			08h
72h	R/W	External Diode 6 Beta Configuration	-	-	-	-	AUTO6	BETA6[2:0]			07h

These registers are used to set the Beta Compensation factor that is used for the External Diode channels.

Bit 3 - AUTOx - Enables the Beta Compensation factor autodetection function.

- '0' - The Beta Compensation Factor autodetection circuitry is disabled. The External Diode will always use the Beta Compensation factor set by the BETAx[2:0] bits.
- '1' (default) - The Beta Compensation factor autodetection circuitry is enabled. At the beginning of every conversion, the optimal Beta Compensation factor setting will be determined and applied. The BETAx[2:0] bits will be automatically updated to indicate the current setting.

Bit 2-0 - BETAx[2:0] - These bits always reflect the current beta configuration settings. These bits will be updated automatically and writing to these bits will have no effect.

Table 5.20 Beta Compensation Look Up Table

BETAX[2:0]			MINIMUM BETA
2	**1**	**0**	
0	0	0	≤ 0.08
0	0	1	≤ 0.111
0	1	0	≤ 0.176
0	1	1	≤ 0.29
1	0	0	≤ 0.48
1	0	1	≤ 0.9
1	1	0	≤ 2.33
1	1	1	Disabled

5.16 Hottest Temperature Registers

Table 5.21 Hottest Temperature Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
32h	R	Hottest Temperature High Byte	Sign	64	32	16	8	4	2	1	80h
33h	R	Hottest Temperature Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

The Hottest Temperature Registers store the measured hottest temperature of all the selected external diode channels (see Section 5.22). If no External diodes are selected then the High Byte Register will read 80h. The data format is the same as the temperature channels.

5.17 Hottest Temperature Status Register

Table 5.22 Hottest Temperature Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
34h	R	Hottest Temperature Status	EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	INT	00h

The Hottest Temperature Status Register flags which external diode temperature is hottest. If multiple temperature channels measure the same temperature and are equal to the hottest temperature, then hottest status will be based on the measurement order.

Bit 7 - EXT7 - The External Diode 7 channel is the hottest.

Bit 6 - EXT6 - The External Diode 6 channel is the hottest.

Bit 4 - EXT5 - The External Diode 5 channel is the hottest.

Bit 3 - EXT4 - The External Diode 4 channel is the hottest.

Bit 3 - EXT3 - The External Diode 3 channel is the hottest.

Bit 2 - EXT2 - The External Diode 2 channel is the hottest.

Bit 1 - EXT1 - The External Diode 1 channel is the hottest.

Bit 0 - INT - The Internal Diode channel is the hottest.

5.18 High Limit Status Register

Table 5.23 High Limit Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
35h	R-C	High Limit Status	E7 HIGH	E6 HIGH	E5 HIGH	E4 HIGH	E3 HIGH	E2 HIGH	E1 HIGH	I HIGH	00h

The High Limit Status Register contains the status bits that are set when a temperature channel high limit is exceeded for a number of consecutive readings as set by the consecutive alert counts (see Section 5.14). If any of these bits are set, then the HIGH status bit in the Status Register is set. Reading from the High Limit Status Register will clear all bits if the error condition has been removed. Reading from the register will also clear the HIGH status bit in the Status Register.

The $\overline{\text{ALERT}}$ pin will be set if any of these status bits are set.

Bit 7 - E7HIGH - This bit is set when the External Diode 7 channel meets or exceeds its programmed high limit.

Bit 6 - E6HIGH - This bit is set when the External Diode 6 channel meets or exceeds its programmed high limit.

Bit 5 - E5HIGH - This bit is set when the External Diode 5 channel meets or exceeds its programmed high limit.

Bit 4 - E4HIGH - This bit is set when the External Diode 4 channel meets or exceeds its programmed high limit.

Bit 3 - E3HIGH - This bit is set when the External Diode 3 channel meets or exceeds its programmed high limit.

Bit 2 - E2HIGH - This bit is set when the External Diode 2 channel meets or exceeds its programmed high limit.

Bit 1 - E1HIGH - This bit is set when the External Diode 1 channel meets or exceeds its programmed high limit.

Bit 0 - IHIGH - This bit is set when the Internal Diode channel meets or exceeds its programmed high limit.

5.19 Low Limit Status Register

Table 5.24 Low Limit Status Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
36h	R-C	Low Limit Status	E7 LOW	E6 LOW	E5 LOW	E4 LOW	E3 LOW	E2 LOW	E1 LOW	ILOW	00h

The Low Limit Status Register contains the status bits that are set when a temperature channel drops below the low limit for a number of consecutive readings as set by the consecutive alert counts (see Section 5.14). If any of these bits are set, then the LOW status bit in the Status Register is set. Reading from the Low Limit Status Register will clear all bits if the error condition has been removed. Reading from the register will also clear the LOW status bit in the Status Register.

The $\overline{\text{ALERT}}$ pin will be set if any of these status bits are set.

Bit 7 - E7LOW - This bit is set when the External Diode 7 channel drops below its programmed low limit.

Bit 6 - E6LOW - This bit is set when the External Diode 6 channel drops below its programmed low limit.

Bit 5- E5LOW - This bit is set when the External Diode 5 channel drops below its programmed low limit.

Bit 4 - E4LOW - This bit is set when the External Diode 4 channel drops below its programmed low limit.

Bit 3 - E3LOW - This bit is set when the External Diode 3 channel drops below its programmed low limit.

Bit 2 - E2LOW - This bit is set when the External Diode 2 channel drops below its programmed low limit.

Bit 1 - E1LOW - This bit is set when the External Diode 1 channel drops below its programmed low limit.

Bit 0 - ILOW - This bit is set when the Internal Diode channel drops below its programmed low limit.

5.20 THERM Limit Status Register

Table 5.25 THERM Limit Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
37h	R-C	THERM Limit Status	E7 THERM	E6 THERM	E5 THERM	E4 THERM	E3 THERM	E2 THERM	E1 THERM	I THERM	00h

The THERM Limit Status Register contains the status bits that are set when a temperature channel THERM Limit is exceeded for a number of consecutive readings as set by the consecutive therm counts (see Section 5.14). If any of these bits are set, then the THERM status bit in the Status Register is set. Reading from the THERM Limit Status Register will not clear the status bits. Once the temperature drops below the THERM Limit minus the THERM Hysteresis, the corresponding status bits will be automatically cleared. The THERM bit in the Status Register will be cleared when all individual channel THERM bits are cleared.

Bit 7 - E7THERM - This bit is set when the External Diode 7 channel meets or exceeds it's programmed THERM Limit.

Bit 6 - E6THERM - This bit is set when the External Diode 6 channel meets or exceeds it's programmed THERM Limit.

Bit 5 - E5THERM - This bit is set when the External Diode 5 channel meets or exceeds it's programmed THERM Limit.

Bit 4 - E4THERM - This bit is set when the External Diode 4 channel meets or exceeds it's programmed THERM Limit.

Bit 3 - E3THERM - This bit is set when the External Diode 3 channel meets or exceeds it's programmed THERM Limit.

Bit 2 - E2THERM - This bit is set when the External Diode 2 channel meets or exceeds it's programmed THERM Limit.

Bit 1 - E1THERM - This bit is set when the External Diode 1 channel meets or exceeds it's programmed THERM limit.

Bit 0- ITHERM - This bit is set when the Internal Diode channel meets or exceeds it's programmed THERM limit.

5.21 REC Configuration Register

Table 5.26 REC Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
39h	R/W	REC Config	E7 REC_n	E6_ REC_n	E5_ REC_n	E4_ REC_n	E3_ REC_n	E2_ REC_n	E1_ REC_n	-	00h

The REC Control Register controls the Resistance Error Correction circuitry for each of the external diode channels.

Bits 7 -0- EX_REC_n - Disables the Resistance Error Correction (REC) for the External Diode X channel.

- '0' (default) - REC is enabled.
- '1' - REC is disabled.

5.22 Hottest Configuration Register

Table 5.27 Hottest Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
3Ah	R/W	Hottest Config	E7HOT	E6HOT	E5HOT	E4HOT	E3HOT	E2HOT	E1HOT	IHOT	00h

The Hottest Configuration Register determines which External Diode Channels (if any) are compared during the “Hottest Of” comparison that is automatically performed at the end of every conversion cycle.

Bits 7 - 0 - ExHOT - Controls whether the External Diode X temperature data is compared during the “Hottest Of” comparison.

- ‘0’ (default) - The External Diode X channel is not compared during the “Hottest Of” Comparison.
- ‘1’ - The External Diode X channel temperature data is compared to all other indicated channels during the “Hottest Of” Comparison.

Bit 0 - IHOT - Controls whether the Internal Diode temperature data is compared during the “Hottest Of” comparison.

- ‘0’ (default) - The Internal Diode channel is not compared during the “Hottest Of” Comparison.
- ‘1’ - The Internal Diode channel temperature data is compared to all other indicated channels during the “Hottest Of” Comparison.

5.23 Channel Configuration Register

Table 5.28 Channel Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
3Bh	R/W	Channel Config	REM_HOT	-	-	-	EXT6_APD	EXT4_APD	EXT2_APD	-	00h

The Channel Configuration Register determines which external diode channels are active in the device.

Bit 7 - REM_HOT - Enables circuitry that will remember the last temperature channel that was determined to be the Hottest and flag an error if the hottest temperature channel changes.

- ‘0’ (default) - The HOTTEST status bit will not be asserted if the hottest temperature channel changes.
- ‘1’ - If the hottest temperature channel changes, then the HOTTEST status bit will be asserted.

Bit 3 - EXT6_APD - Enables the DP6 / DN7 and DN6 / DP7 pins to support two anti-parallel diode connections versus a single diode connection.

- ‘0’ (default) - The DP6 / DN7 and DN6 / DP7 pins do not support two anti-parallel diode connections. The pins will only monitor a single external diode (External Diode 6).
- ‘1’ - The DP6 / DN7 and DN6 / DP7 pins support two anti-parallel diode connections (External Diode 6 and External Diode 7).

Bit 2 - EXT4_APD - Enables the DP4 / DN5 and DN4 / DP5 pins to support two anti-parallel diode connections versus a single diode connection.

- ‘0’ (default) - The DP4 / DN5 and DN4 / DP5 pins do not support two anti-parallel diode connections. The pins will only monitor a single external diode (External Diode 4).
- ‘1’ - The DP4 / DN5 and DN4 / DP5 pins support two anti-parallel diode connections (External Diode 4 and External Diode 5).

Bit 1 - EXT2_APD- Enables the DP2 / DN3 and DN2 / DP3 pins to support two anti-parallel diode connections versus a single diode connection.

- ‘0’ (default) - The DP2 / DN3 and DN2 / DP3 pins do not support two anti-parallel diode connections. The pins will only monitor a single external diode (External Diode 2).
- ‘1’ - The DP2 / DN3 and DN2 / DP3 pins support two anti-parallel diode connections (External Diode 2 and External Diode 3).

5.24 Filter Control Register

Table 5.29 Filter Control Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
40h	R/W	Filter Control	AVG 7_EN	AVG6 _EN	AVG5 _EN	AVG4 _EN	AVG 3_EN	AVG2 _EN	AVG 1_EN	-	00h

The Filter Configuration Register controls the digital filter on the external diode channels.

Bits 7 - 0 - AVGx_EN- Control the digital averaging that is applied to the External Diode X temperature measurements.

- '0' (default) - Digital Averaging is disabled.
- '1' - Digital averaging is enabled as a 4x running average for the External Diode X channel.

5.25 Product ID Register

Table 5.30 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID	0	0	1	0	1	0	0	1	29h EMC1428

The Product ID Register holds a unique value that identifies the device.

5.26 Manufacturer ID Register (FEh)

Table 5.31 Manufacturer ID Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	Manufacturer ID	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID Register holds an 8-bit word that identifies SMSC.

5.27 Revision Register (FFh)

Table 5.32 Revision Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	0	0	0	0	0	0	0	1	01h

The Revision register contains an 8 bit word that identifies the die revision.

Chapter 6 Package Information

6.1 EMC1428 Package Drawing

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3		0.20 REF		-	LEAD-FRAME THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D2/E2	2.00	2.10	2.20	2	X/Y EXPOSED PAD SIZE
L	0.45	0.50	0.55	-	TERMINAL LENGTH
b	0.25	0.30	0.35	2	TERMINAL WIDTH
K	0.20	-	-	-	TERMINAL TO PAD DISTANCE
e		0.65 BSC		-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 6.1 16 pin QFN 4mm x 4mm Package Dimensions

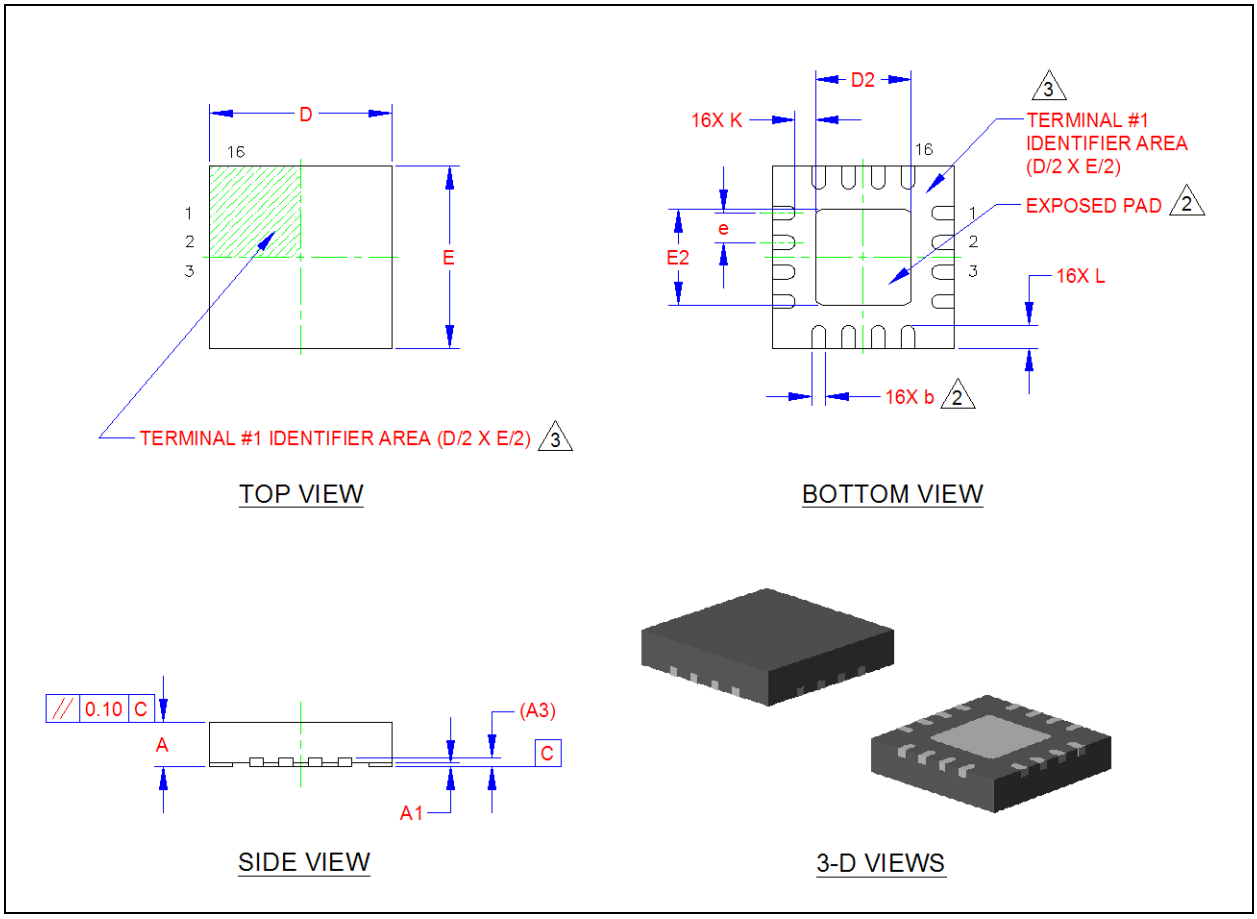
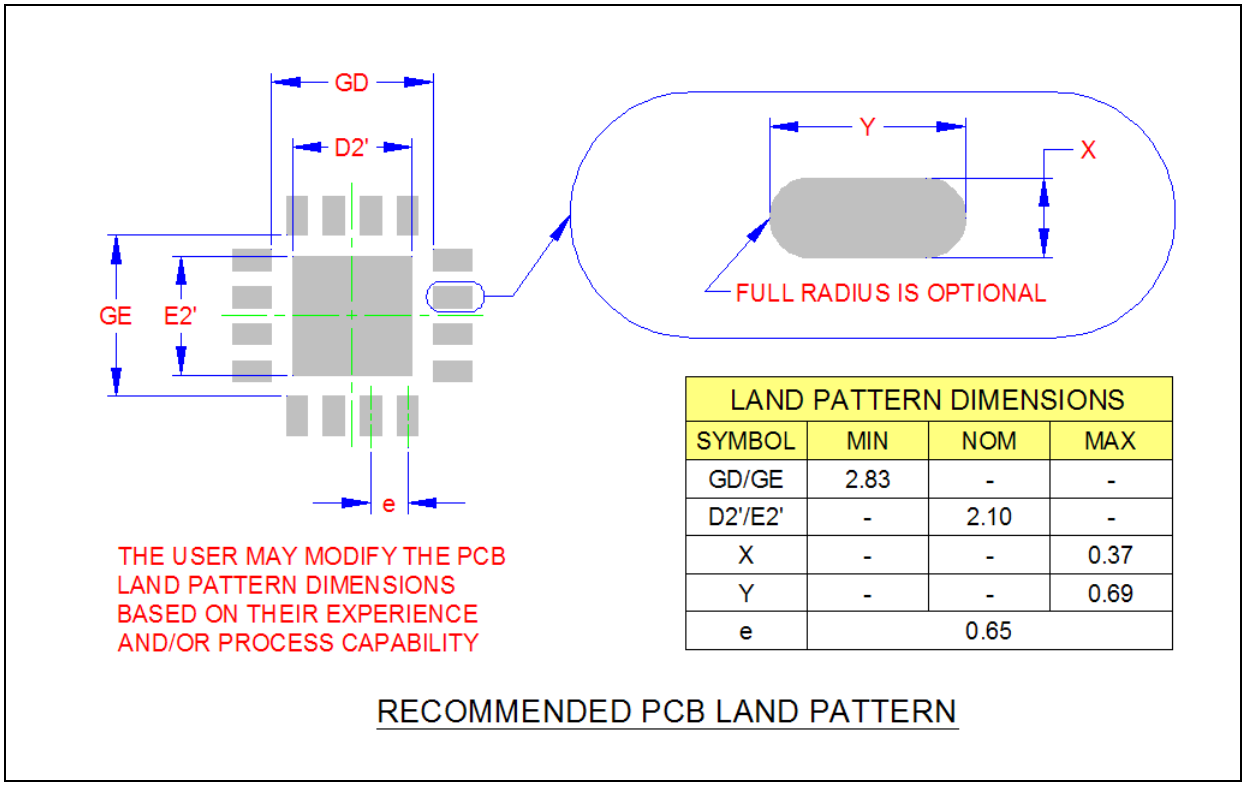


Figure 6.2 16 pin QFN 4mm x 4mm Package Drawing



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	2.83	-	-
D2'/E2'	-	2.10	-
X	-	-	0.37
Y	-	-	0.69
e		0.65	

Figure 6.3 16 pin QFN 4mm x 4mm PCB Footprint