



# 512Kx32 SRAM MODULE, 3.3V

## FEATURES

- DSP Memory Solution
  - ADSP-21060L (SHARC)
  - ADSP-21062L (SHARC)
  - Texas Instruments TMS320LC31
- RISC Memory Solution
  - MPC860 (Power Quic)
- Random Access Memory Array
  - Fast Access Times: 12, 15, 17, and 20ns
  - Individual Byte Enables
  - User configurable organization with Minimal Additional Logic
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 68 Lead PLCC, No. 99 JEDEC MO-47AE
  - Small Footprint, 0.990 Sq. In.
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +3.3V (±5%) Supply Operation

The EDI8L32512V is a high speed, 3.3V, 16 megabit SRAM. The device is available with access times of 12, 15, 17 and 20ns allowing the creation of a no wait state DSP and RISC microprocessor memory solutions.

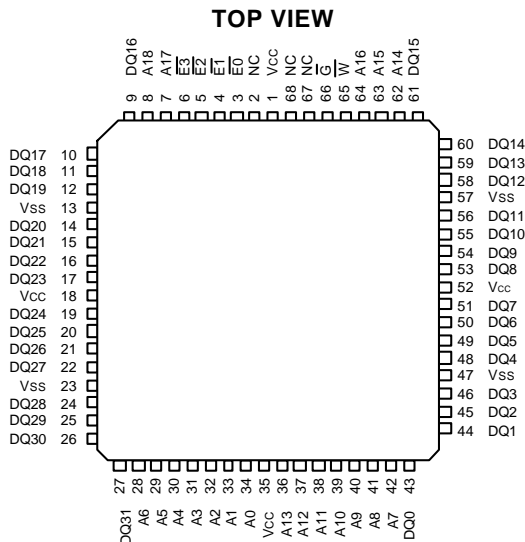
The device can be configured as a 512K x 32 and used to create a single chip external data memory solution for TI's TMS320LC31 (figure 5), or Analog's SHARC™ DSP (figure 6).

The device provides a 56% space savings when compared to four 512K x 8, 36 pin SOJs. In addition the EDI8L32512C has only a 10pF load on the data lines vs. 32pF for four plastic SOJs.

The device provides a memory upgrade of the EDI8L32256V (256K x 32) or the EDI8L32128V (128K x 32) (figure 8). Alternatively, the device's chip enables can configure it as a 1M x 16. A 1Mx 48 program memory array for Analog's SHARC DSP is created using three devices (figure 7). If this memory is too deep, two 512K x 24s (EDI8L24512V) can be used to create a 512K x 48 array or two 128K x 24s (EDI8L24128V) can be used to create a 128K x 48 array.

**Note:** Solder Reflow Temperature should not exceed 260°C for 10 seconds.

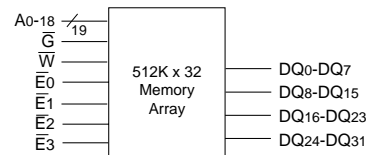
FIG. 1 PIN CONFIGURATION



### PIN DESCRIPTION

A0-18	Address Inputs
$\bar{E}0-3$	Chip Enables (One per Byte)
$\bar{W}$	Master Write Enable
$\bar{G}$	Master Output Enable
DQ0-31	Common Data Input/Output
Vcc	Power (+3.3V±5%)
Vss	Ground
NC	No Connection

### BLOCK DIAGRAM



**NOTE:** For memory upgrade information, refer to Page 7, Figure 8 "EDI MCM-L upgrade path."



**ABSOLUTE MAXIMUM RATINGS**

Voltage on any pin relative to Vss	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	2.5 Watts
Output Current	20 mA
Junction Temperature, TJ	+175°C

\* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**TRUTH TABLE**

$\bar{E}$	$\bar{W}$	$\bar{G}$	Mode	Output	Power
H	X	X	Standby	High Z	Icc2, Icc3
L	H	H	Output Deselect	High Z	Icc1
L	H	L	Read	Data Out	Icc1
L	L	X	Write	Data In	Icc1

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.135	3.3	3.465	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	VIH	2.2	—	Vcc +0.3	V
Input Low Voltage	VIL	-0.3	—	+0.8	V

**CAPACITANCE**

(f = 1.0MHz, VIN = Vcc or Vss)

Parameter	Sym	Max	Unit
Address Lines	C1	30	pF
Data Lines	Cd/O	10	pF
Write & Output Enable Line	$\bar{W}$ , $\bar{G}$	30	pF
Chip Enable Line	E0-3	8	pF

**DC ELECTRICAL CHARACTERISTICS**

(Vcc = 3.3V, TA = 25°C)

Parameter	Symbol	Conditions	12 & 15			17 & 20			Units
			Min	Typ	Max	Min	Typ	Max	
Operating Power Supply Current	Icc1	$\bar{W} = VIL, I/O = 0mA, \text{Min Cycle}$	—	440	720	—	440	640	mA
Standby (TTL) Power Supply Current	Icc2	$\bar{E} \geq VIH, VIN \leq VIL \text{ or } VIN \geq VIH$	—	100	200	—	100	200	mA
Full Standby Power CMOS Supply Current	Icc3	$\bar{E} \geq Vcc - 0.2V$ $VIN \geq Vcc - 0.2V \text{ or } VIN \leq 0.2V$	—	60	100	—	60	100	mA
Input Leakage Current	ILI	VIN = 0V to Vcc	—	—	±10	—	—	±10	µA
Output Leakage Current	ILO	VIO = 0V to Vcc	—	—	±10	—	—	±10	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	—	—	2.4	—	—	V
Output Low Voltage	VOL	IOL = 4.0mA	—	—	0.4	—	—	0.4	V

**AC TEST CONDITIONS**

Figure 1

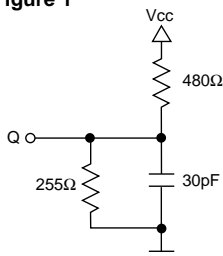
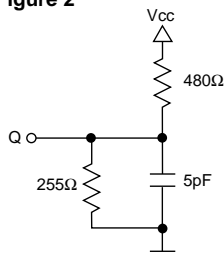


Figure 2



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(NOTE: For tEHOZ, tGHOZ and tWLOZ, CL = 5pF, Figure 2)



**AC CHARACTERISTICS – READ CYCLE**

(V<sub>CC</sub> = 3.3V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0°C to +70°C)

Parameter	Symbol		12ns		15ns		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	12		15		17		20		ns
Address Access Time	tAVQV	tAA		12		15		17		20	ns
Chip Enable Access Time	tELQV	tACS		10		12		15		20	ns
Chip Enable to Output in Low Z (1)	tELOX	tCLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	tEHOZ	tCHZ		6		7		8		9	ns
Output Hold from Address Change	tAVOX	tOH	3		3		3		3		ns
Output Enable to Output Valid	tGLOV	tOE		6		7		8		9	ns
Output Enable to Output in Low Z (1)	tGLOX	tOLZ	0		0		0		0		ns
Output Disable to Output in High Z (1)	tGHOZ	tOHZ		6		7		8		9	ns

1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS – WRITE CYCLE**

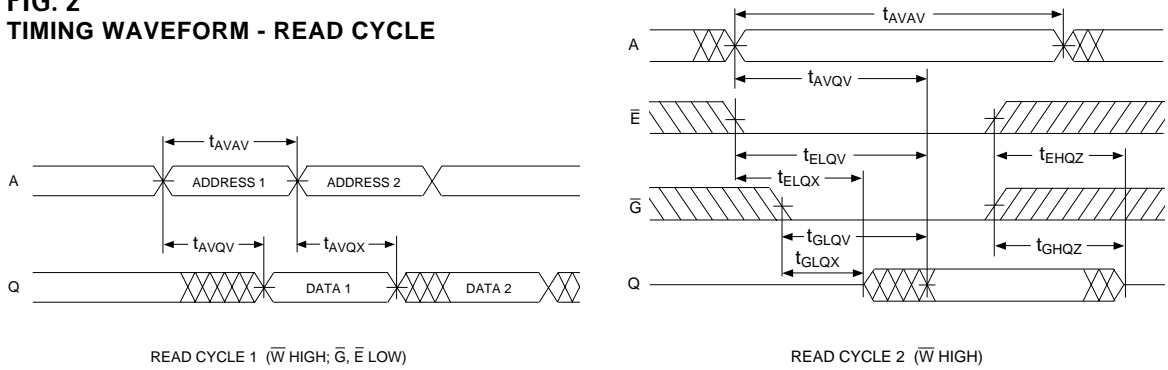
(V<sub>CC</sub> = 3.3V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0°C to +70°C)

Parameter	Symbol		12ns		15ns		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	12		15		17		20		ns
Chip Enable to End of Write	tELWH	tCW	8		10		11		12		ns
	tELEH	tCW	8		10		11		12		ns
Address Setup Time	tAWWL	tAS	0		0		0		0		ns
	tAVEL	tAS	0		0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	8		10		11		12		ns
	tAVEH	tAW	8		10		11		12		ns
Write Pulse Width	tWLWH	tWP	8		10		11		12		ns
	tELEH	tWP	8		10		11		12		ns
Write Recovery Time	tWHAX	tWR	0		0		0		0		ns
	tEHAX	tWR	0		0		0		0		ns
Data Hold Time	tWHDX	tDH	0		0		0		0		ns
	tEHDX	tDH	0		0		0		0		ns
Write to Output in High Z (1)	tWLOZ	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time	tDWWH	tDW	6		7		8		9		ns
	tDVEH	tDW	6		7		8		9		ns
Output Active from End of Write (1)	tWHQX	tWLZ	3		3		3		3		ns

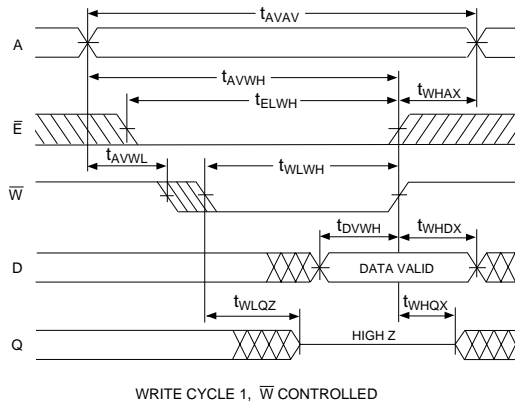
1. This parameter is guaranteed by design but not tested.



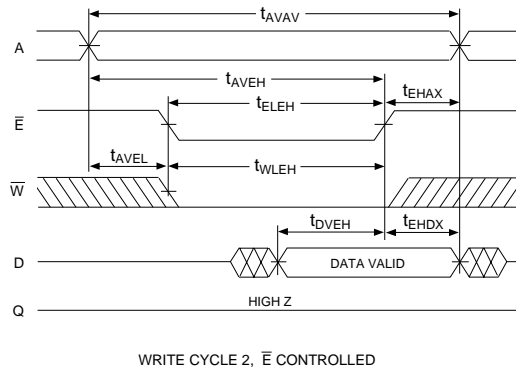
**FIG. 2**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 3**  
**WRITE CYCLE -  $\bar{W}$  CONTROLLED**



**FIG. 4**  
**WRITE CYCLE -  $\bar{E}$  CONTROLLED**



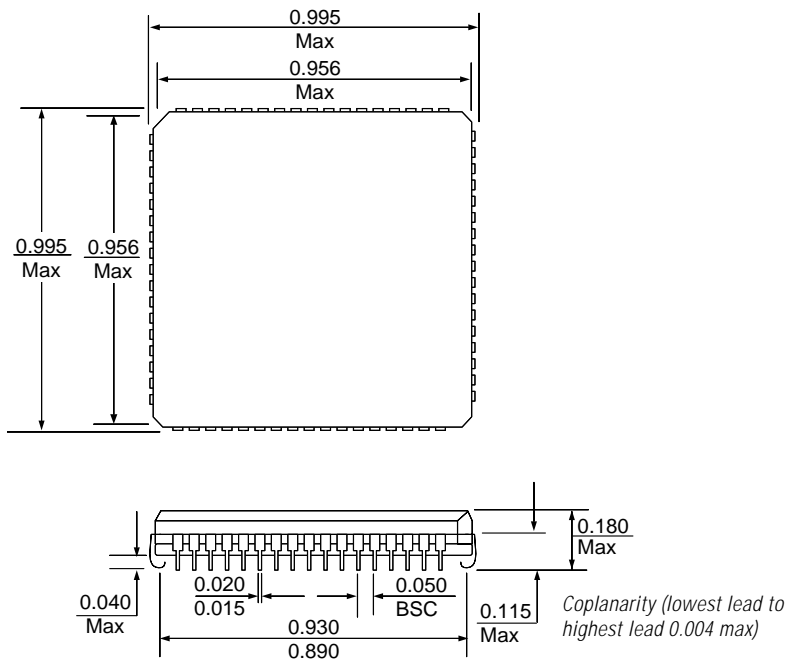


**ORDERING INFORMATION**

Commercial Temperature Range (0°C to +70°C)		
Part Number	Speed (ns)	Package No.
EDI8L32512V12AC	12	99
EDI8L32512V15AC	15	99
EDI8L32512V17AC	17	99
EDI8L32512V20AC	20	99

Industrial Temperature Range (-40°C to +85°C)		
Part Number	Speed (ns)	Package No.
EDI8L32512V15AI	15	99
EDI8L32512V17AI	17	99
EDI8L32512V20AI	20	99

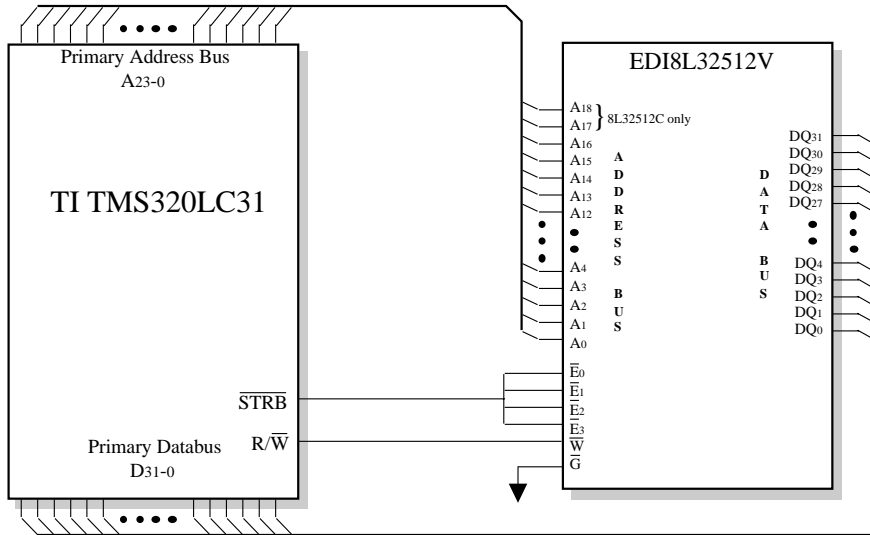
**PACKAGE 99: 68 LEAD PLCC**  
**JEDEC MO-47AE**



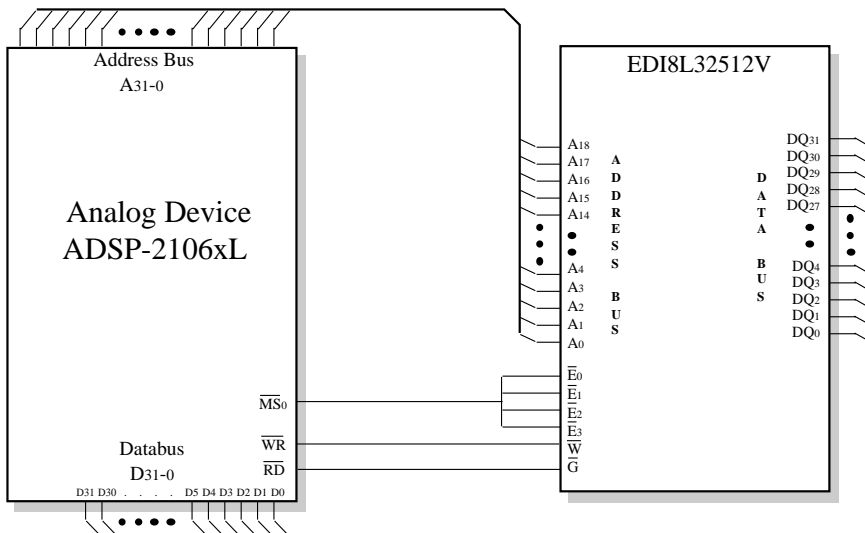
ALL DIMENSIONS ARE IN INCHES



**FIG. 5**  
**INTERFACING THE TEXAS INSTRUMENTS TMS320LC31 WITH**  
**THE EDI8L32512V (512Kx32)**

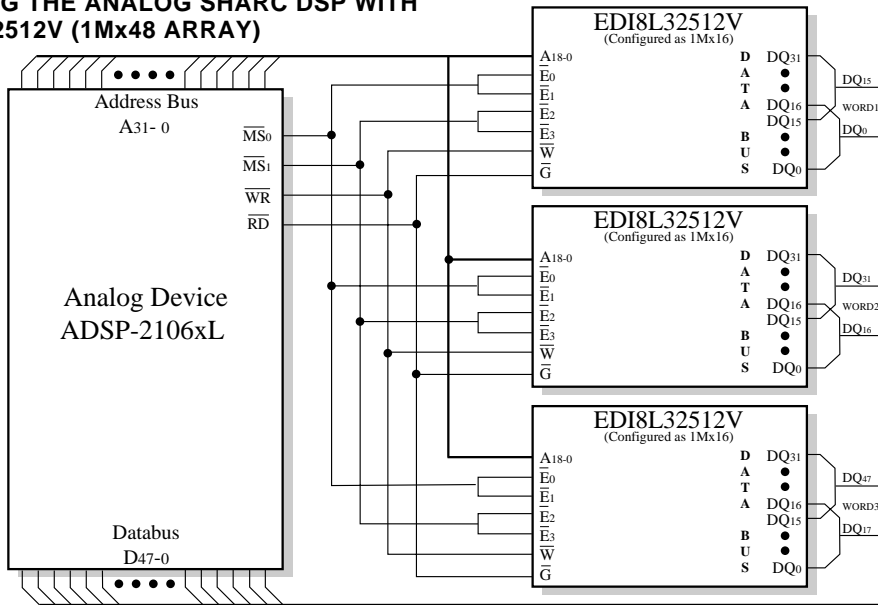


**FIG. 6**  
**INTERFACING THE ANALOG SHARC DSP WITH**  
**THE EDI8L32512V (512Kx32 ARRAY).**





**FIG. 7**  
**INTERFACING THE ANALOG SHARC DSP WITH**  
**THE EDI8L32512V (1Mx48 ARRAY)**



**FIG. 8**  
**MCM-L UPGRADE PATH**

512Kx32  
 256Kx32  
 128Kx32

