Edge649
Octal Pin Electronics Driver/Receiver

TEST AND MEASUREMENT PRODUCTS

Description

The Edge649 is an octal pin electronics driver and receiver combination fabricated in a high- performance CMOS process. It is designed for automatic test equipment and instrumentation where cost, functional density, and power are all at a premium.

The Edge649 incorporates eight channels of programmable drivers and receivers into one package. Each channel has per pin driver levels, receiver threshold, and tristate control.

The 11V driver output and receiver input range allows the Edge649 to interface directly between TTL, ECL, CMOS (3V, 5V, and 8V), and custom level circuitry.

The Edge649 is pin and functionally compatible with the EDGE648, with the following performance differences:

- reduced driver preshoot
- faster driver propagation delay
- superior driver pulse width distortion
- higher driver Fmax operation
- slightly slower driver output slew rates
- higher comparator Fmax operation
- lower comparator propagation delay
- superior comparator pulse width distortion.

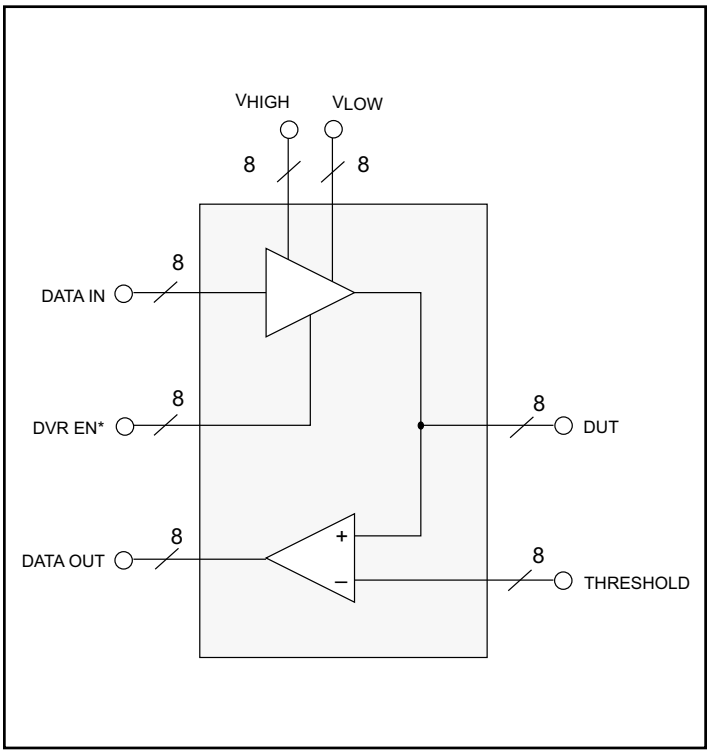
Applications

- Burn-In ATE
- Functional Board Testers
- In-Circuit Board Testers
- Combinational Board Testers
- Low Cost Chip Testers
- ASIC Verifiers
- VXI-Based Test Equipment

Features

- 50 MHz Operation
- 11 V DUT I/O Range
- Programmable Output Levels
- Programmable Input Thresholds
- Per Pin Flexibility
- High Integration Levels
- 615 mW Quiescent Power Dissipation
- Edge648 Compatible

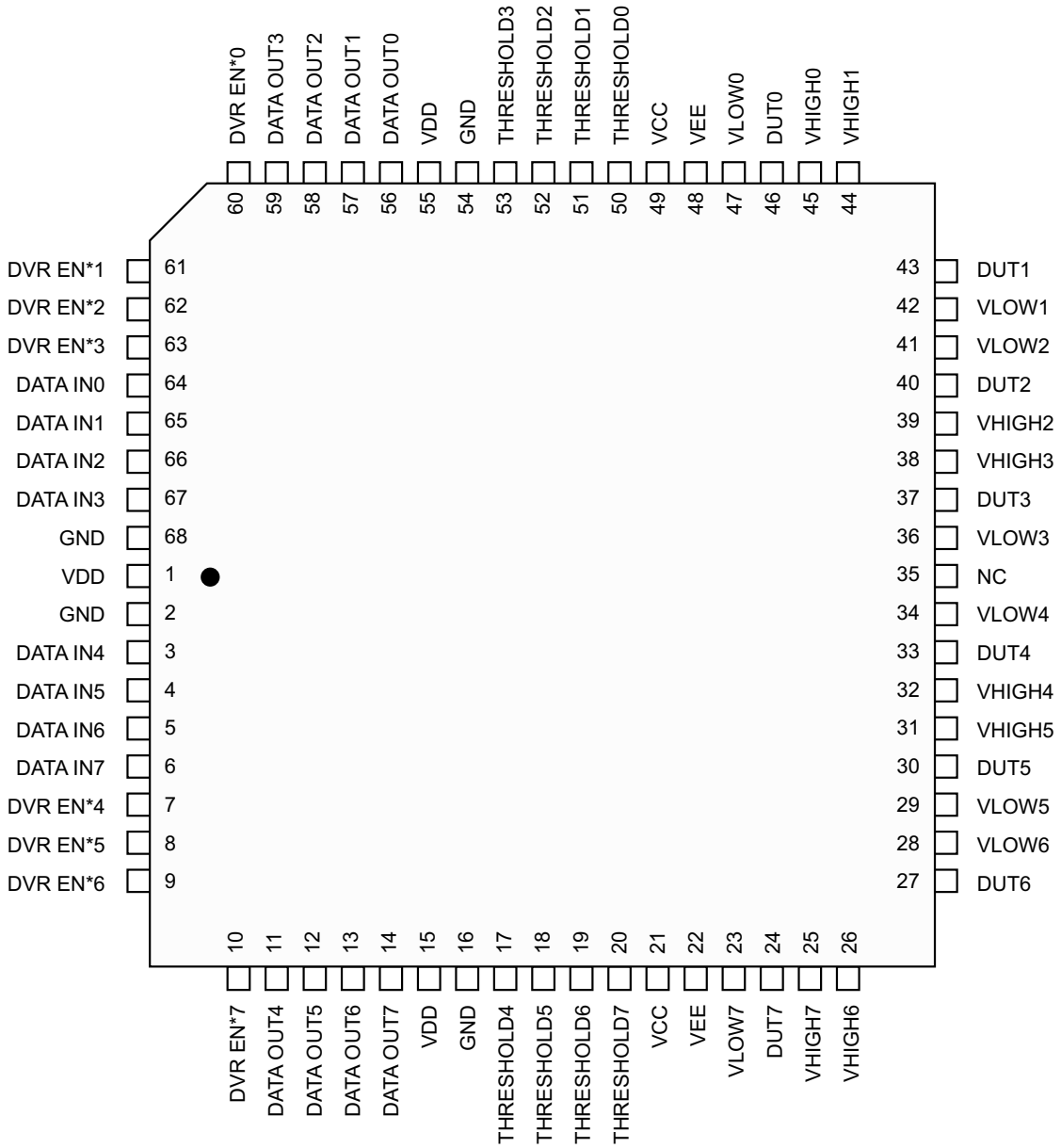
Functional Block Diagram



PIN Description

Pin Name	Pin Number	Description
DATA IN (0:7)	64, 65, 66, 67, 3, 4, 5, 6	TTL compatible inputs that determine the high/low status of the DUT drivers.
DATA OUT (0:7)	56, 57, 58, 59, 11, 12, 13, 14	CMOS level outputs that indicate the status of the DUT receivers.
DUT (0:7)	46, 43, 40, 37, 33, 30, 27, 24	Pin electronic inputs/outputs that receive/drive the device under test.
DVR EN (0:7)	60, 61, 62, 63, 7, 8, 9, 10	TTL compatible inputs that control the high impedance state of the DUT drivers.
VHIGH (0:7)	45, 44, 39, 38, 32, 31, 26, 25	Unbuffered analog inputs that set the voltage level of a logical 1 of the DUT drivers.
VLOW (0:7)	47, 42, 41, 36, 34, 29, 28, 23	Unbuffered analog inputs that set the voltage level of a logical 0 of the DUT drivers.
THRESHOLD (0:7)	50, 51, 52, 53, 17, 18, 19, 20	Buffered analog input voltage that sets the threshold for the DUT comparators.
VCC	21, 49	Analog positive power supply.
VEE	22, 48	Analog negative power supply.
VDD	1, 15, 55	Digital power supply.
GND	2, 16, 54, 68	Device ground.
N/C	35	No connection.

PIN Description *(continued)*



Driver Description

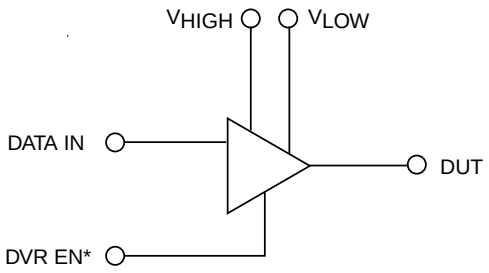


Figure 1. Driver Diagram

As shown in Figure 1, Edge649 supports programmable high and low levels and tristate per channel. There are no shared lines between any drivers. The DVR EN* and DATA IN signals are TTL compatible inputs that control the driver (see Figure 2).

With DVR EN* high, the DUT driver goes into a high impedance state. With DVR EN* low, DATA IN high forces the driver into a high state (DUT = V_{HIGH}), and DATA IN low forces the driver low (DUT = V_{LOW}).

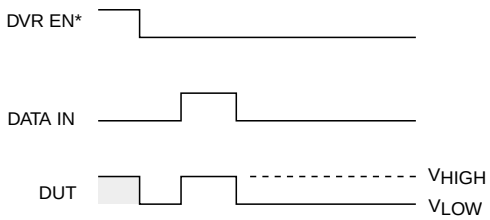


Figure 2. Driver Functionality

V_{HIGH} and V_{LOW}

V_{HIGH} and V_{LOW} define the logical "1" and "0" levels of the DUT driver and can be adjusted anywhere over the range determined by VCC and VEE. Table 1 documents the relationship between the analog power to supplies (VCC and VEE), the driver range (V_{HIGH} and V_{LOW}), and the comparator threshold range ($V_{THRESHOLD}$).

The V_{HIGH} and V_{LOW} inputs are unbuffered in that they also provide the driver output current (see Figure 3), so the source of V_{HIGH} and V_{LOW} must have ample current drive capability.

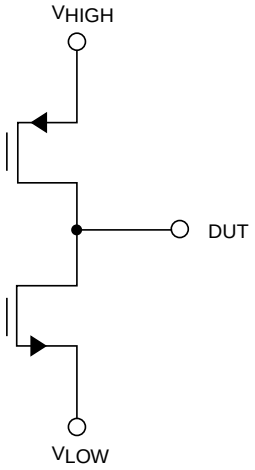


Figure 3. Simplified Model of the Unbuffered Output Stage

Drive/Receive Common Mode Range	Threshold Range	Power Supply Conditions
0V <= DUT <= +6.5V	0.1V <= THRESHOLD <= 3.0V	VCC = +6.5V VEE = 0V
0V <= DUT <= +8V	0.1V <= THRESHOLD <= 4.5V	VCC = +8V VEE = 0V
0V <= DUT <= +11V	0.1V <= THRESHOLD <= 7.5V	VCC + 11V VEE = 0V
-3V <= DUT <= +8V	-2.9V <= THRESHOLD <= 4.5V	VCC = +8V VEE = -3V

Table 1. Power Supply Requirement

Circuit Description *(continued)*

Driver Output Protection

In a functional testing environment, where a resistor is added in series with the driver output, the Edge649 can withstand a short to any legal DUT voltage for an indefinite amount of time.

In a low impedance application with no additional output series resistance, care must be exercised and systems should be designed to check for this condition and tristate the driver if a short is detected.

Receiver Functionality

Edge649 supports programmable thresholds per channel. There are no shared lines between comparators. THRESHOLD is a high input impedance analog input which defines a logical “1” and “0” at the DUT (see Figure 4). If the DUT voltage is more positive than THRESHOLD, DATA OUT will be high. With DUT lower than THRESHOLD, DATA OUT will be low.

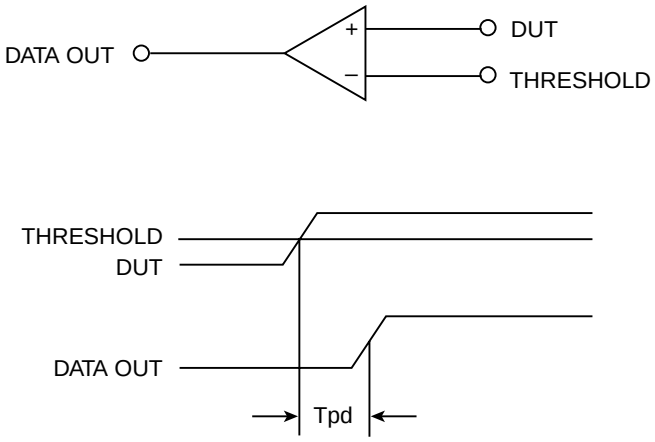


Figure 4. Receiver Functionality

Power Supplies

The Edge649 uses three power supplies: VDD, VCC and VEE. VDD is the digital supply for all of the data inputs and outputs. VCC and VEE are the analog power supplies for the Edge649 drivers and comparators. In order to protect the Edge649 and avoid damaging it, the following power supply requirements must be satisifed at all times:

$$VEE \le GND \le VDD \le VCC$$

Also, $VEE \le$ All Inputs $\le VCC$ at all times

The three-diode configuration shown in Figure 5, used on a once-per-board basis, insures power supply sequence and fault tolerance.

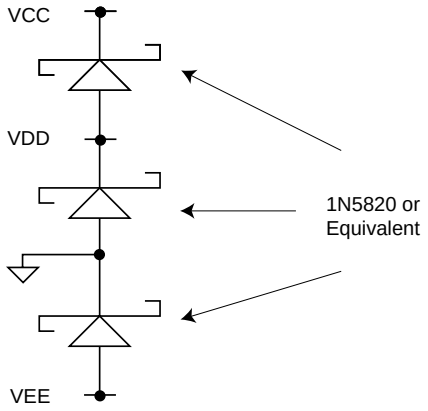


Figure 5. Power Supply Protection Scheme

The sequence below can be used as a guideline with the Edge649:

Power-On Sequencing	*Power-Off Sequencing*
1. VCC (substrate)	1. Inputs
2. VEE	2. VDD
3. VDD	3. VEE
4. Inputs	4. VCC

Power Supplies Decoupling

VDD, which provides the digital power, should be decoupled to GND with a .1 µF chip capacitor in parallel with a .001 µF chip capacitor. The bypass capacitors should be as close to the device as possible. Power and ground planes are recommended to provide a low inductance return path.

VCC and VEE, which power the DUT drivers and receivers, should also be decoupled to GND with a .1 µF chip capacitor in parallel with a .001 µF chip capacitor. A VCC and VEE plane, or at least a solid power bus, is recommended for optimal performance.

V_{HIGH} and V_{LOW} Decoupling

As the V_{HIGH} and V_{LOW} inputs are unbuffered and must supply the driver output current, decoupling capacitors for these inputs are recommended in proportion to the amount of output current the application requires

Expanding the Common Mode Range

Although the Edge649 can drive and receive 11V swings, these 11 V signals can be adjusted over an 14V range. By using programmable regulators V1 and V2 for the VCC and VEE supplies (feasible because these two analog power supplies do not supply driver output current), the Edge649 I/O range can be optimized for a variety of applications (see Figure 6).

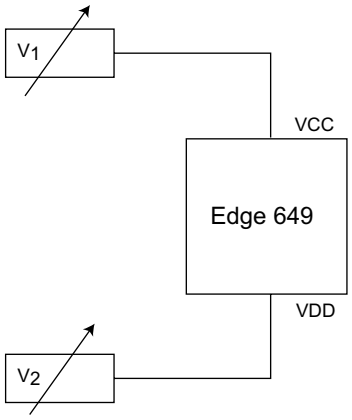


Figure 6.

There are three rules which govern the supplies V1 and V2:

1) $VDD + 1.5V \le V1 \le +11V$
2) $-3V \le V2 \le 0V$
3) $(V1 - V2) \le 11V$

Window Comparator

Certain applications require a dual threshold window comparator to distinguish between the DUT being high, low, or floating. To support this application, two Edge649 channels can be combined to create one channel with a window comparator (see Figure 7). Notice that connecting two DUT pins ties together the positive inputs of both receivers. The result is a difference in polarity between the digital outputs reporting the high and low status of the DUT.

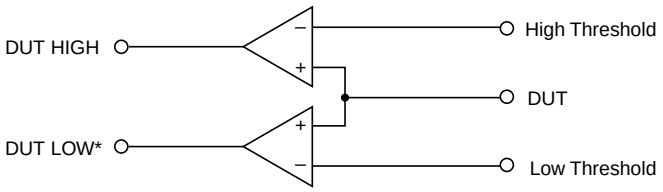


Figure 7. Edge649 as a Window Comparator

Once two receivers are connected as window comparators, the two drivers also get connected in parallel. This dual driver configuration supports a multitude of applications that have traditionally been difficult to accommodate.

Trinary Driver

At times, there is a need for a three-level driver. Typically, two levels are required for the standard digital "1" and "0" pattern generation. The third level provides a higher voltage to place the device under test (DUT) into a programming or test mode. By controlling the DATA IN and DVR EN* inputs, a trinary driver with tristate is realizable (see Figure 8).

Driver with Pull Up/Pull Down

As the drivers are unbuffered, paralleling two drivers for one DUT node provides a means for adding pull up or pull down capability. By connecting the V_{HIGH} and V_{LOW} inputs of one driver through a resistor to a voltage, additional functionality that would normally require an external relay on the DUT transmission line to engage and disengage these functions is realizable.

One common application for the pull up feature is testing open collector devices. The pull down satisfies open emitter DUTs (typically ECL). Either the pull up or down could be used to establish a default high impedance voltage on a bidirectional bus. Notice that in all applications, the resistors can be switched dynamically or statically.

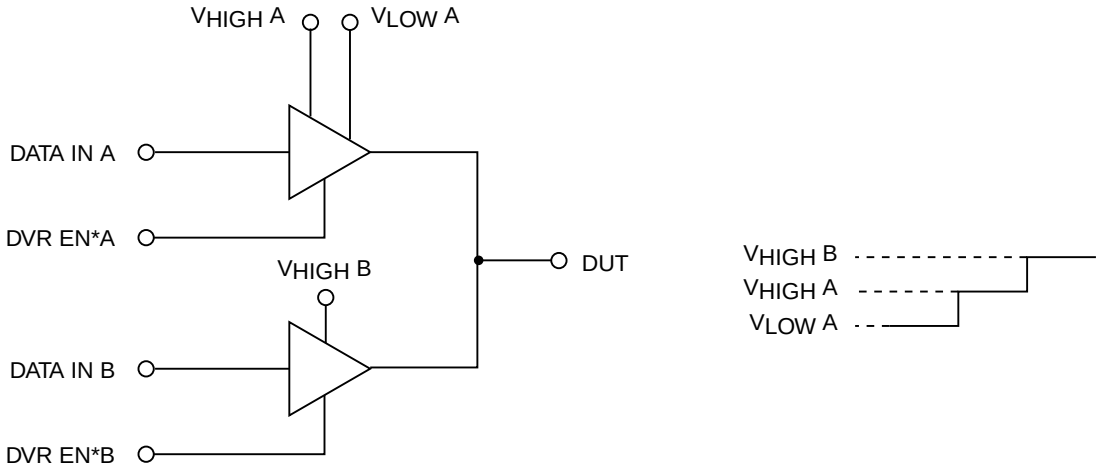


Figure 8. Trinary Driver

Also, either the pull up or pull down resistor could be used to terminate the transmission from the DUT to the pin electronics in an effort to minimize any reflections.

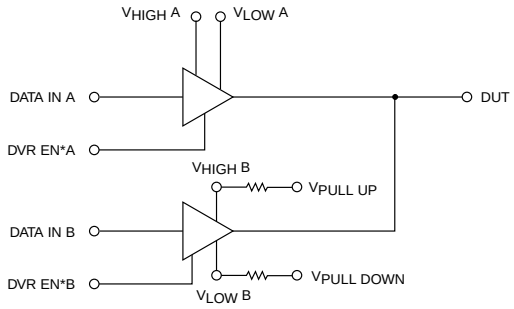


Figure 9. Driver with Pull Up/Pull Down

Trinary Driver with Termination

Other combinations are also possible. For example, two parallel drivers can be configured to implement one trinary driver with a pull down (or pull up) dynamic termination (see Figure 10).

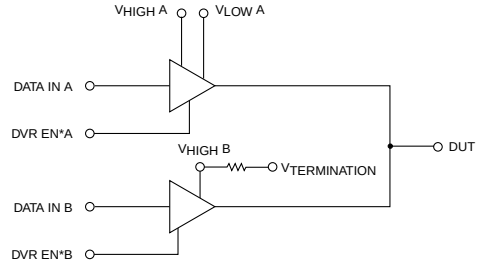


Figure 10. Trinary Driver with Termination

Two Logic Family Driver

Many test systems support exactly two families of driver and receiver levels and select between family A and family B settings on a per-pin basis, typically using an analog multiplexer, (See Figure 11.) Common examples of these families are:

Family A = TTL
Family B = CMOS
or
Family A = TTL
Family B = ECL

The Edge649 supports this system architecture with minimal hardware and the elimination of the per-pin analog multiplexer. The drive and receive levels need to be generated once per system, then distributed and buffered suitably.

Parametric Functions

Two drivers in parallel also offer the possibility of connecting force and sense parametric circuitry to the DUT without adding additional circuitry to the controlled impedance DUT line. For example, Figure 12 shows the second driver being utilized to force a current and measure a voltage.

Notice that the V_{HIGH} and V_{LOW} pins are used from different drivers to allow the force and sense functions to be active simultaneously.

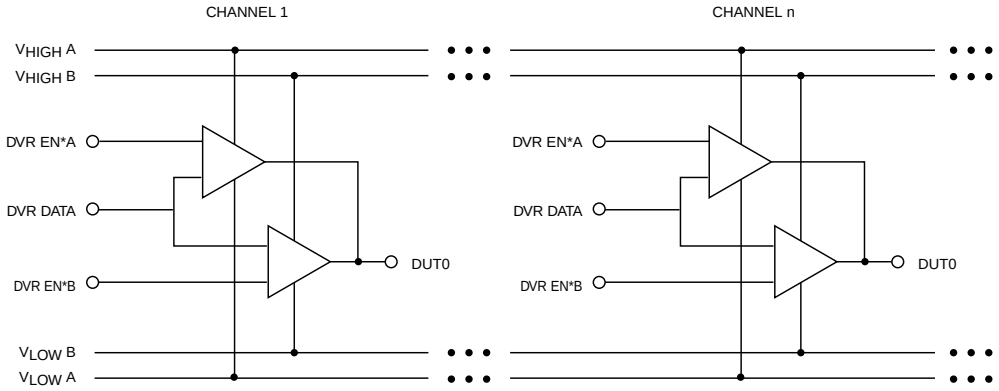


Figure 11. Family A/B Using Two Drivers Per Pin

Optional Output Configuration

Certain functional applications require a series output resistor yet also demand that the comparator be connected directly to the DUT, not via the backmatch resistor. To create this configuration, two distinct termination resistors may be connected to the V_{HIGH} and V_{LOW} input pins (see Figure 13).

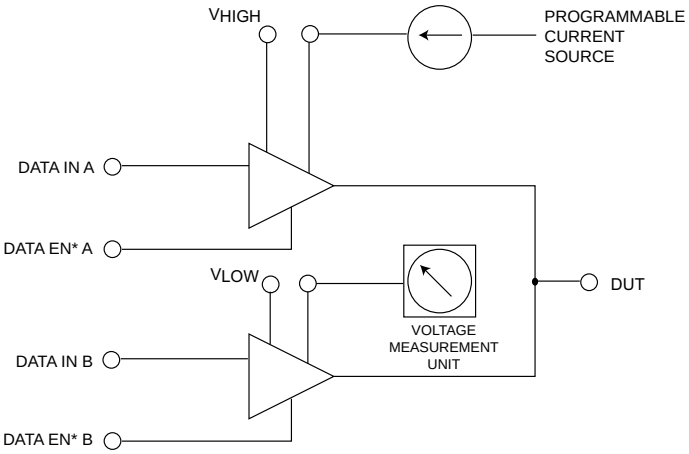


Figure 12. Edge649 Supporting Parametric Testing

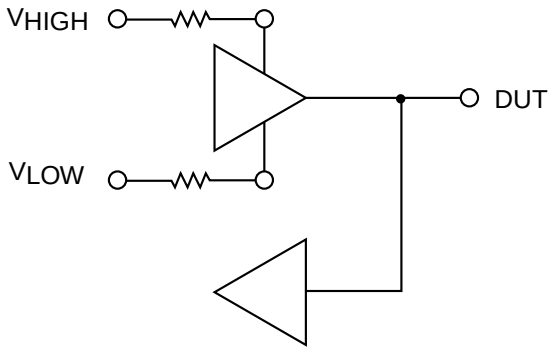
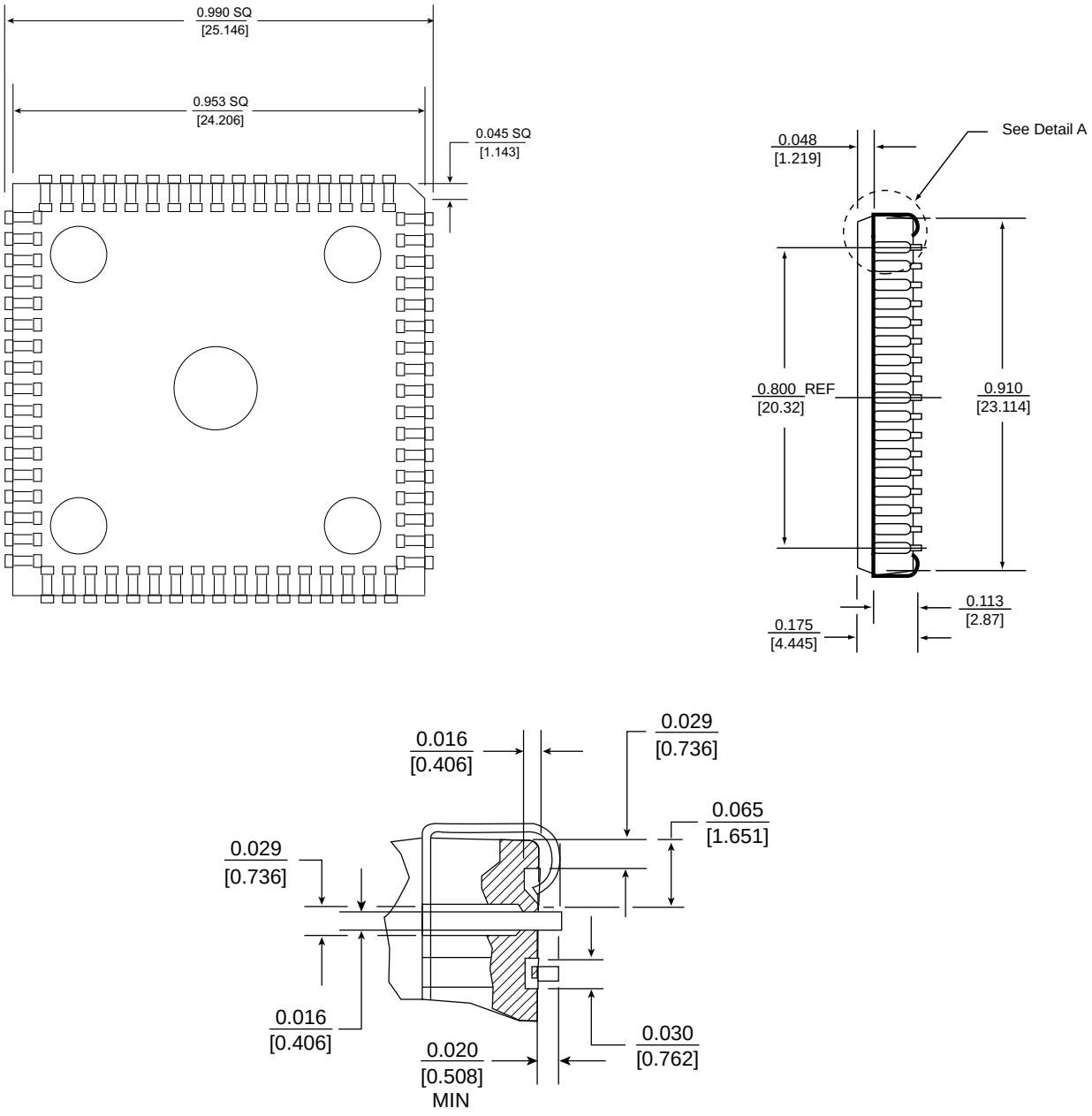


Figure 13. Functional Application with the Comparator Connected Directly to the DUT

Thermal Information

Parameter	Symbol	Min	Typ	Max	Units
Thermal Resistance Junction to Case	θJC		9.8		°C/W
Junction to Air Still Air 50 LFPM 400 LFPM	 θJA θJA θJA		 34 26 19		 °C/W °C/W °C/W

68 Pin PLCC Package
θJA = 42 to 48˚C / W



Notes: (unless otherwise specified)
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital Power Supply	VDD	4.5	5	5.5	V
Analog Positive Power Supply	VCC	VDD + 2.0		11	V
Analog Negative Power Supply	VEE	-3		0	V
Total Analog Power Supply	VCC - VEE	7.0		11	V
Ambient Operating Temperature	TA TJ	0 0		+70 +125	°C °C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Total Analog Power Supply	VCC - VEE			13	V
Positive Analog Power Supply	VCC	+5.0		13	V
Negative Analog Power Supply	VEE	-4.0		0.5	V
Driver High Output Voltage	V_{HIGH}	VEE - .5		VCC + .5	V
Driver Low Output Voltage	V_{LOW}	VEE - .5		VCC + .5	V
Driver Output Swing	V_{HIGH} - V_{LOW}	-5		12	V
Receiver Threshold Voltage	THRESHOLD	VEE - .5		VCC + .5	V
Digital Inputs	DATA IN DVR EN*	GND - .5		VDD + .5	V
Digital Power Supply	VDD	0		6.5	V
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver/Receiver Characteristics					
Driver High Voltage Level	V_{HIGH}				
@ ± 1 mA		VEE + 3		VCC	V
@ ± 125 mA		VEE + 7		VCC	V
Driver Low Voltage Level	V_{LOW}				
@ ±1 mA		VEE		VCC – 3	V
@ ±125 mA		VEE		VCC – 7	V
DC Driver Output Current (Note 1)	I_{OUT}	–125		+125	mA
Driver Output Impedance	R_{OUT}				
@ ± 1 mA				40	Ω
@ ± 125 mA			8	17	Ω
DUT Pin Capacitance	C_{OUT}		20		pF
DUT Output voltage	DUT<0:7>	VEE		VCC	V
Receiver Threshold Level	$V_{THRESHOLD}$	VEE + 0.1		VCC – 3.5	V
Threshold Bias Current	I_{BIAS}		0	1.0	µA
DUT Leakage Input Current	I_{LEAK}		.002	1.0	µA
Receiver Offset Voltage	VOS	–200	45	200	mV
Quiescent Power Supply Current					
Positive Power Supply	ICC		25	40	mA
Negative Power Supply	IEE		25	40	mA
Digital Power Supply	IDD		20	35	mA
Digital Inputs ***DATA IN (0:7), DVR EN* (0:7)***					
Input High Voltage	VIH_{MIN}	2.0			V
Input Low Voltage	VIL_{MAX}			0.8	V
Input Current	I_{IN}			1.0	µA
Input Capacitance	C_{IN}		5		pF
Digital Outputs ***DATA OUT (0:7)***					
Output Voltage High (Note 2)	VOH	VDD – .4			V
Output Voltage Low (Note 3)	VOL			GND + .4	V
DC Output current	I_{OUT}	–4		4	mA

Note 1 : Output current specification is per individual driver.
Note 2: Output current of 4 mA.
Note 3: Output current of –4 mA.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay					
DATA IN <0:7> to DUT <0:7> (Note 2)	T1	12	20	33	ns
DUT <0:7> to DATA OUT <0:7> (Note 3)	T2	8	15	27	ns
Active to HiZ (Note 4)	T3	17	25	38	ns
HiZ to Active (Note 4)	T4	12	20	33	ns
DUT Output Rise/Fall Times (Note 1)					
1V Swing (20% - 80%)			3.0		ns
3V Swing (10% - 90%)			3.5		ns
5V Swing (10% - 90%)			4.0		ns
8V Swing (10% - 90%)			4.5		ns
10V Swing (10% - 90%)			5.0		ns
Digital Outputs (DATA OUT <0:7>)					
DATA OUT Rise Time (10% - 90%)	TR		2		ns
DATA OUT Fall Time (10% - 90%)	TF		2		ns
Minimum Pulse Width					
Driver Output			20		ns
Comparator Output			10		ns
Maximum Operating Frequency	Fmax		50		MHz

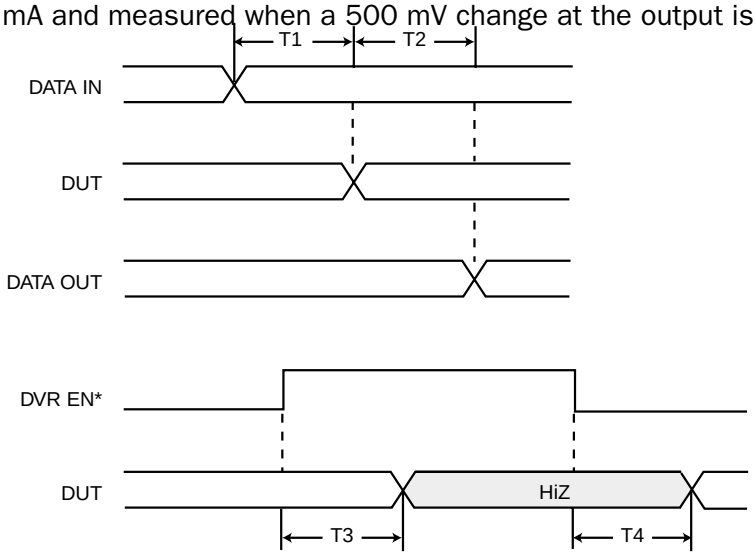
AC Test Conditions: VCC = 8V, VEE = –3V, VDD = 5V.

Note 1: Into 18 inches of 50Ω transmission line terminated with 1KΩ and 5 pF with the proper series termination resistor.

Note 2: Measured at 2.5V with a 10 mA load under the following conditions: VHIGH = +5.0V, VLOW = 0V, VCC = +8V, VEE = -3V, and VDD = +5V.

Note 3: Measured at 2.5V with a 4 mA load.

Note 4: Load = 10 mA and measured when a 500 mV change at the output is detected.



Ordering Information

Model Number	Package
E649APJ	68-Pin PLCC
EVM649APJ	Edge649 Evaluation Module

Contact Information

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Revision History

Current Revision Date: October 21, 2002
Previous Revision Date: June 11, 2002

Page #	Section Name	Previous Revision	Current Revision
6	Power Supplies		Para 1 rewritten. Para 2 deleted. Power On & Off Sequencing added

Current Revision Date: June 11, 2002
Previous Revision Date: December 6, 2001

Page #	Section Name	Previous Revision	Current Revision
2	Pin Descriptions	VLOW	Change Pin #44 to Pin #47
14	Ordering Information	E649BPJ EVM649EVM	E649APJ EVM649APJ

Revision History

Current Revision Date: December 6, 2001
Previous Revision Date: October 28, 1996

Page #	Section Name	Previous Revision	Current Revision
4	Circuit Description	Table 1	Update Threshold Ranges
11	Recommended Operating Conditions	 Analog Positive Power Supply, Min: VDD + 1.5 Total Analog Power Supply, Min: 6.5	*Delete:* Driver High Output Voltage Driver Low Output Voltage Total Driver Output Swing Receiver Threshold Voltage Analog Positive Power Supply, Min: VDD + 2.0 Total Analog Power Supply, Min: 7.0
12	DC Characteristics	 Driver High Voltage @ ±1 mA, Min: VEE @ ± 125 mA, VEE + 6 Driver Low Voltqge @ ±1 mA, Max: VCC @ ± 125 mA, Max: VCC – 6 Driver Output Impedance @ ± 1 mA, Max: TBD @ ±125 mA, Max: 12 Receiver Threshold Level, Max: VCC – 1.5 Receiver Offset Voltage, Min: –100, Typ: +25, Max: 100	*Add:* Driver High Voltage Driver Low Voltage Driver Output Impedance *Delete:* Driver Headroom *Delete: Output Voltage Swing* Driver High Voltage Level @ ±1 mA, Min: VEE + 3 @ ± 125 mA, VEE + 7 Driver Low Voltqge Level @ ±1 mA, Max: VCC – 3 @ ± 125 mA, Max: VCC – 7 Driver Output Impedance @ ± 1 mA, Max: 40 @ ±125 mA, Max: 17 Receiver Threshold Level, Max: VCC – 3.5 Receiver Offset Voltage, Min: –200, Typ: 45, Max: 200
13	AC Characteristics		*Add:* AC Test Conditions