ELPIDA

DATA SHEET

128MB SDRAM S.O.DIMM

EBS12UC6APS (16M words × 64 bits, 1 bank)

Description

The EBS12UC6APS is 16M words × 64 bits, 1 bank Synchronous Dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 4 pieces of 256M bits SDRAM (EDS2516APTA) sealed in TSOP package. This module provides high density and large quantities of memory in a small space without utilizing the surface mounting technology. Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Fully compatible with 8 bytes S.O.DIMM: JEDEC standard outline
- 144-pin socket type small outline dual in line memory module (S.O.DIMM)
  - PCB height: 31.75mm (1.25inch)
  - Lead pitch: 0.80mm
- 3.3V power supply
- Clock frequency: 100MHz/133MHz (max.)
- LVTTL interface
- Data bus width: × 64 non-ECC
- Single pulsed /RAS
- 4 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length (BL): 1, 2, 4, 8, Full page
- 2 variations of burst sequence
  - Sequential
  - Interleave
- Programmable /CAS latency (CL): 2, 3
- Byte control by DQMB
- Refresh cycles: 8192 refresh cycles/64ms
- 2 variations of refresh
  - Auto refresh
  - Self refresh

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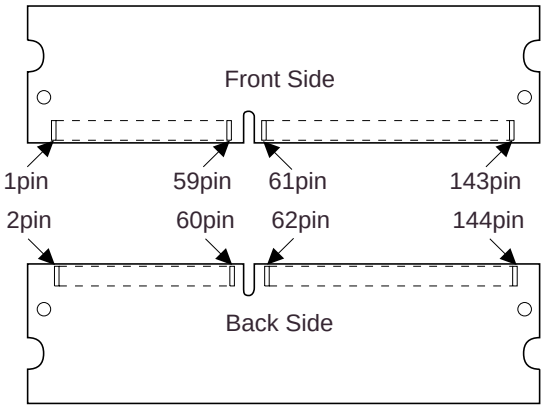
Ordering Information

Part number	Clock frequency MHz (max.)	/CAS latency	Package	Contact pad	Mounted devices
EBS12UC6APS-7A	133	2, 3	144-pin S.O.DIMM	Gold	EDS2516APTA
EBS12UC6APS-75 *	133	3			
EBS12UC6APS-80	100	2, 3			
EBS12UC6APS-7AL	133	2, 3			
EBS12UC6APS-75L*	133	3			
EBS12UC6APS-80L	100	2, 3			

Note: 100MHz operation at /CAS latency = 2.

Pin Configurations



Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VSS	73	NC	2	VSS	74	CLK1
3	DQ0	75	VSS	4	DQ32	76	VSS
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	VDD	10	DQ35	82	VDD
11	VDD	83	DQ16	12	VDD	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	VSS	20	DQ39	92	VSS
21	VSS	93	DQ20	22	VSS	94	DQ52
23	DQMB0	95	DQ21	24	DQMB4	96	DQ53
25	DQMB1	97	DQ22	26	DQMB5	98	DQ54
27	VDD	99	DQ23	28	VDD	100	DQ55
29	A0	101	VDD	30	A3	102	VDD
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	BA0
35	VSS	107	VSS	36	VSS	108	VSS
37	DQ8	109	A9	38	DQ40	110	BA1
39	DQ9	111	A10 (AP)	40	DQ41	112	A11
41	DQ10	113	VDD	42	DQ42	114	VDD
43	DQ11	115	DQMB2	44	DQ43	116	DQMB6

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
45	VDD	117	DQMB3	46	VDD	118	DQMB7
47	DQ12	119	VSS	48	DQ44	120	VSS
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	VSS	127	DQ27	56	VSS	128	DQ59
57	NC	129	VDD	58	NC	130	VDD
59	NC	131	DQ28	60	NC	132	DQ60
61	CLK0	133	DQ29	62	CKE0	134	DQ61
63	VDD	135	DQ30	64	VDD	136	DQ62
65	/RAS	137	DQ31	66	/CAS	138	DQ63
67	/WE	139	VSS	68	NC	140	VSS
69	/CS0	141	SDA	70	A12	142	SCL
71	NC	143	VDD	72	NC	144	VDD

Pin Description

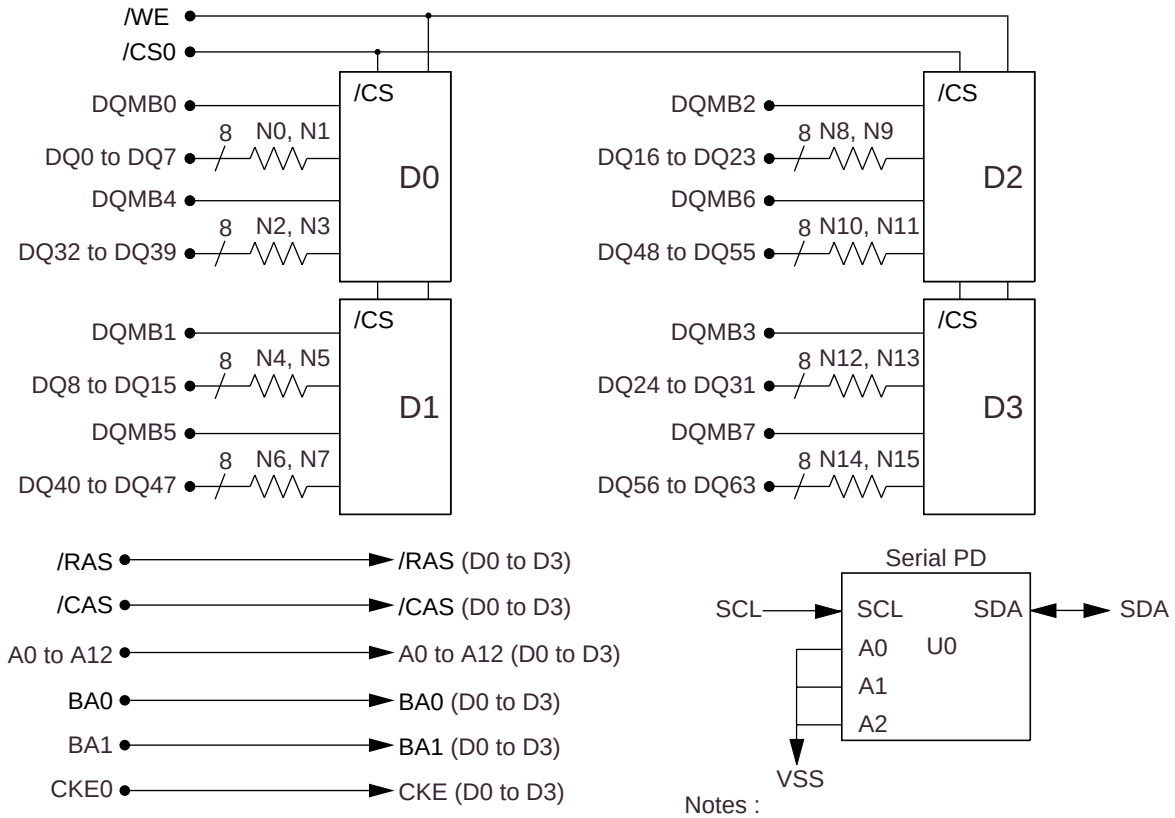
Pin name	Function
A0 to A12	Address input — Row address A0 to A12 — Column address A0 to A8
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
/CS0	Chip select input
/RAS	Row enable (/RAS) input
/CAS	Column enable (/CAS) input
/WE	Write enable input
DQMB0 to DQMB7	Byte data mask
CLK0, CLK1	Clock input
CKE0	Clock enable input
SDA	Data input/output for serial PD
SCL	Clock input for serial PD
VDD	Primary positive power supply
VSS	Ground
NC	No connection

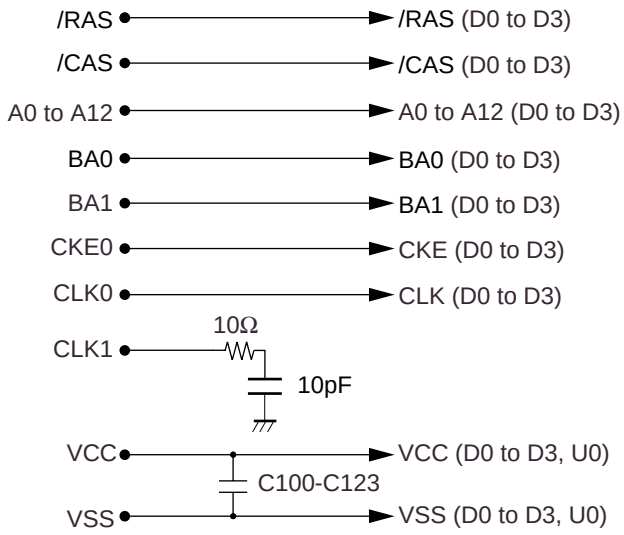
Serial PD Matrix

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80H	128 bytes
1	Total SPD memory size	0	0	0	0	1	0	0	0	08H	256 bytes
2	Memory type	0	0	0	0	0	1	0	0	04H	SDRAM
3	Number of row addresses bits	0	0	0	0	1	1	0	1	0DH	13
4	Number of column addresses bits	0	0	0	0	1	0	0	1	09H	9
5	Number of banks	0	0	0	0	0	0	0	1	01H	1
6	Module data width	0	1	0	0	0	0	0	0	40H	64 bits
7	Module data width (continued)	0	0	0	0	0	0	0	0	00H	0
8	Module interface signal levels	0	0	0	0	0	0	0	1	01H	LVTTL
9	SDRAM cycle time at CL = 3 (highest /CAS latency) (-7A/7AL, -75/75L)	0	1	1	1	0	1	0	1	75H	7.5ns
	(-80/80L)	1	0	0	0	0	0	0	0	80H	8ns
10	SDRAM access from Clock at CL = 3 (highest /CAS latency) (-7A/7AL, -75/75L)	0	1	0	1	0	1	0	0	54H	5.4ns
	(-80/80L)	0	1	1	0	0	0	0	0	60H	6ns
11	Module configuration type	0	0	0	0	0	0	0	0	00H	None.
12	Refresh rate/type	1	0	0	0	0	0	1	0	82H	7.8µs
13	SDRAM width	0	0	0	1	0	0	0	0	10H	× 16
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00H	None.
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01H	1 CLK
16	SDRAM device attributes: Burst lengths supported	1	0	0	0	1	1	1	1	8FH	1,2,4,8,F
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	1	0	0	04H	4
18	SDRAM device attributes: /CAS latency	0	0	0	0	0	1	1	0	06H	2,3
19	SDRAM device attributes: /CS latency	0	0	0	0	0	0	0	1	01H	0
20	SDRAM device attributes: /WE latency	0	0	0	0	0	0	0	1	01H	0
21	SDRAM device attributes	0	0	0	0	0	0	0	0	00H	
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0EH	
23	SDRAM cycle time at CL = 2 (2nd highest /CAS latency) (-7A/7AL)	0	1	1	1	0	1	0	1	75H	7.5ns
	(-75/75L, -80/80L)	1	0	1	0	0	0	0	0	A0H	10ns
24	SDRAM access from Clock at CL = 2 (2nd highest /CAS latency) (-7A/7AL)	0	1	0	1	0	1	0	0	54H	5.4ns
	(-75/75L, -80/80L)	0	1	1	0	0	0	0	0	60H	6ns
25 to 26		0	0	0	0	0	0	0	0	00H	
27	Minimum row precharge time (-7A/7AL)	0	0	0	0	1	1	1	1	0FH	15ns
	(-75/75L, -80/80L)	0	0	0	1	0	1	0	0	14H	20ns

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
28	Row active to row active min (-7A/7AL, -75/75L)	0	0	0	0	1	1	1	1	0FH	15ns
	(-80/80L)	0	0	0	1	0	0	0	0	10H	16ns
29	/RAS to /CAS delay min (-7A/7AL)	0	0	0	0	1	1	1	1	0FH	15ns
	(-75/75L, -80/80L)	0	0	0	1	0	1	0	0	14H	20ns
30	Minimum /RAS pulse width (-7A/7AL, -75/75L)	0	0	1	0	1	1	0	1	2DH	45ns
	(-80/80L)	0	0	1	1	0	0	0	0	30H	48ns
31	Density of each bank on module	0	0	1	0	0	0	0	0	20H	128MB
32	Address and command signal input setup time (-7A/7AL, -75/75L)	0	0	0	1	0	1	0	1	15H	1.5ns
	(-80/80L)	0	0	1	0	0	0	0	0	20H	2ns
33	Address and command signal input hold time (-7A/7AL, -75/75L)	0	0	0	0	1	0	0	0	08H	0.8ns
	(-80/80L)	0	0	0	1	0	0	0	0	10H	1ns
34	Data signal input setup time (-7A/7AL, -75/75L)	0	0	0	1	0	1	0	1	15H	1.5ns
	(-80/80L)	0	0	1	0	0	0	0	0	20H	2ns
35	Data signal input hold time (-7A/7AL, -75/75L)	0	0	0	0	1	0	0	0	08H	0.8ns
	(-80/80L)	0	0	0	1	0	0	0	0	10H	1ns
36 to 61	Superset information	0	0	0	0	0	0	0	0	00H	
62	SPD data revision code	0	0	0	1	0	0	1	0	12H	1.2
63	Checksum for Bytes 0 to 62 (-7A/7AL)	0	1	1	1	1	0	0	0	78H	
	(-75/75L)	1	0	1	1	1	0	0	1	B9H	
	(-80/80L)	1	1	1	1	1	0	1	0	FAH	
64	Manufacturer's JEDEC ID code	1	1	1	1	1	1	1	0	FEH	Elpida Memory
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00H	
72	Manufacturing location										
73 to 90	Manufacturer's part number										
91 to 92	Revision code										
93 to 94	Manufacturing date										
95 to 98	Assembly serial number										
99 to 125	Manufacturer specific data										
126	Reserved (Intel specification frequency)	0	1	1	0	0	1	0	0	64H	100MHz
127	Reserved (Intel specification /CAS# latency support)	1	1	0	0	0	1	1	1	C7H	

Block Diagram





Notes :
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

* D0 to D3 : EDS2516AP
U0 : 2k bits EEPROM
C100 to C123 : 0.1µF
N0 to N15 : Network resistors (10Ω)

Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power up, wait more than 100 µs and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to VDD + 0.5 (≤ 4.6 (max.))	V	
Supply voltage relative to VSS	VDD	–0.5 to +4.6	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	4	W	
Operating temperature	TA	0 to +70	°C	1
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. SDRAM device specification

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Operating Conditions (TA = 0 to +70°C) (SDRAM device specification)

Parameter	Symbol	min.	max.	Unit	Note
Supply voltage	VDD	3.0	3.6	V	1
	VSS	0	0	V	2
Input high voltage	VIH	2.0	VDD + 0.3	V	3
Input low voltage	VIL	–0.3	0.8	V	4

Notes: 1. The supply voltage with all VDD pins must be on the same level.
2. The supply voltage with all VSS pins must be on the same level.
3. VIH (max.) = VDD + 2.0V for pulse width ≤ 3ns at VDD.
4. VIL (min.) = VSS – 2.0V for pulse width ≤ 3ns at VSS.

DC Characteristics 1 (TA = 0 to +70°C, VDD = 3.3V ± 0.3V, VSS = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current	ICC1	-7A/7AL	540	mA	Burst length = 1 tRC = tRC (min.)	1, 2, 3
	ICC1	-75/75L	460	mA		
	ICC1	-80/80L	444	mA		
Standby current in power down	ICC2P		12	mA	CKE = VIL, tCK = 12ns	6
Standby current in non power down	ICC2N		80	mA	CKE, /CS = VIH, tCK = 12ns	4
Active standby current in power down	ICC3P		16	mA	CKE = VIL, tCK = 12ns	1, 2, 6
Active standby current in non power down	ICC3N		120	mA	CKE, /CS = VIH, tCK = 12ns	1, 2, 4
Burst operating current	ICC4		580	mA	tCK = tCK (min.), BL = 4	1, 2, 5
Refresh current	ICC5	-7A/7AL	1000	mA	tRC = tRC (min.)	3
	ICC5	-75/75L	880	mA		
	ICC5	-80/80L	850	mA		
Self refresh current	ICC6		12	mA	VIH ≥ VDD – 0.2V VIL ≤ 0.2V	7
Self refresh current (L-version)	ICC6	-XXL	4	mA		

Notes: 1. ICC depends on output load condition when the device is selected. ICC (max.) is specified at the output open condition
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, /CLK operating current.
7. After self refresh mode set, self refresh current.

DC Characteristics 2 (TA = 0 to +70°C, VDD = 3.3V ± 0.3V, VSS = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–8	8	µA	0 ≤ VIN ≤ VDD	
Output leakage current	ILO	–1.5	1.5	µA	0 ≤ VOUT ≤ VDD DQ = disable	
Output high voltage	VOH	2.4	—	V	IOH = –4mA	
Output low voltage	VOL	—	0.4	V	IOL = 4mA	

Pin Capacitance (TA = +25°C, VDD = 3.3V ± 0.3V)

Parameter	Symbol	Pins	max.	Unit	Notes
Input capacitance	CI1	Address	TBD	pF	1, 2, 4
	CI2	/RAS, /CAS, /WE	TBD	pF	1, 2, 4
	CI3	CKE	TBD	pF	1, 2, 4
	CI4	/CS	TBD	pF	1, 2, 4
	CI5	CLK	TBD	pF	1, 2, 4
	CI6	DQMB	TBD	pF	1, 2, 4
Data input/output capacitance	CI/O1	DQ	TBD	pF	1, 2, 3, 4

AC Characteristics (TA = 0 to +70°C, VDD = 3.3V ± 0.3V, VSS = 0V) (SDRAM device specification)

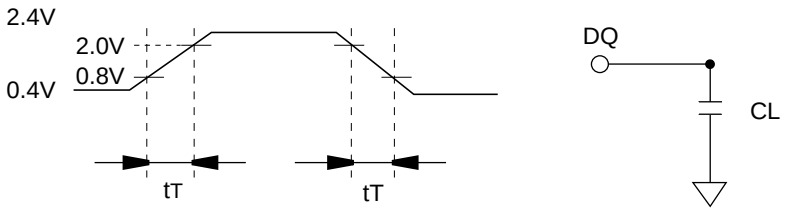
		-7A/7AL		-75/75L		-80/80L			
Parameter	Symbol	min.	max.	min.	max.	min.	max.	Unit	Notes
System clock cycle time (CL = 2)	tCK	7.5	—	10	—	10	—	ns	1
(CL = 3)	tCK	7.5	—	7.5	—	10	—	ns	
CLK high pulse width	tCH	2.5	—	2.5	—	3	—	ns	1
CLK low pulse width	tCL	2.5	—	2.5	—	3	—	ns	1
Access time from CLK	tAC	—	5.4	—	5.4	—	6	ns	1, 2
Data-out hold time	tOH	2.7	—	2.7	—	2.7	—	ns	1, 2
CLK to Data-out low impedance	tLZ	1	—	1	—	1	—	ns	1, 2, 3
CLK to Data-out high impedance	tHZ	—	5.4	—	5.4	—	6	ns	1, 4
Input setup time	tSI	1.5	—	1.5	—	2	—	ns	1
Input hold time	tHI	0.8	—	0.8	—	1	—	ns	1
Ref/Active to Ref/Active command period	tRC	60	—	67.5	—	70	—	ns	1
Active to Precharge command period	tRAS	45	120000	45	120000	48	120000	ns	1
Active command to column command (same bank)	tRCD	15	—	20	—	20	—	ns	1
Precharge to active command period	tRP	15	—	20	—	20	—	ns	1
Write recovery or data-in to precharge lead time	tDPL	15	—	15	—	20	—	ns	1
Last data into active latency	tDAL	2CLK + 15ns	—	2CLK + 20ns	—	2CLK + 20ns	—		
Active (a) to Active (b) command period	tRRD	15	—	15	—	20	—	ns	1
Transition time (rise and fall)	tT	0.5	5	0.5	5	0.5	5	ns	
Refresh period (8192 refresh cycles)	tREF	—	64	—	64	—	64	ms	

Notes: 1. AC measurement assumes tT = 0.5ns. Reference level for timing of input signals is 1.4V.

2. Access time is measured at 1.4V. Load condition is C_L = 50pF.
3. tLZ (min.) defines the time at which the outputs achieves the low impedance state.
4. tHZ (max.) defines the time at which the outputs achieves the high impedance state.

Test Conditions

- Input and output timing reference levels: 1.4V
- Input waveform and output load: See following figures



Input Waveform and Output Load

Relationship Between Frequency and Minimum Latency (SDRAM device specification)

Parameter		-7A/7AL	-75/75L	-80/80L	
Frequency (MHz)		133	133	10	
tCK (ns)		7.5	7.5	10	
/CAS latency	Symbol	CL = 2	CL = 3	CL = 2	Notes
Active command to column command (same bank)	IRCD	2	3	2	1
Active command to active command (same bank)	IRC	8	9	7	1
Active command to precharge command (same bank)	IRAS	6	6	5	1
Precharge command to active command (same bank)	IRP	2	3	2	1
Write recovery or data-in to precharge command (same bank)	IDPL	2	2	2	1
Active command to active command (different bank)	IRRD	2	2	2	1
Self refresh exit time	ISREX	1	1	1	2
Last data in to active command (Auto precharge, same bank)	IDAL	4	5	4	= [IDPL + IRP]
Self refresh exit to command input	ISEC	8	9	7	= [IRC] 3
Precharge command to high impedance	IHZP	2	3	2	
Last data out to active command (auto precharge) (same bank)	IAPR	1	1	1	
Last data out to precharge (early precharge)	IEP	–1	–2	–1	
Column command to column command	ICCD	1	1	1	
Write command to data in latency	IWCD	0	0	0	
DQM to data in	IDID	0	0	0	
DQM to data out	IDOD	2	2	2	
CKE to CLK disable	ICLE	1	1	1	
Register set to active command	IMRD	2	2	2	
/CS to command disable	ICDD	0	0	0	
Power down exit to command input	IPEC	1	1	1	

Notes: 1. IRCD to IRRD are recommended value.
2. Be valid [DESL] or [NOP] at next command of self refresh exit.
3. Except [DESL] and [NOP]

Pin Functions

CLK0, CLK1 (input pin): CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.

/CS0 (input pin): When /CS is Low, the command input cycle becomes valid. When /CS is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS and /WE (input pins): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A12 (input pins): Row address (AX0 to AX12) is determined by A0 to A12 level at the bank active command cycle CLK rising edge. Column address (AY0 to AY8) is determined by A0 to A8 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 and BA1 (BA) is precharged.

BA0 and BA1 (input pin)

BA0 and BA1 are bank select signal (BA). (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL. ×: VIH or VIL

CKE0 (input pin): This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQMB0 to DQMB7 (input pins): Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z.

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.

DQ0 to DQ63 (input/output pins): Data is input to and output from these pins.

VDD (power supply pins): 3.3V is applied.

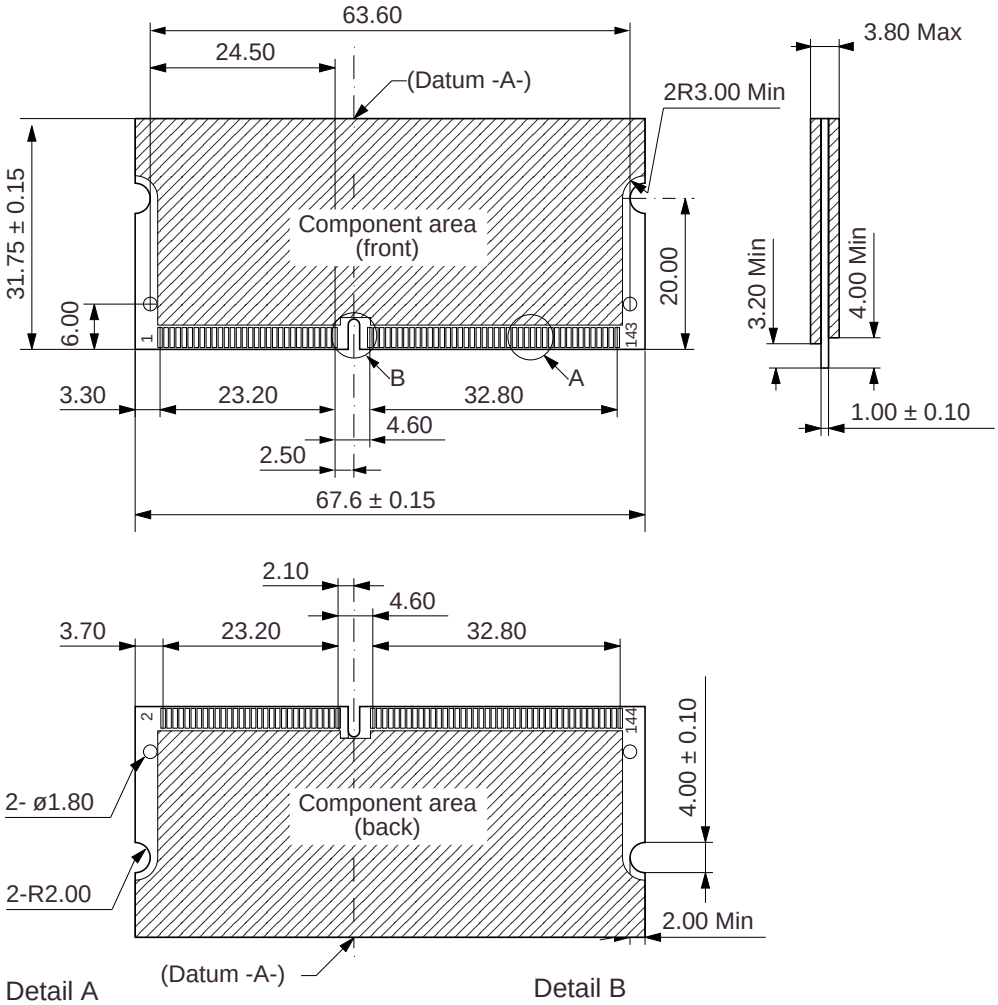
VSS (power supply pins): Ground is connected.

Detailed Operation Part

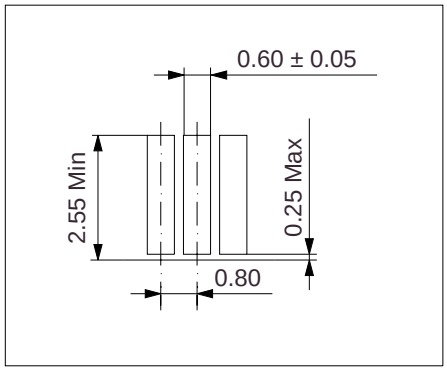
Refer to the EDS2504AC/08AC/16AC, EDS2504AP/08AP/16AP datasheet (E0110E).

Physical Outline

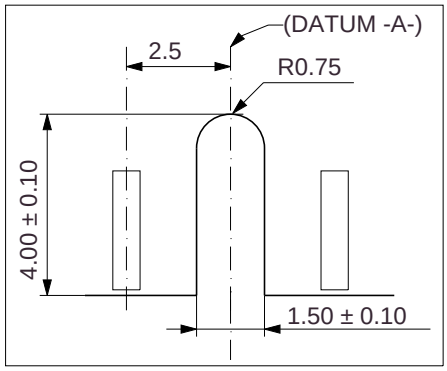
Unit:mm



Detail A



Detail B



ECA-TS2-0047-01

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0107

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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