# Edge749
# Octal Pin Electronics Driver/Receiver

TEST AND MEASUREMENT PRODUCTS

## Description

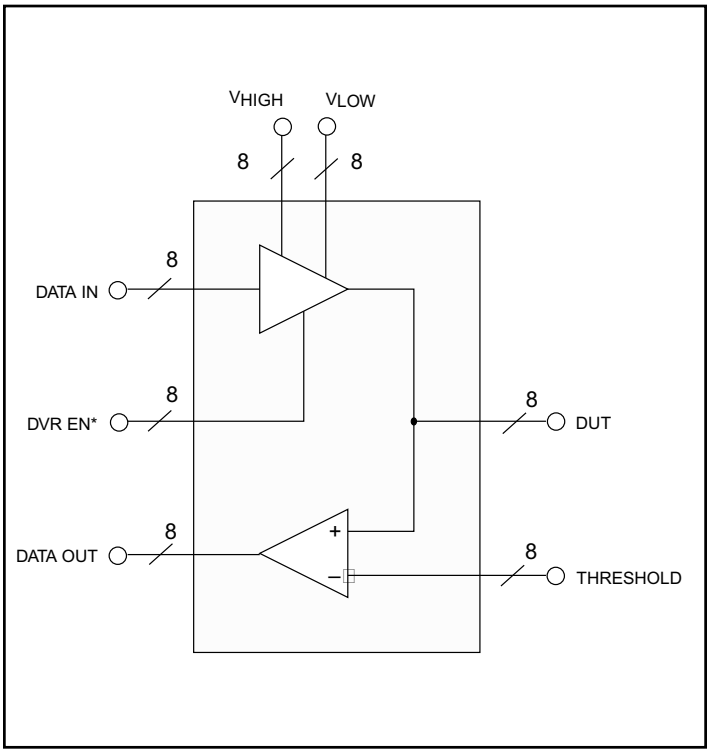
The Edge749 is an octal pin electronics driver and receiver combination fabricated in a high-performance CMOS process. It is designed for automatic test equipment and instrumentation where cost, functional density, and power are all at a premium.

The Edge749 incorporates eight channels of programmable drivers and receivers into one package. Each channel has per pin driver levels, receiver threshold, and tristate control.

The 18V driver output and receiver input range allows the Edge749 to interface directly between TTL, ECL, CMOS (3V, 5V, and 8V), very high voltage, and custom level circuitry.

The Edge749 is pin and functionally compatible with the Edge648 and Edge649.

## Functional Block Diagram




## Features

- 20 MHz Operation
- 18 V DUT I/O Range
- Programmable Output Levels
- Programmable Input Thresholds
- Per Pin Flexibility
- High Integration Levels
- Low Power Dissipation
- Edge 648 and 649 Compatible

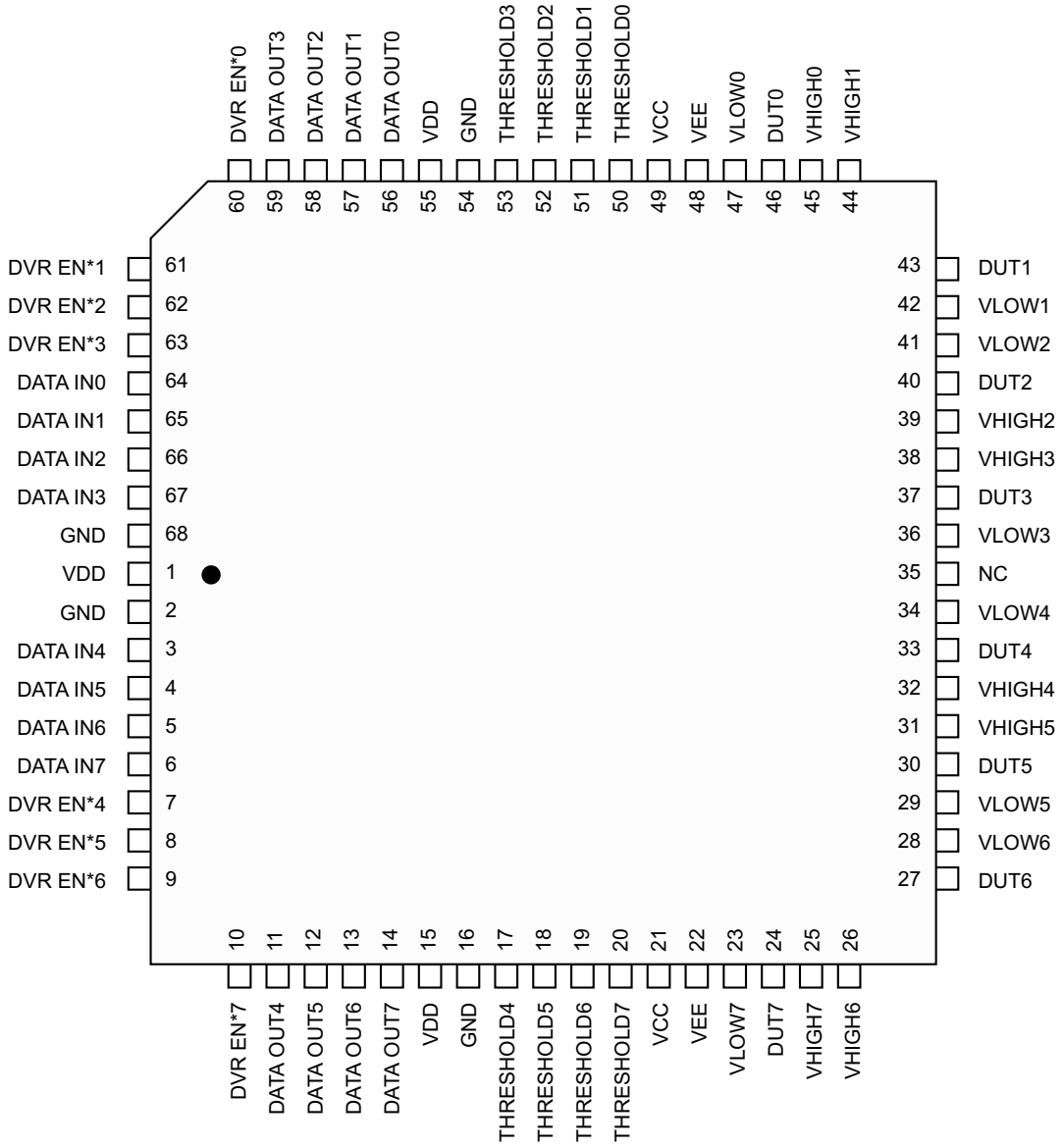
## Applications

- Burn-In ATE
- Functional Board Testers
- In-Circuit Board Testers
- Combinational Board Testers
- Low Cost Chip Testers
- ASIC Verifiers
- VXI-Based Test Equipment

## PIN Description

| Pin Name | Pin Number | Description |
|---|---|---|
| DATA IN (0:7) | 64, 65, 66, 67, 3, 4, 5, 6 | TTL compatible inputs that determine the high/low status of the DUT drivers. |
| DATA OUT (0:7) | 56, 57, 58, 59, 11, 12, 13, 14 | CMOS level outputs that indicate the status of the DUT receivers. |
| DUT (0:7) | 46, 43, 40, 37, 33, 30, 27, 24 | Pin electronic inputs/outputs that receive/drive the device under test. |
| DVR EN (0:7) | 60, 61, 62, 63, 7, 8, 9, 10 | TTl compatible inputs that control the high impedance state of the DUT drivers. |
| VHIGH (0:7) | 45, 44, 39, 38, 32, 31, 26, 25 | Unbuffered analog inputs that set the voltage level of a logical 1 of the DUT drivers. |
| VLOW (0:7) | 47, 42, 41, 36, 34, 29, 28, 23 | Unbuffered analog inputs that set the voltage level of a logical 0 of the DUT drivers. |
| THRESHOLD (0:7) | 50, 51, 52, 53, 17, 18, 19, 20 | Buffered analog input voltage that sets the threshold for the DUT comparators. |
| VCC | 21, 49 | Analog positive power supply. |
| VEE | 22, 48 | Analog negative power supply. |
| VDD | 1, 15, 55 | Digital power supply. |
| GND | 2, 16, 54, 68 | Device ground. |
| N/C | 35 | No connection. |

## PIN Description *(continued)*



## Circuit Description

### Driver Description

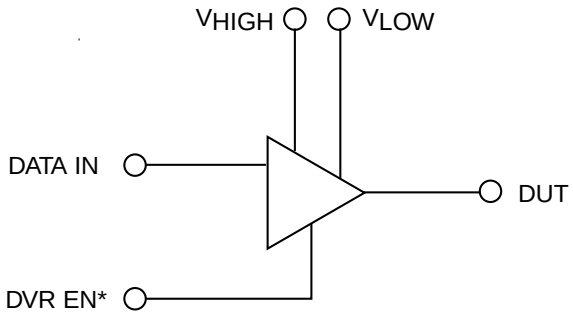



***Figure 1. Driver Diagram***

As shown in Figure 1, Edge749 supports programmable high and low levels and tristate per channel. There are no shared lines between any drivers. The DVR EN* and DATA IN signals are TTL compatible inputs that control the driver (see Figure 2).

With DVR EN* high, the DUT driver goes into a high impedance state. With DVR EN* low, DATA IN high forces the driver into a high state (DUT = $V_{HIGH}$), and DATA IN low forces the driver low (DUT = $V_{LOW}$).

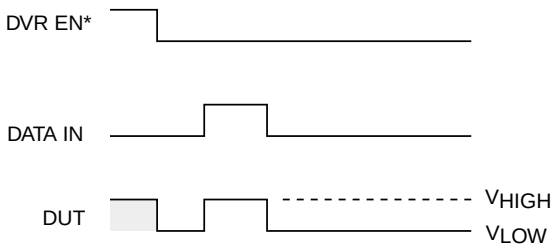



***Figure 2. Driver Functionality***

### $V_{HIGH}$ and $V_{LOW}$

$V_{HIGH}$ and $V_{LOW}$ define the logical “1” and “0” levels of the DUT driver and can be adjusted anywhere over the range determined by VCC and VEE. Table 1 documents the relationship between the analog power to supplies (VCC and VEE), the driver range ($V_{HIGH}$ and $V_{LOW}$), and the comparator threshold range ($V_{THRESHOLD}$).

The $V_{HIGH}$ and $V_{LOW}$ inputs are unbuffered in that they also provide the driver output current (see Figure 3), so the source of $V_{HIGH}$ and $V_{LOW}$ must have ample current drive capability.

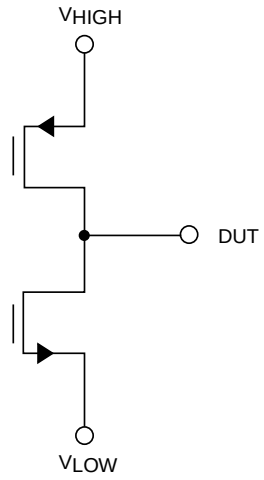



***Figure 3. Simplified Model of the Unbuffered Output Stage***

| Drive Common Mode Range | Receive Common Mode Range | Threshold Range |
|---|---|---|
| VEE <= DUT <= VCC | VEE <= DUT <= VCC | VEE + 3V <= THRESHOLD <= VOC - 3V |

***Table 1. Headroom vs. Power Supplies***

### Driver Output Protection

In a functional testing environment, where a resistor is added in series with the driver output (to create a 50Ω output impedance), the Edge749 can withstand a short to any legal DUT voltage for an indefinite amount of time.

In a low impedance application with no additional output series resistance, care must be exercised and systems should be designed to check for this condition and tristate the driver if a short is detected.

### Receiver Functionality

Edge749 supports programmable thresholds per channel. There are no shared lines between comparators. THRESHOLD is a high input impedance analog input which defines a logical "1" and "0" at the DUT (see Figure 4). If the DUT voltage is more positive than THRESHOLD, DATA OUT will be high. With DUT lower than THRESHOLD, DATA OUT will be low.

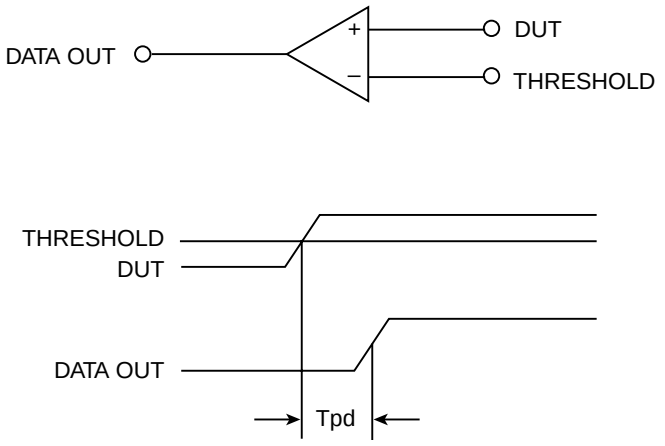



***Figure 4. Receiver Functionality***

## Application Information

### Power Supplies

The Edge749 uses three power supplies: VDD, VCC and VEE. VDD is the digital supply for all of the data inputs and outputs. VCC and VEE are the analog power supplies for the Edge749 drivers and comparators. In order to protect the Edge749 and avoid damaging it, the following power supply requirements must be satisifed at all times:

$$VEE \le GND \le VDD \le VCC$$

Also, $VEE \le$ All Inputs $\le VCC$ at all times

The three-Schottky diode configuration shown in Figure 5, used on a once-per-board basis, insures power supply sequence and fault tolerance.

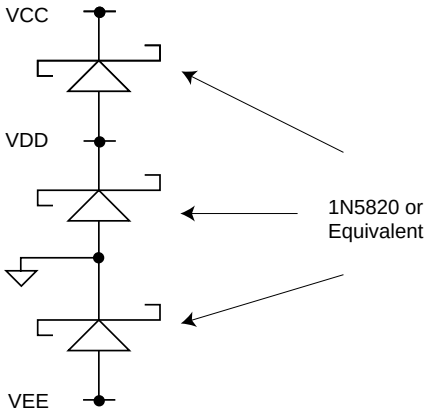



***Figure 5. Power Supply Protection Scheme***

| *Power-On Sequencing* | *Power-Off Sequencing* |
|---|---|
| 1. VCC (substrate) | 1. Inputs |
| 2. VEE | 2. VDD |
| 3. VDD | 3. VEE |
| 4. Inputs | 4. VCC |

### Power Supplies Decoupling

VDD, which provides the digital power, should be decoupled to GND with a .1 µF chip capacitor in parallel with a .001 µF chip capacitor. The bypass capacitors should be as close to the device as possible. Power and ground planes are recommended to provide a low inductance return path.

VCC and VEE, which power the DUT drivers and receivers, should also be decoupled to GND with a .1 µF chip capacitor in parallel with a .001 µF chip capacitor. A VCC and VEE plane, or at least a solid power bus, is recommended for optimal performance.

### $V_{HIGH}$ and $V_{LOW}$ Decoupling

As the $V_{HIGH}$ and $V_{LOW}$ inputs are unbuffered and must supply the driver output current, decoupling capacitors for these inputs are recommended in proportion to the amount of output current the application requires.

### Expanding the Common Mode Range

Although the Edge749 can drive and receive 18 V swings, these 18 V signals can be adjusted over an 21 V range. By using programmable regulators V1 and V2 for the VCC and VEE supplies (feasible because these two analog power supplies do not supply driver output current), the Edge749 I/O range can be optimized for a variety of applications (see Figure 6).

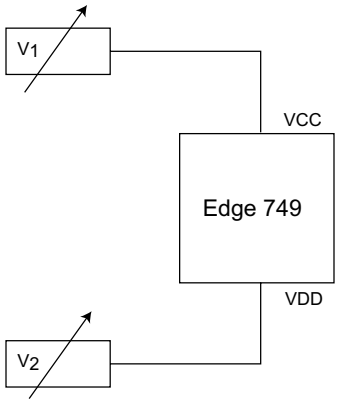



***Figure 6.***

There are three rules which govern the supplies V1 and V2:

1) $+10V < V1 < +18V$
2) $-3V < V2 < 0V$
3) $(V1 - V2) < +18V$.

### Window Comparator

Certain applications require a dual threshold window comparator to distinguish between the DUT being high, low, or floating. To support this application, two Edge749 channels can be combined to create one channel with a window comparator (see Figure 7). Notice that connecting two DUT pins ties together the positive inputs of both receivers. The result is a difference in polarity between the digital outputs reporting the high and low status of the DUT.

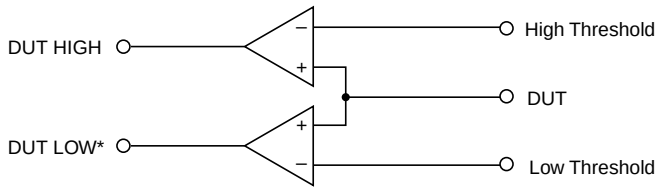



***Figure 7. Edge749 as a Window Comparator***

Once two receivers are connected as window comparators, the two drivers also get connected in parallel. This dual driver configuration supports a multitude of applications that have traditionally been difficult to accommodate.

### Trinary Driver

At times, there is a need for a three-level driver. Typically, two levels are required for the standard digital "1" and "0" pattern generation. The third level provides a higher voltage to place the device under test (DUT) into a programming or test mode. By controlling the DATA IN and DVR EN* inputs, a trinary driver with tristate is realizable (see Figure 8).

### Driver with Pull Up/Pull Down

As the drivers are unbuffered, paralleling two drivers for one DUT node provides a means for adding pull up or pull down capability. By connecting the $V_{HIGH}$ and $V_{LOW}$ inputs of one driver through a resistor to a voltage, additional functionality that would normally require an external relay on the DUT transmission line to engage and disengage these functions is realizable.

One common application for the pull up feature is testing open collector devices. The pull down satisfies open emitter DUTs (typically ECL). Either the pull up or down could be used to establish a default high impedance voltage on a bidirectional bus. Notice that in all applications, the resistors can be switched dynamically or statically.

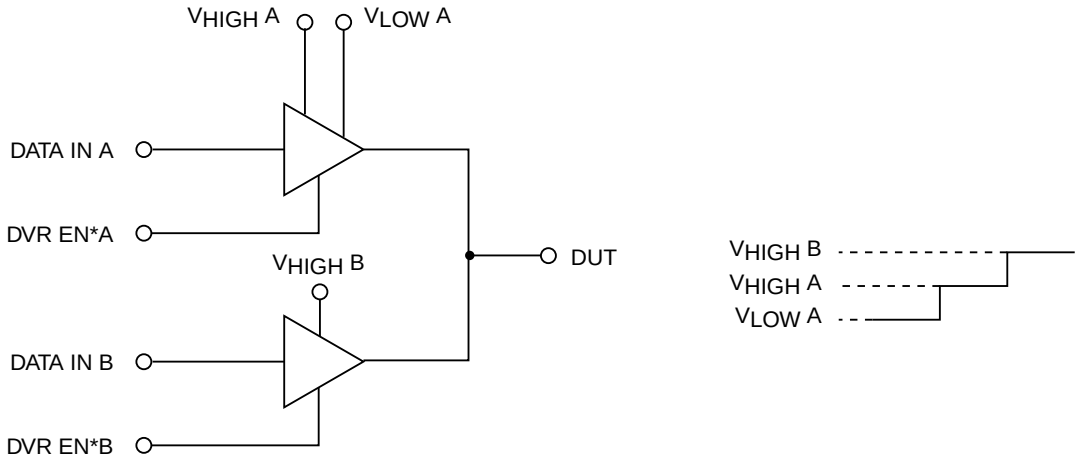



***Figure 8. Trinary Driver***

## Application Information *(continued)*

Also, either the pull up or pull down resistor could be used to terminate the transmission from the DUT to the pin electronics in an effort to minimize any reflections.

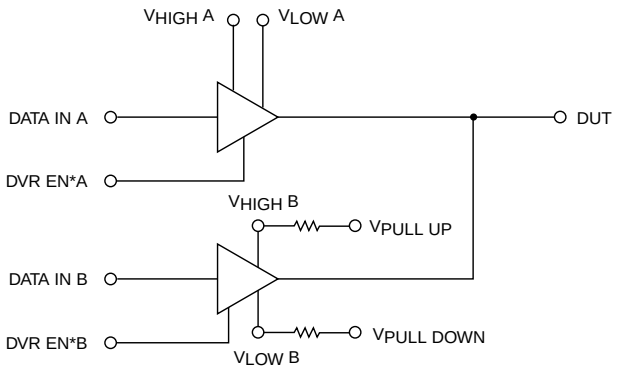



***Figure 9. Driver with Pull Up/Pull Down***

### Trinary Driver with Termination

Other combinations are also possible. For example, two parallel drivers can be configured to implement one trinary driver with a pull down (or pull up) dynamic termination (see Figure 10).

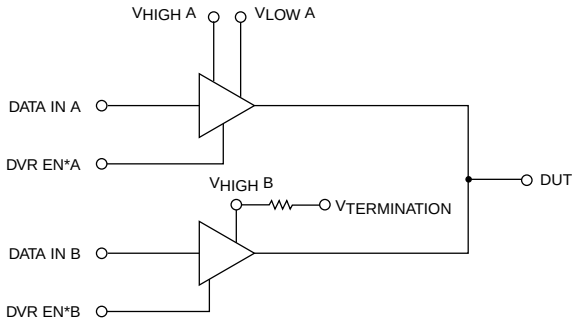



***Figure 10. Trinary Driver with Termination***

### Two Logic Family Driver

Many test systems support exactly two families of driver and receiver levels and select between family A and family B settings on a per-pin basis, typically using an analog multiplexer (See Figure 11). Common examples of these families are:

Family A = TTL
Family B = CMOS
or
Family A = TTL
Family B = ECL

The Edge749 supports this system architecture with minimal hardware and the elimination of the per-pin analog multiplexer. The drive and receive levels need to be generated once per system, then distributed and buffered suitably.

### Parametric Functions

Two drivers in parallel also offer the possibility of connecting force and sense parametric circuitry to the DUT without adding additional circuitry to the controlled impedance DUT line. For example, Figure 12 shows the second driver being utilized to force a current and measure a voltage.

Notice that the $V_{HIGH}$ and $V_{LOW}$ pins are used from different drivers to allow the force and sense functions to be active simultaneously.

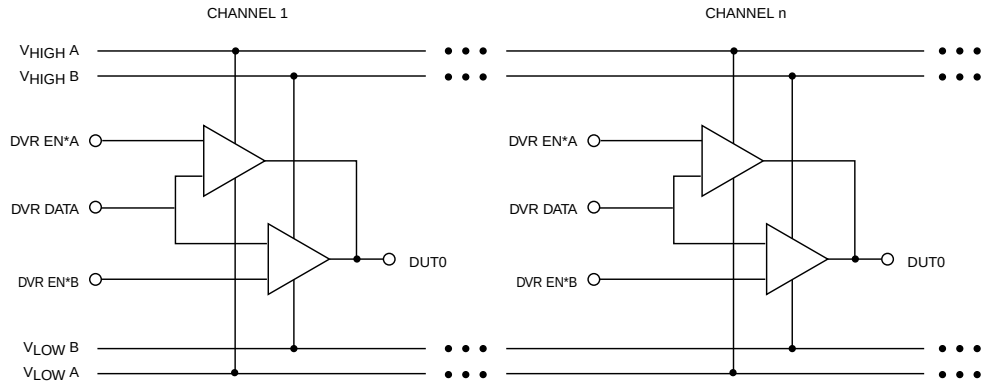



***Figure 11. Family A/B Using Two Drivers Per Pin***

### Driver Output Impedance

Ideally, a driver would have a constant output impedance over all ouptut conditions. However, the Edge749 ouptut impedance does vary slightly over the common mode drive level and whether it is driving high or low. Figure 12 shows the variation in Rout.

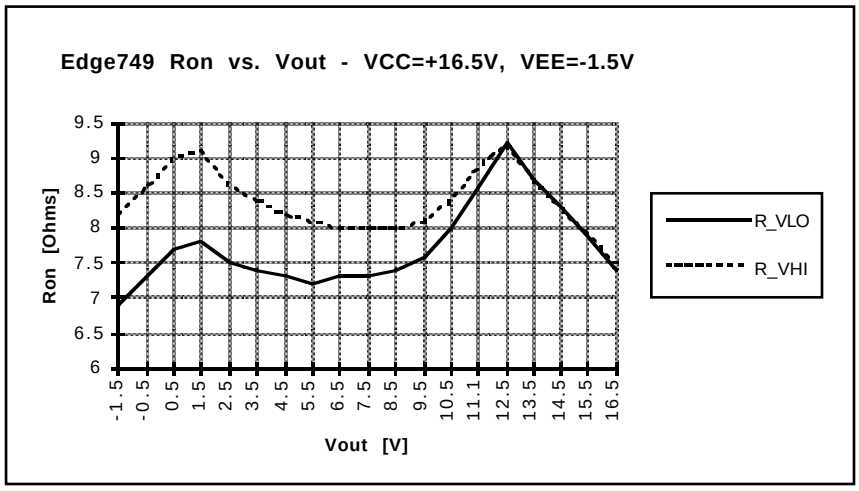



***Figure 12. ROUT vs. DOUT***

### High Impedance Leakage

The Edge749 is designed to be extremely low leakage (see Figure 13.) In a low performance application, where the output capacitance is not a concern, the low leakage may allow the elimination of an isolation relay.

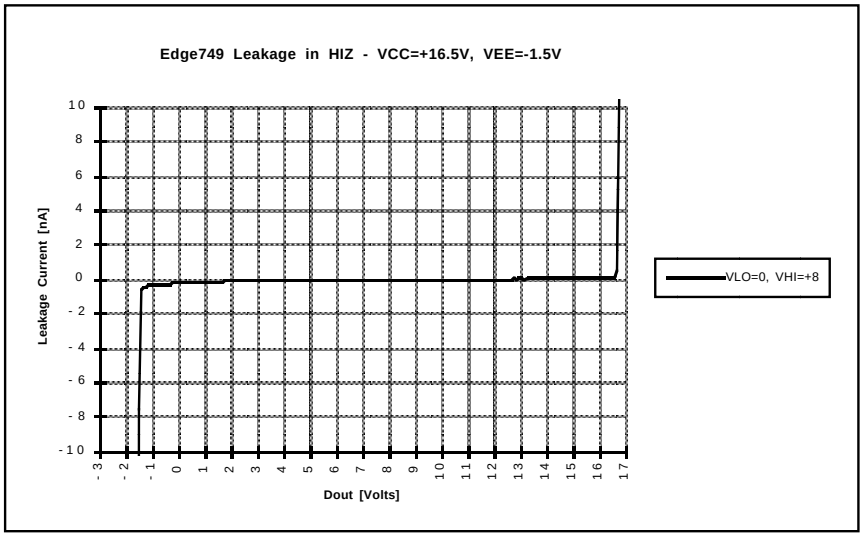
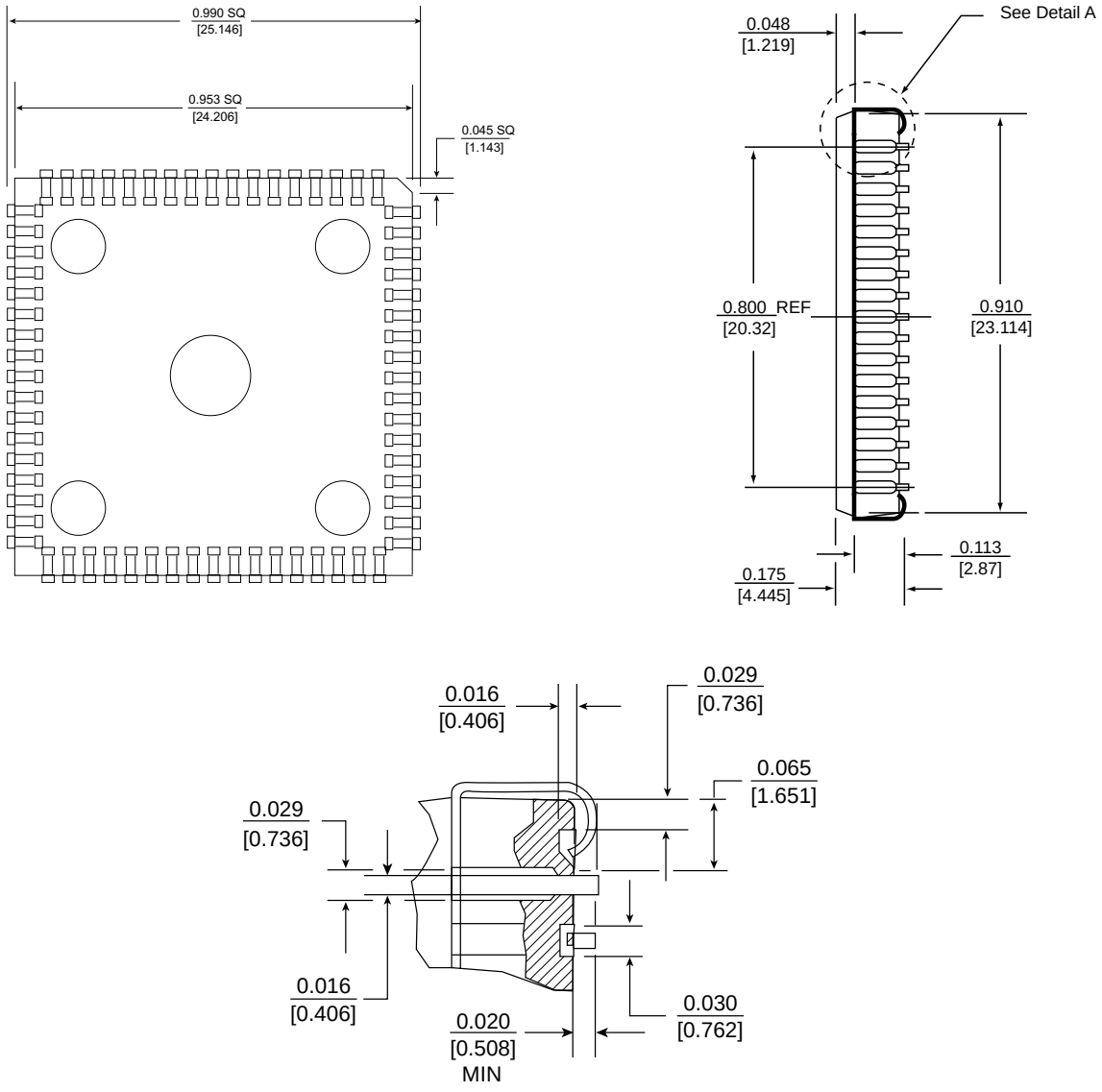



***Figure 13. High Impedance Leakage***

**68 Pin PLCC Package**
**θJA = 42 to 48˚C / W**




Notes: (unless otherwise specified)
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Digital Power Supply | VDD | 4.5 | 5 | 5.5 | V |
| Analog Positive Power Supply | VCC | 10 | 15 | 18 | V |
| Analog Negative Power Supply | VEE | -3 | -2 | 0 | V |
| Total Analog Power Supply | VCC - VEE | 10 | | 18 | V |
| Driver High Output Voltage | $V_{HIGH}$ | VEE | | VCC | V |
| Driver Low Output Voltage | $V_{LOW}$ | VEE | | VCC | V |
| Total Driver Output Swing | $V_{HIGH}$ - $V_{LOW}$ | -18 | | 18 | V |
| Receiver Threshold Voltage | THRESHOLD | VEE + 3 | | VCC - 3 | V |
| Ambient Operating Temperature | TA<br>TJ | 0<br>0 | | +70<br>+125 | °C<br>°C |

## Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Total Analog Power Supply | VCC - VEE | | | 19 | V |
| Positive Analog Power Supply | VCC | -.5 | | 19 | V |
| Negative Analog Power Supply | VEE | -5 | | 0.5 | V |
| Driver High Output Voltage | $V_{HIGH}$ | VEE - .5 | | VCC + .5 | V |
| Driver Low Output Voltage | $V_{LOW}$ | VEE - .5 | | VCC + .5 | V |
| Driver Output Swing | $V_{HIGH}$ - $V_{LOW}$ | -18.5 | | 18.5 | V |
| Receiver Threshold Voltage | THRESHOLD | VEE - .5 | | VCC + .5 | V |
| Digital Inputs | DATA IN<br>DVR EN* | GND - .5 | | VDD + .5 | V |
| Digital Power Supply | VDD | 0 | | 6.5 | V |
| Ambient Operating Temperature | TA | -55 | | +125 | °C |
| Storage Temperature | TS | -65 | | +150 | °C |
| Junction Temperature | TJ | | | +150 | °C |
| Soldering Temperature | TSOL | | | 260 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## DC Characteristics

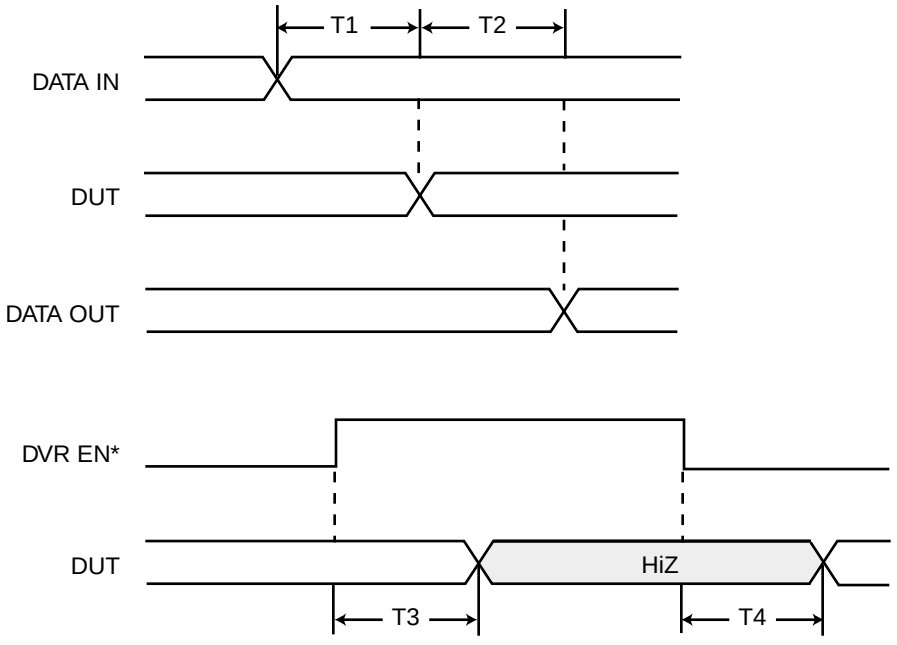
| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***Driver/Receiver Characteristics*** | | | | | |
| Output Voltage Swing | $V_{HIGH}$ - $V_{LOW}$ | -18 | | 18 | V |
| DC Driver Output Current (Note 1) | $I_{OUT}$ | -125 | | +125 | mA |
| Output Impedance (Note 2) | $R_{OUT}$ | 4 | 8 | 12 | Ω |
| DUT Pin Capacitance | $C_{OUT}$ | | 20 | | pF |
| DUT Output voltage | DUT<0:7> | VEE | | VCC | V |
| Receiver Threshold Level | $V_{THRESHOLD}$ | VEE + 3 | | VCC - 3 | V |
| Threshold Bias Current | | | 0 | 1.0 | µA |
| DUT Leakage Input Current | $I_{BIAS}$ | | .001 | 1.0 | µA |
| Receiver Offset Voltage (Note 3) | VOS | -200 | | 200 | mV |
| Quiescent Power Supply Current | | | | | |
| Positive Power Supply | ICC | | 60 | 80 | mA |
| Negative Power Supply | IEE | -60 | -40 | | mA |
| Digital Power Supply | IDD | | 5 | 15 | mA |
| ***Digital Inputs*** ***DATA IN (0:7), DVR EN* (0:7)*** | | | | | |
| Input High Voltage | $VIH_{MIN}$ | 2.0 | | VDD | V |
| Input Low Voltage | $VIL_{MAX}$ | 0 | | 0.8 | V |
| Input Current | $I_{IN}$ | | | 1.0 | µA |
| Input Capacitance | $C_{IN}$ | | 5 | | pF |
| ***Digital Outputs*** ***DATA OUT (0:7)*** | | | | | |
| Output Voltage High (Note 4) | VOH | VDD - .4 | | VDD + .4 | V |
| Output Voltage Low (Note 5) | VOL | -0.4 | 0 | 0.4 | V |
| DC Output current | $I_{OUT}$ | | | 4 | mA |

*Note 1 :* Output current specification is per individual driver.
*Note 2 :* Tested for driving a high state and low state at +18V, +6V, and 0V.
*Note 3 :* Measured at THRESHOLD = +1.5V.
*Note 4:* Output current of –4 mA.
*Note 5:* Output current of 4 mA.

## AC Characteristics

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Propagation Delay | | | | | |
| DATA IN <0:7> to DUT <0:7> | T1 | 20 | 29 | 38 | ns |
| DUT <0:7> to DATA OUT <0:7> | T2 | 10 | 21 | 30 | ns |
| Active to HiZ | T3 | 20 | 32 | 40 | ns |
| HiZ to Active | T4 | 20 | 28 | 35 | ns |
| DUT Output Rise/Fall Times (Note 1) | | | | | |
| 1V Swing (20% - 80%) | | | 1.0 | | ns |
| 3V Swing (10% - 90%) | | | 1.5 | | ns |
| 5V Swing (10% - 90%) | | | 1.5 | | ns |
| 8V Swing (10% - 90%) | | | 1.5 | | ns |
| 10V Swing (10% - 90%) | | | 1.5 | | ns |
| Digital Outputs (DATA OUT <0:7>) | | | | | |
| DATA OUT Rise Time (10% - 90%) | TR | | 2.5 | | ns |
| DATA OUT Fall Time (10% - 90%) | TF | | 2.5 | | ns |
| Minimum Pulse Width | | | | | |
| Driver Output | | 25 | 20 | | ns |
| Comparator Output | | 20 | 15 | | ns |
| Maximum Operating Frequency | Fmax | 15 | 20 | | MHz |

*Note 1:* Into 18 inches of 50Ω transmission line terminated with 1KΩ and 5 pF with the proper series termination resistor.



## Ordering Information

| Model Number | Package |
|---|---|
| E749BPJ | 68-Pin PLCC |
| EVM749EVM | Edge749 Evaluation Module |

## Contact Infor mation

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## Revision History

**Current Revision Date:** October 21, 2002
**Previous Revision Date:** June 11, 2002

| Page # | Section Name | Previous Revision | Current Revision |
|---|---|---|---|
| 6 | Power Supplies | | Para 1 rewritten<br>Para 2 deleted<br>Power On and Off Sequencing added |

**Current Revision Date:** June 11, 2002
**Previous Revision Date:** June 23, 1998

| Page # | Section Name | Previous Revision | Current Revision |
|---|---|---|---|
| 2 | Pin Descriptions | VLOW | Change Pin #44 to Pin #47 |