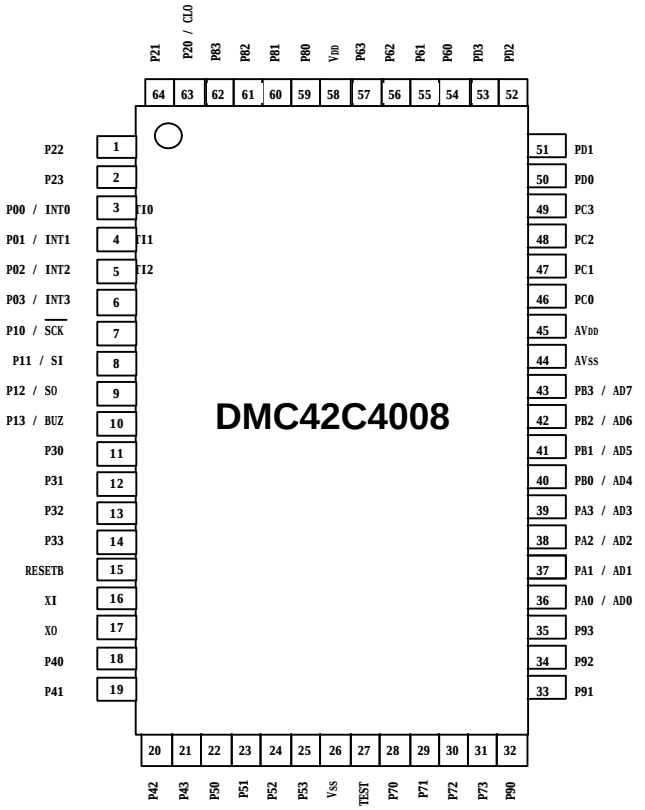
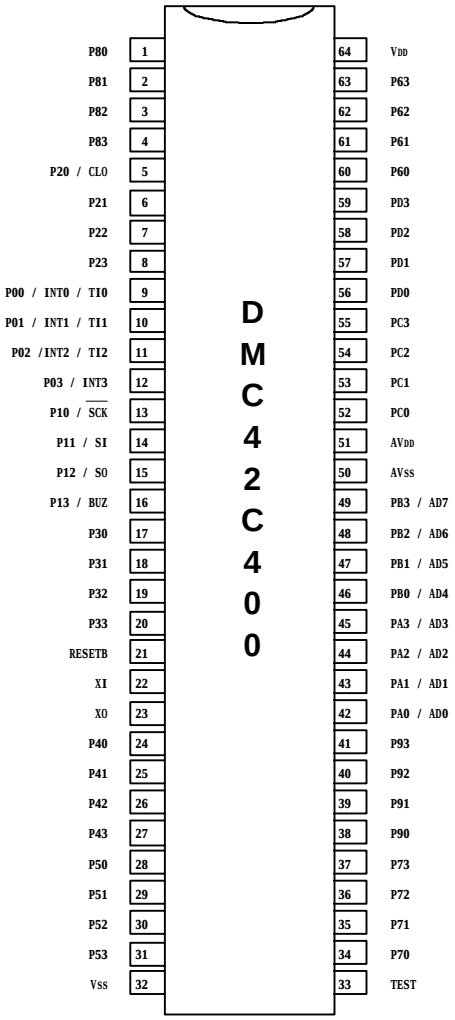
DESCRIPTION

The DMC42C4008 is a 4-bit single chip microcomputer having 8K bytes ROM and is designed with CMOS silicon gate technology. The DMC42C4008 includes peripherals such as various timers, A/D converter(8ch), serial communication interface(8bit), on-chip oscillator and clock circuit. It provides the hardware features, architectural enhancements and instructions which are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of programmable memory.

PIN CONFIGURATIONS





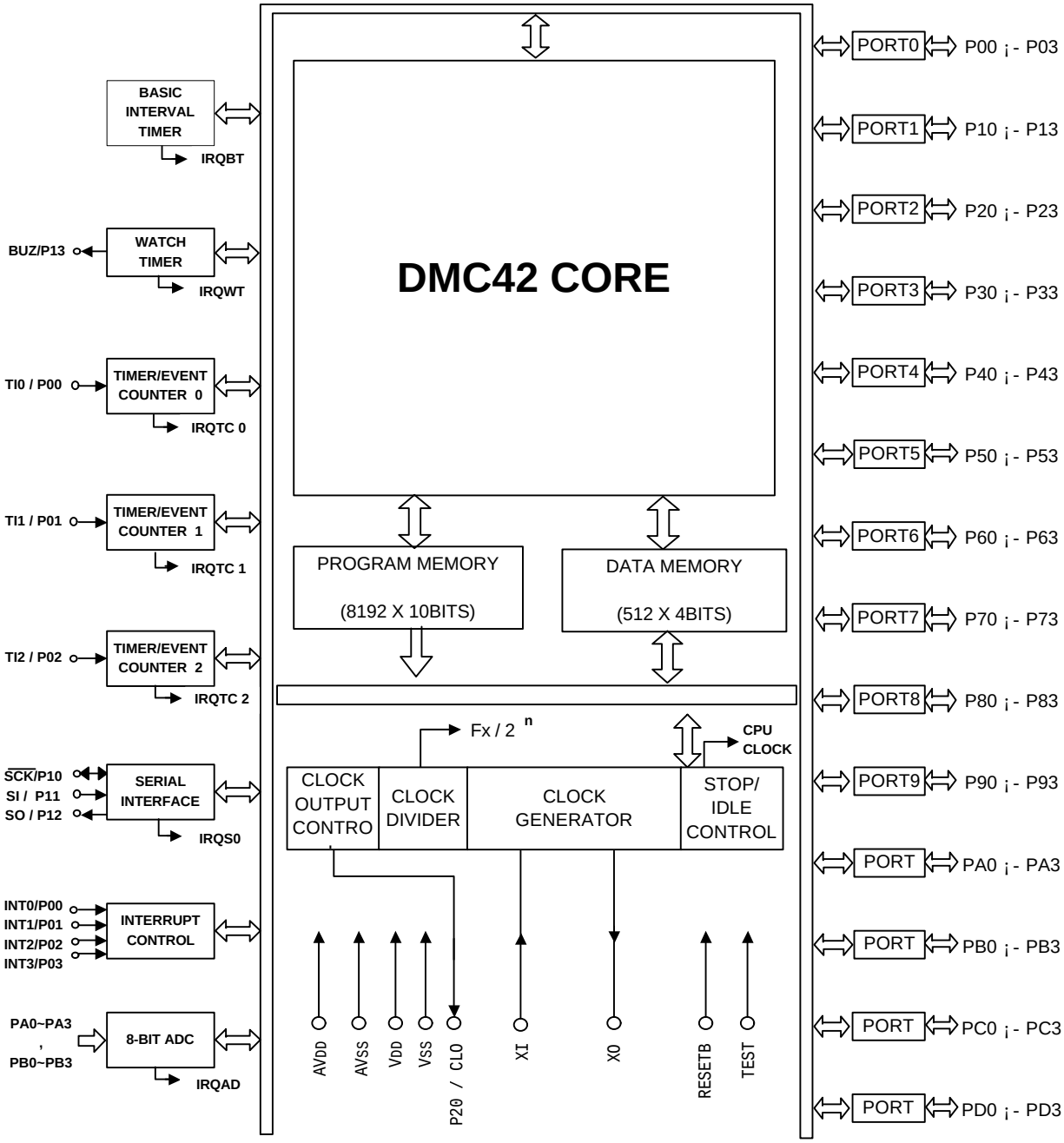
FEATURE

- Memory mapped I/O
- Program memory : 8192 x 10bits
- Data memory : 512 x 4bits
- Instructions
  - Various bit manipulation
  - 8-bit data operation
  - 7-bit relative branch
  - 1 byte absolute call
- Instruction cycle times
  - Main (XI = 4.19MHz)
    . 15.3 us (XI/64 = 65.5KHz)
    . 1.91 us (XI/8 = 524.0KHz)
    . 0.95 us (XI/4 = 1.05MHz)
- 4 Register Bank
- General register : 8 x 4-bit respectively
- Accumulator
  - Bit Accumulator (CY), 4 bit Accumulator (A), 8 bit Accumulator (XA)
- Multiple vectored interrupt source
  - External interrupt : 4
  - Internal interrupt : 7
- Watch timer
  - fast mode : 3.91 msec
  - normal mode : 0.5 sec
  - buzzer output : 1, 2, 4 KHz
- Basic interval timer
  - 8 kinds of period
  - Used stabilization wait timer to wake up Stop mode
- Three 8-bit timer / event counters
- 8-bit serial communication interface
  - External / Internal clock selection
  - Mode : Transmit ·Receive
    Receive only
    Clock continuous
- 8-bit A/D converter
  - 8-bit successive approximate type
  - 8 channels
  - Sample and hold
  - Conversion time : 17.1 us at 4.19MHz
- Key scan
  - 4, 6, 8 Pins Selectable : Port 4, 5
  - Falling edge operation
- 56 I/O Ports
  - CMOS Ports : 40
  - N-channel open drain Ports : 16
  - Direct LED drive
  - Internal pull-up resistor (Mask option)
- Power saving mode
  - STOP : Main clock, CPU clock stop
  - STBY : Only CPU clock stop
    Main clock operation
- Package : 64 QFP, 64 SDIP

APPLICATION

VTR, Audio, Telephone, Printer, Refrigerator
Fan Heater, Washing Machine

BLOCK DIAGRAM



PROGRAM MEMORY (ROM)

	CONTENTS
0000H	VECTOR ADDRESS AREA
001FH	
0020H	ZERO-PAGE CALL AREA
005FH	
0060H	**8K Byte**
1FFFH	

VECTOR ADDRESS

	Prioty	INTERRUPT SUORCE	
0000H	0	RESET	Reset Signal
0002H	1	IRQBT	Basic Interval Timer
0004H	2	IRQ0	External interrupt 0
0006H	3	IRQ1	External interrupt 1
0008H	4	IRQTC0	Timer Event Counter 0
000AH	5	IRQTC1	Timer Event Counter 1
000CH	6	IRQ2	External interrupt 2
000EH	7	IRQTC2	Timer Event Counter 2
0010H	8	IRQ3	External interrupt 3
0012H	9	IRQS0	Serial I/O 0
0014H	10	IRQAD	8 bit ADC
0016H			
0018H	12	IRQWT	Watch Timer
001AH	13	IRQKS	Key Scan
001CH			
001EH	15	-	reserved

DATA MEMORY (RAM)

		DIRECT	INDIRECT			STACK	GENERAL REGISTER	
		m	@HL		@DE @DL			
	$00 PAGE0 (256 Byte) $FF			**MP=0**		**SPS=0**	**RB=0 RB=2**	**RB=1 RB=4**
	$00 PAGE1 (256 Byte) $FF	**MB=0**	**MB=0**	**MP=1**		**SPS=1**		
BANK 0 (1K)	$00 PAGE2 (256 Byte) $FF			**MP=2**		**SPS=2**		
	$00 PAGE3 (256 Byte) $FF	**I/O MEMORY**		**MP=3**				

; Usable

I/O ADDRESS MAP

ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL
	b3	b2	b1	b0		1 bit	4 bit	8bit		VALUE
318H	Stack pointer low (SPL)				R/W			O	Stack pointer low	E
319H	Stack pointer high (SPH)				R/W			O	stack pointer high	F
31AH	SP3	SP2	SP1	SP0	R/W			O	Stack Page Select Low (SPSL)	0
31BH	-	-	SP5	SP4	R/W			O	Stack Page Select High (SPSh)	0
31CH	AC		IS1	IS0	R/W	O	O	O	Psw low (PSWL)	0
31DH	CY	Z	OV	T					Psw high (PSWH)	0
320H 321H	T/E counter mode register 0 (TMOD0)				W	320H.3		O	Clock source select. counter start (ch0)	00
322H 323H	T/E counter register 0 (TMCNT0)				R			O	readable count value (ch0)	00
324H 325H	T/E reference register 0 (TMREF0)				W			O	count reference register (ch0)	FF
326H 327H	T/E counter mode register 1 (TMOD1)				W	326H.3		O	clock source select. counter start (ch1)	00
328H 329H	T/E counter register 1 (TMCNT1)				R			O	readable count value (ch1)	00
32AH 32BH	T/E reference register 1 (TMREF1)				W			O	count reference register (ch1)	FF
32CH 32DH	T/E counter mode register 2 (TMOD2)				W	32CH.3		O	clock source select. counter start (ch2)	00
32EH 32FH	T/E counter register 2 (TMCNT2)				R			O	readable count value (ch2)	00
330H 331H	T/E reference register 2 (TMREF2)				W			O	count reference register (ch2)	FF
332H	Basic Timer mode register(BMOD)				R/W	332H.3	O		clock select, Bit start	0
334H 335H	Basic interval timer count register(BITCNT)				R			O	readable count register	00
336H 337H	Watch timer mode register (WMOD)				R/W	336H.3		O	clock/buzzer select. bit3 readable	00
386H 387H	Adc8 mode register (ADCM8)				R/W	386H.3		O	analog input pin select. start & low 4bit readable	00
388H 389H	Adc8 output latch (ADCOL8)				R			O	8bit conversion data	00
3A0H	Power control register (PCON)				R/W		O		system clock select, idle, stop mode	00
3A2H	Operating mode register (SCMOD)				R/W	O			main/sub system clock select	0
3A4H	Clock output mode register (CLOMD)				W		O		cpu clock output select, clock out EN/DIS	00
3A8H 3A9H	Serial interface mode register0 (SIOM0)				W	3A8H.3		O	receive/transmit mode. clock select	00
3AAH 3ABH	Serial interface buffer0 (SBUFF0)				R/W				serial shift register 0	XX
3ACH 3ADH	Serial interface mode register1 (SIOM1)				W	3ACH.3		O	receive/transmit mode, clock select	00

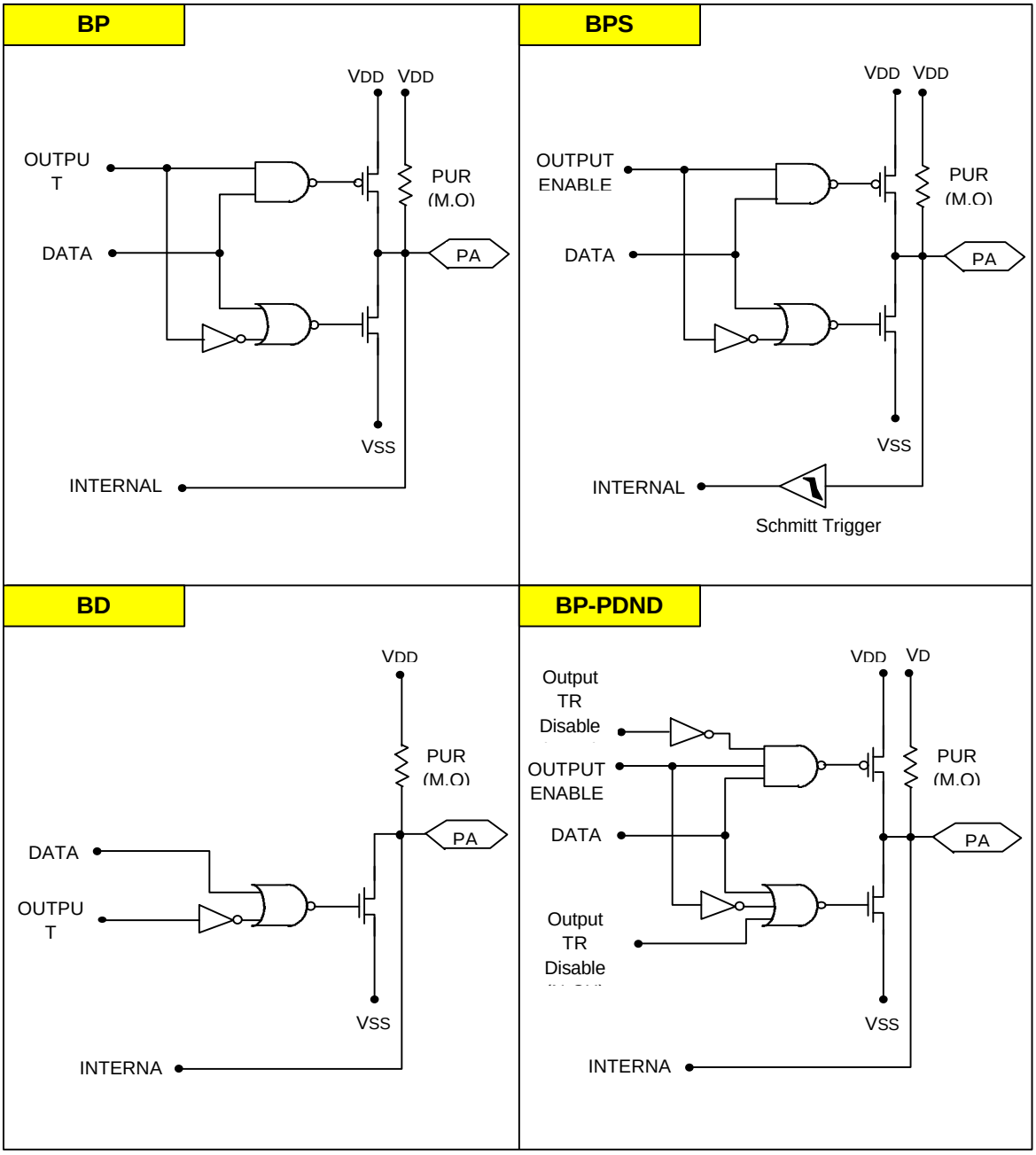
ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL
	b3	b2	b1	b0		1 bit	4 bit	8bit		VALUE
3AEH	Serial interface buffer1				R/W			O	serial shift register 1	00
3AFH	(SBUFF1)									
3B2H	Power on flag (PONF)				P/W	3B2H.0		O	power on reset flag	0
3C2H	IME				R/W	3C2H.3		O	Interrupt priorty select, IME flag.	00
3C3H	IPSR3	IPSR2	IPSR1	IPSR0						
3C4H	External interrupt mode register0 (IMOD0)				W		O		external interrupt 0 edge detection	00
3C5H	External interrupt mode register1 (IMOD1)				W		O		external interrupt 1 edge detection	00
3C6H	External interrupt mode register2 (IMOD2)				W		O		external interrupt 2 edge detection	00
3C7H	External interrupt mode register3 (IMOD3)				W		O		external interrupt 3 edge detection	00
3D8H	IE2	IRQ2	IEBT	IRQBT	R/W	O	O		Interrupt EN/IRQ flag	0
3D9H	IEAD8	IRQAD8	IEWT	IRQWT	R/W	O	O		Interrupt EN/IRQ flag	0
3DAH			IES0	IRQS0	R/W	O	O		Interrupt EN/IRQ flag	0
3DBH	IETC1	IRQTC1	IETC0	IRQTC0	R/W	O	O		Interrupt EN/IRQ flag	0
3DCH	IE1	IRQ1	IE0	IRQ0	R/W	O	O		Interrupt EN/IRQ flag	0
3DDH	IETC2	IRQTC2	IES1	IRQS1	R/W	O	O		Interrupt EN/IRQ flag	0
3DEH			IE3	IRQ3	R/W	O	O		Interrupt EN/IRQ flag	0
3E0H	PW03	PW02	PW01	PW00	W			O	port 0, 1 mode register (PMGA)	00
3E1H	PW13	PW12	PW11	PW10						
3E2H	PW23	PW22	PW21	PW20	W			O	port 2, 3 mode register (PMGB)	00
3E3H	PW33	PW32	PW31	PW30						
3E4H	PW43	PW42	PW41	PW40	W			O	port 4, 5 mode register (PMGC)	00
3E5H	PW53	PW52	PW51	PW50						
3E6H	PW63	PW62	PW61	PW60	W			O	port 6, 7 mode register (PMGD)	00
3E7H	PW73	PW72	PW71	PW70						
3E8H	PW83	PW82	PW81	PW80	W			O	port 8, 9 mode register (PMGE)	00
3E9H	PW93	PW92	PW91	PW90						
3EAH	PWA3	PWA2	PWA1	PWA0	W			O	port a, b mode register (PMGF)	00
3EBH	PWB3	PWB2	PWB1	PWB0						
3ECH	PWC3	PWC2	PWC1	PWC0	W			O	port c, d mode register (PMGG)	00
3EDH	PWD3	PWD2	PWD1	PWD0						
3F0H	PORT0 (R0)				R/W	O	O		R0 Port Data Register	0
3F1H	PORT1 (R1)				R/W	O	O		R1 Port Data Register	0
3F2H	PORT2 (R2)				R/W	O	O		R2 Port Data Register	0
3F3H	PORT3 (R3)				R/W	O	O		R3 Port Data Register	0
3F4H	PORT4 (R4)				R/W	O	O	O	R4 Port Data Register	0
3F5H	PORT5 (R5)				R/W	O	O		R5 Port Data Register	0
3F6H	PORT6 (R6)				R/W	O	O		R6 Port Data Register	0
3F7H	PORT7 (R7)				R/W	O	O		R7 Port Data Register	0
3F8H	PORT8 (R8)				R/W	O	O		R8 Port Data Register	0
3F9H	PORT9 (R9)				R/W	O	O		R9 Port Data Register	0
3FAH	PORTA (RA)				R/W	O	O		RA Port Data Register	0
3FBH	PORTB (RB)				R/W	O	O		RB Port Data Register	0
3FCH	PORTC (RC)				R/W	O	O	O	RC Port Data Register	0
3FDH	PORTD (RD)				R/W	O	O		RD Port Data Register	0

PIN DESCRIPTION

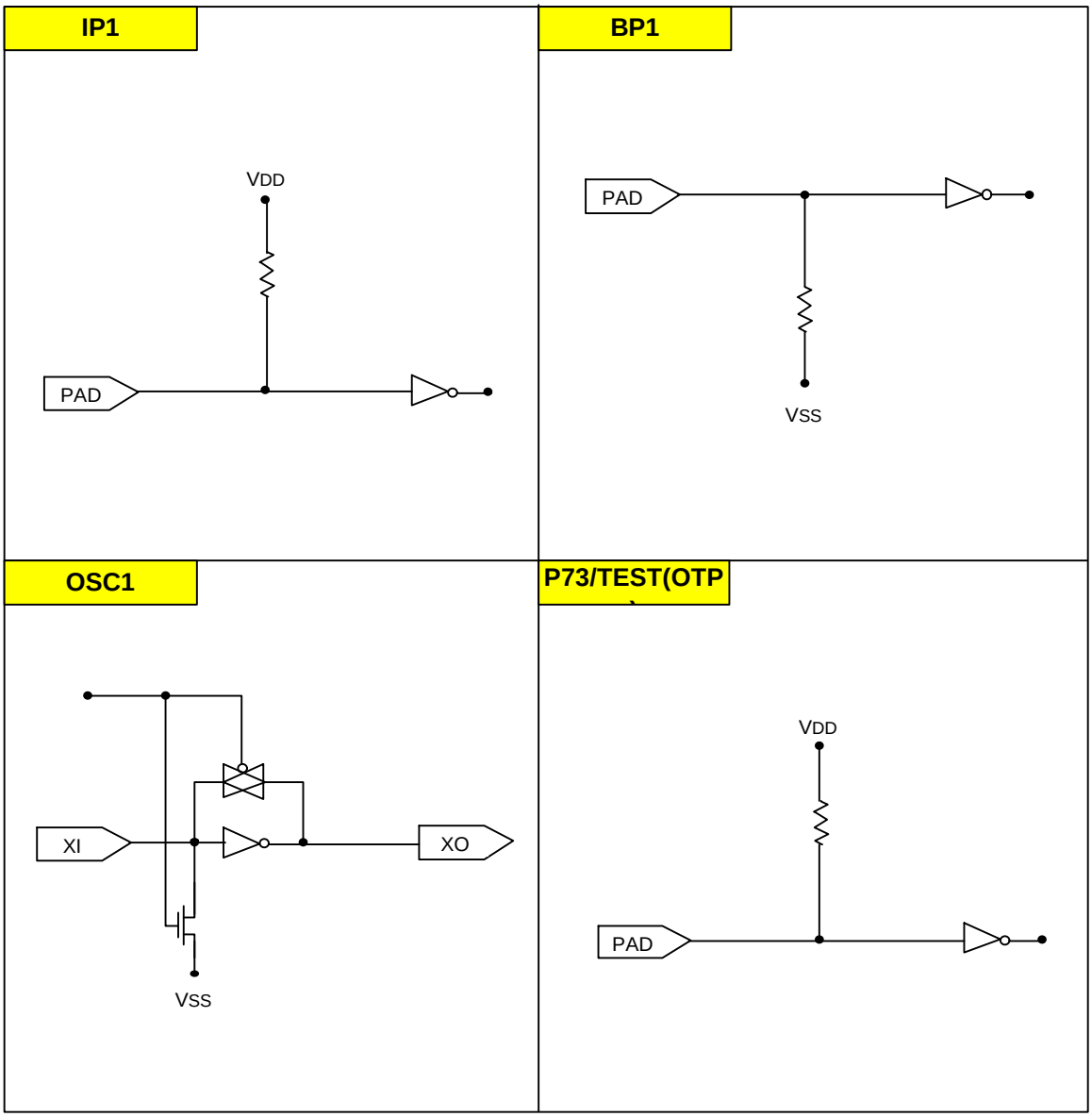
PIN SYMBOL	SHARED PIN	I/O	FUNCTION	RESET	PORT TYPE
P00 P01 P02 P03	INT0/TI0 INT1/TI1 INT2/TI2 INT3	I/O	4-BIT I/O PORT PORT 0		BPS
P10	$\overline{SCK}$	I/O	4-BIT I/O PORT PORT 1		BPS
P11	SI				
P12	SO				
P13	BUZ				
P20	CLO	I/O	4-BIT I/O PORT PORT 2		BP
P21~ P23	-				
P3	-	I/O	4-BIT I/O PORT. PORT3		BP
P4	-		4-BIT I/O PORT. PORT4		BD
P5	-		4-BIT I/O PORT. PORT5		
P6	-		4-BIT I/O PORT. PORT6		BP-PDND
P7	-		4-BIT I/O PORT. PORT7	INPUT	BP
P8	-		4-BIT I/O PORT. PORT8		
P9	-		4-BIT I/O PORT. PORT9		
PA	AD0~AD3		4-BIT I/O PORT. PORTA		
PB	AD4~AD7		4-BIT I/O PORT. PORTB		
PC	-		4-BIT I/O PORT. PORTC		BD
PD	-		4-BIT I/O PORT. PORTD		
INT0/TI0	P00	I	External interrupt input port rising/falling edge detection Event pulse input port for the timer/event counters		BP
INT1/TI1	P01				
INT2/TI2	P02				
INT3	P03				
$\overline{SCK}$	P10	I/O	Serial clock in/out port		BPS
SI	P11	I	Serial data input port		
SO	P12	O	Serial data output port		
BUZ	P13	O	Buzzer output port		
CLO	P20	O	Clock output port		BP
Key scan	P4-P5	I	4, 6, 8, bits Key scan input selectable		
AD0~AD3	PA	I	Analog input for the 8-bit A/D converter		
AD4~AD7	PB				
XI XO	-		XI, XO are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.		OSC1
RESETB	-	I	Reset input pin		IP1
TEST	-	I	Connect to V_{SS}		BP1
AV_{DD}, AV_{SS}	-		Power & ground for the A/D converter		
V_{DD}, V_{SS}	-		Power & ground		

NOTE) P4, P5, PC, PD : 8-bit operation possible

I/O CIRCUITS



NOTE) PUR : Pull-Up Resistor
M.O : Mask Option


IP1
VDD
PAD
BP1
PAD
VSS
OSC1
XI
XO
VSS
P73/TEST(OTP
VDD
PAD

ABSOLUTE MAXIMUM RATINGS

(T_A = 0¡É to 70¡É, V_{DD} = 5V ±10%, f_X = 4.19MHz)

PARAMETER	SYMBOL	CONDITION	RATING		UNIT
Supply Voltage	V_{DD}	-	-0.3 to +7.0		V
Input Voltage	V_I	All I/O ports	-0.3 to V_{DD}+0.3		V
Output Voltage	V_O	-	-0.3 to V_{DD}+0.3		V
Output Current High	I_{OH}	One I/O port active	-15		mA
		All I/O ports active	-30		
Output Current Low	I_{OL}	One I/O port active	Peak Value	+30	mA
		-	RMS Value	+15	
		Total value for ports P1, P2, P3, P8	Peak Value	+100	
			RMS Value	+60	
		Total value for ports P0, P4, P5, P6	Peak Value	+100	
			RMS Value	+60	
Operating Temperature	T_A	-	-40 to +85		¡É
Storage Temperature	T_{stg}	-	-55 to +125		¡É

* RMS values are calculated as peak value $\times \sqrt{\text{Duty}}$
* Exceeding beyond those listed values under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = 0, V_{DD} = 5V ±10%, T_A = 25¡É, f_X = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION			LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT
High Level Input Voltage	V_{IH}	Port 0 ~ Port D			0.7V_{DD}	-	V_{DD}	V
		RESETB, XI			0.8V_{DD}	-	V_{DD}	
Low Level Input Voltage	V_{IL}	Port 0 ~ Port D (Excepted TEST/R73)			-	-	0.3V_{DD}	V
		RESETB, XI, TEST/R73			-	-	0.2V_{DD}	
High Level Output Voltage	V_{OH}	All Ports Except Open Drain Ports (Port 4,5,C,D)	(I_{OH} = - 4mA)		0.85V_{DD}	-	-	V
			(I_{OH} = - 1mA)		0.95V_{DD}	-	-	
			(I_{OH} = - 100uA)		0.99V_{DD}	-	-	
Low Level Output Voltage	V_{OL}	All Ports	(I_{OL} = 10mA)		-	-	0.5	V
			(I_{OL} = 4mA)		-	-	0.3	
			(I_{OL} = 400uA)		-	-	60	mV
High Level Input Leakage Current	I_{IH}	All Pin Except XI, RESETB (V_{IN} = V_{DD})			-	-	3	uA
					-	1.2	100	
Low Level Input Leakage Current	I_{IL}	All Pin Except RESETB, P73/TEST (V_{IN} = 0V)			-	-	-3	uA
					-	-1.2	-200	
Supply Current	I_{DD1}	Main Clock (XI) = 4.19MHz	Dynamic Mode	V_{DD} = 5V ±10%	-	-	10	mA
			Idle Mode		-	-	5	
	I_{DD2}	Main Clock (XI) = 2MHz	Dynamic Mode	V_{DD} = 3V ±10%	-	-	2	
			Idle Mode		-	-	1	

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = 0, V_{DD} = 5V ±10%, T_A = 25¡É, f_X = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION			LIMIT			UNIT
					MIN.	TYP.	MAX.	
Supply Current	I_{DD3} (1)	Main Clock (XI) = 4.19MHz	Stop Mode	V_{DD} = 5V ±10%	-	1	5	uA
				V_{DD} = 3V ±10%	-	0.5	3	
Internal Pull-up Resistor (M.O)	R_{PU}	All Ports VI or VO = 0V, VDD = 5V			-	-	40	Kohm
Pull-up Resistor	R_{L1}	V_I = 0V, V_{DD} = 5V ±10% RESETB			20	-	60	
Pull-down Resistor	R_{L2}	V_I = 0V, V_{DD} = 5V ±10% TEST			10	-	30	

NOTES) :

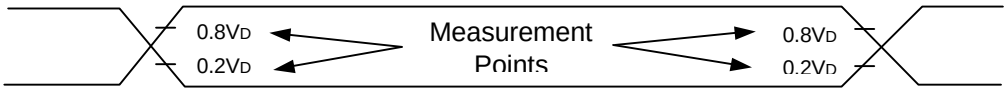
(1) Main system clock oscillation stops.

AC ELECTRICAL CHARACTERISTICS

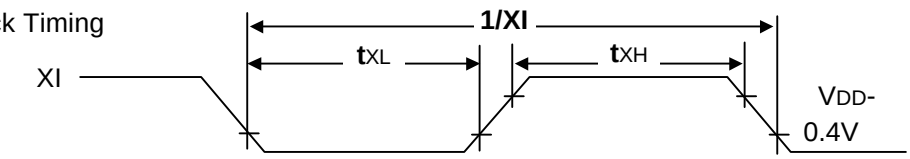
(T_A = -40 to +85¡É, V_{DD} = 2.7 to 6.0V)

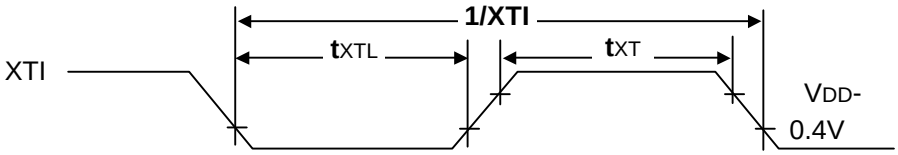
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Cycle Time	t_{CY}	V_{DD} = 4.5 to 6.0V		0.95	-	64	uS
		V_{DD} = 2.7 to 3.3V		3.8	-	64	uS
TI Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0V		0	-	1	MHz
		V_{DD} = 2.7 to 3.3V		0	-	275	KHz
TI Input High, Low	t_{TIH}	V_{DD} = 4.5 to 6.0V		0.48	-	-	uS
Level Width	t_{TIL}	V_{DD} = 2.7 to 3.3V		1.8	-	-	uS
$\overline{SCK}$ Cycle Time	t_{KCY}	V_{DD} = 4.5 to	Input	800	-	-	nS
			Output	950	-	-	nS
		V_{DD} = 2.7 to	Input	3200	-	-	nS
			Output	3800	-	-	nS
$\overline{SCK}$ High, Low Level Widtl	t_{KH}	V_{DD} = 4.5 to	Input	400	-	-	nS
			Output	t_{KCY}/2~50	-	-	nS
	t_{KL}	V_{DD} = 2.7 to	Input	1600	-	-	nS
			Output	t_{KCY}/2~15	-	-	nS
SI Set up Time to $\overline{SCK}$ Hig	t_{SIK}			100	-	-	nS
SI Hold Time to $\overline{SCK}$ High	t_{KSI}			400	-	-	nS
$\overline{SCK}$ to S0 Output	t_{KSO}	V_{DD} = 4.5 to	Input	-	-	300	nS
Delay Time			Output	-	-	250	nS
		V_{DD} = 2.7 to	Input	-	-	1000	nS
			Output	-	-	1000	nS
INT 0 ~ 4 Input Level	t_{INTH}			5	-	-	uS
High, Low	t_{INTL}			5	-	-	uS
RESETB Low Level	t_{RSL}			5	-	-	uS

AC Timing Measurement Points (Except XI and XTI)

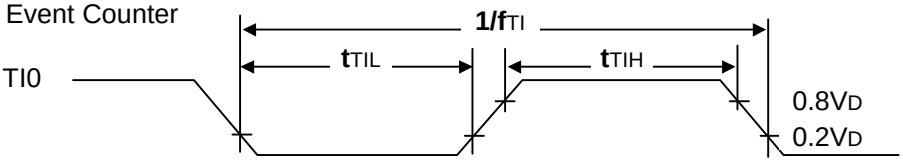


Clock Timing

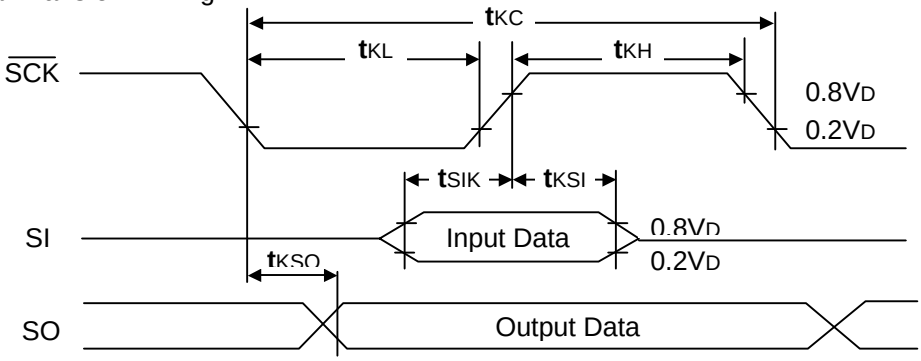




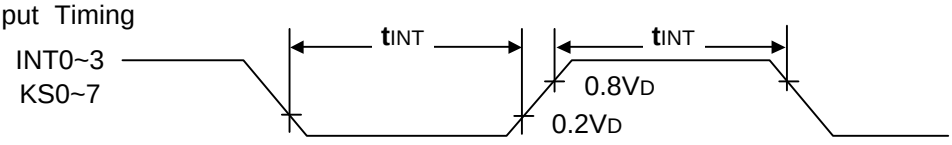
Timer Event Counter



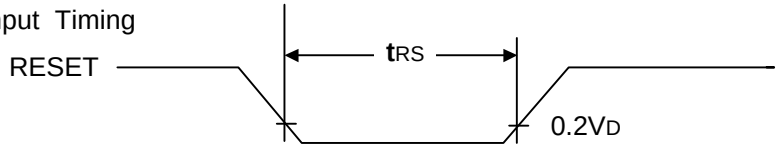
Serial Transfer Timing



Interrupt Input Timing



RESETB Input Timing



RAM DATA RETENTION CHARACTERISTICS (in STOP Mode)

(T_A = -40 to +85¡É)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{DDDR}		2.0	-	6.0	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 2.0V	-	0.1	10	uA
Release Signal Set Time	t_{SREL}		0	-	-	uS
Oscillation Stabilization Wait Time	t_{WAIT}	When released by RESETB	-	2^{17}/fx	-	mS
		When released by interrupt Signal	-	NOTE 1)	-	mS

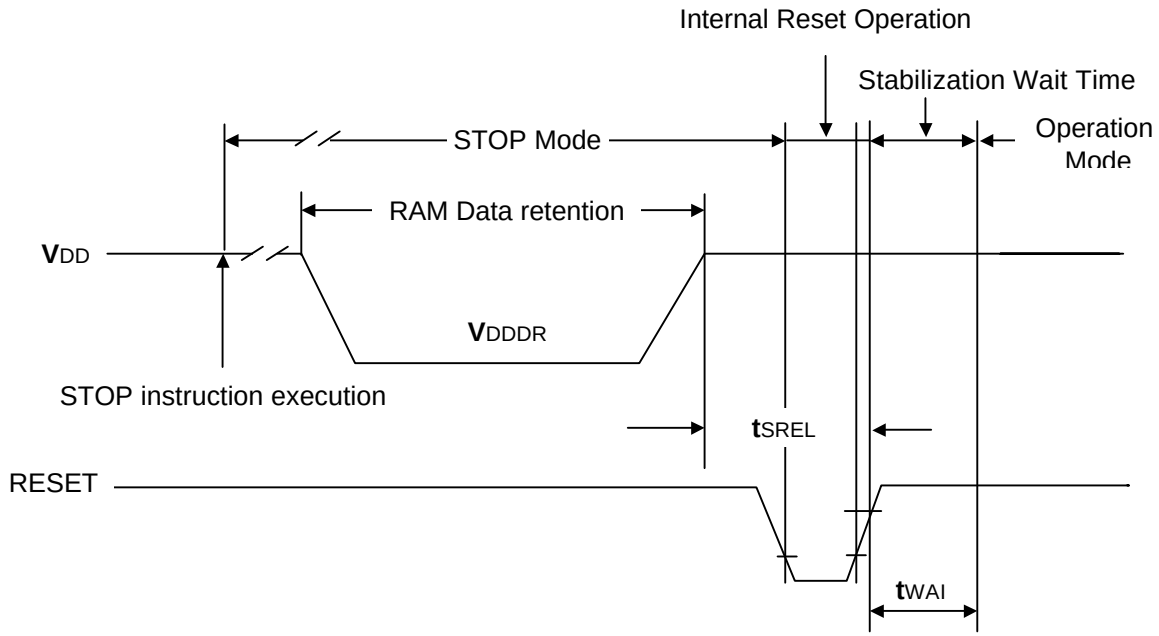
NOTE 1) Depends on the setting of the basic interval timer mode register.
(refer to the table below)

(fx = 4.19MHz)

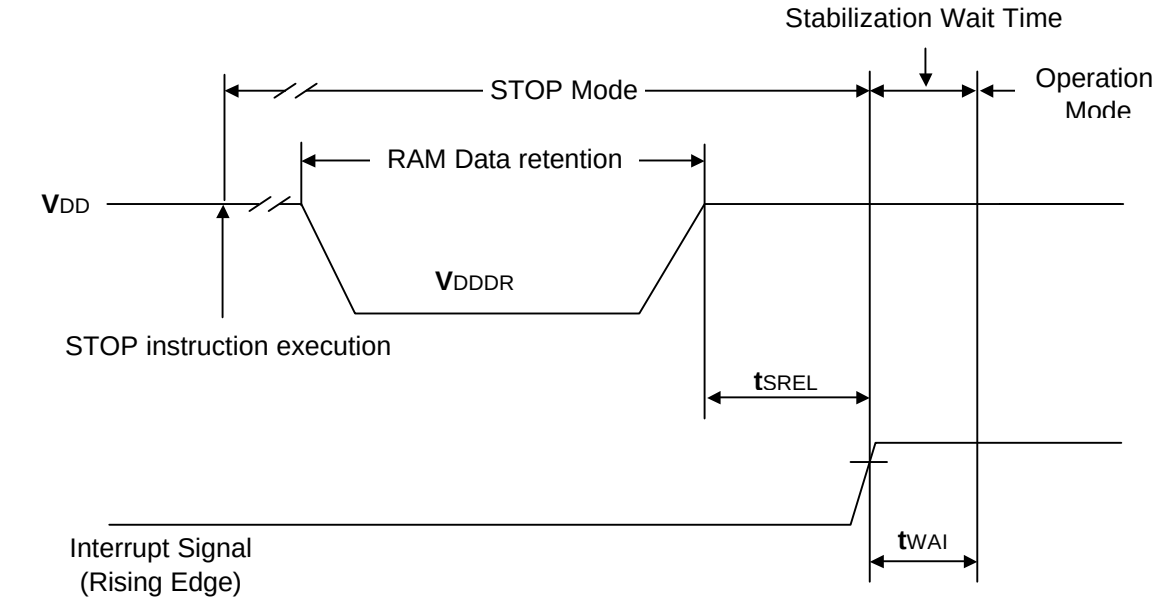
BMOD2	BMOD1	BMOD0	Oscillation Stabilization
0	0	0	2^{20}/fx (Approximately 250ms)
0	1	1	2^{17}/fx (Approximately 31.3ms)
1	0	0	2^{15}/fx (Approximately 7.82ms)
1	0	1	2^{13}/fx (Approximately 1.95ms)

RAM DATA RETENTION TIMING

When STOP mode is released by RESETB input



When STOP mode is released by interrupt signal

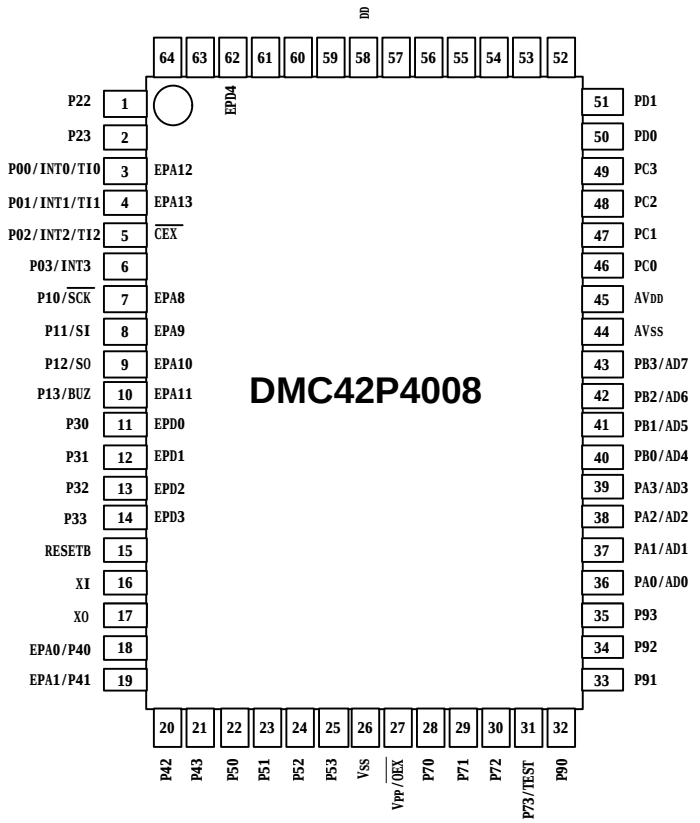


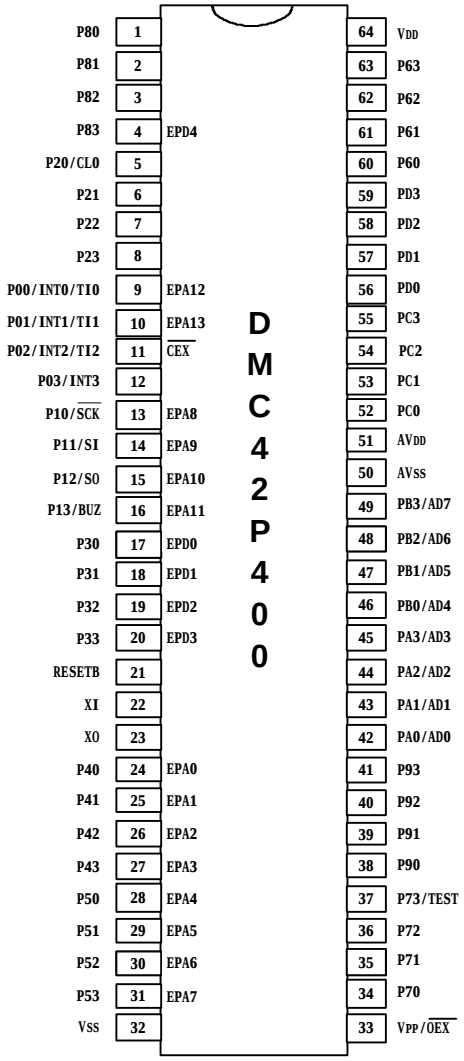
DMC42P4008

DESCRIPTION

The DMC42P4008 is a system evaluation LSI having a built in One-Time Programming circuit. A programming and verification for the internal EPROM is achieved by using a general EPROM programmer with an adapter socket.
The function of this device is exactly same as the DMC42C4008 with programming of the internal EPROM. The DMC42P4008 is the OTP version of the DMC42C4008 with replacement of MASK ROM to EPROM as an internal ROM.

PIN CONFIGURATION





DEVICE OPERATION

The operational modes of the DMC42P4008 are listed in Table 1.
A single 5V power supply is required in the read mode.
All inputs are TTL levels except for V_{PP} / $\overline{OEX}$.

V_{PP} = 12.5±0.5V

PINS / MODE	$\overline{CEX}$	V_{PP} / $\overline{OEX}$	V_{DD}	OUTPU
READ	V_{IL}	V_{IL}	5.0V	D_{OUT}
PROGRAM	V_{IL}	V_{PP}	6.0V	D_{IN}
VERIFY	V_{IL}	V_{IL}	6.0V	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	6.0V	High Z

TABLE 1. Operating Modes

PIN NAME	MODE	
	EPROM MODE	USER MODE
TEST	V_{IL}	V_{IH}
RESETB	V_{IL}	V_{IH} / V_{II}

TABLE 2. The modes of DMC42P4008

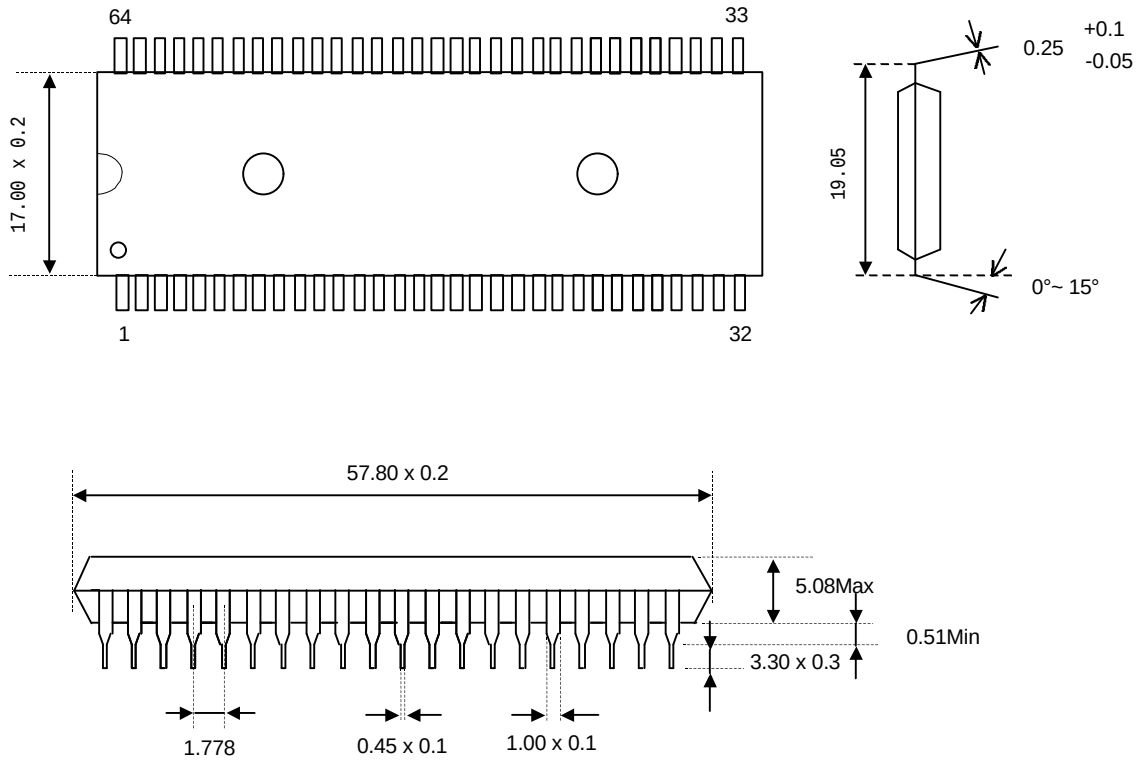
DC PROGRAMMING CHARACTERISTICS

PARAMETER	SYMBO	TEST CONDITION	LIMIT		UNIT
			MIN.	MAX.	
Input Low Voltage	V_{IL}		-0.1	0.8	V
Input High Voltage	V_{IH}		2.0	V_{DD}	V
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	-	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = -400uA	2.4	-	V
Quick-pulse Programming	V_{PP}		12.5	13.0	V
Quick-pulse Programming	V_{DD}		6.0	6.5	V

PACKAGE DIMENSION

[UNIT : Millimeter]

64 SDIP



PACKAGE DIMENSION

[UNIT : Millimeter]