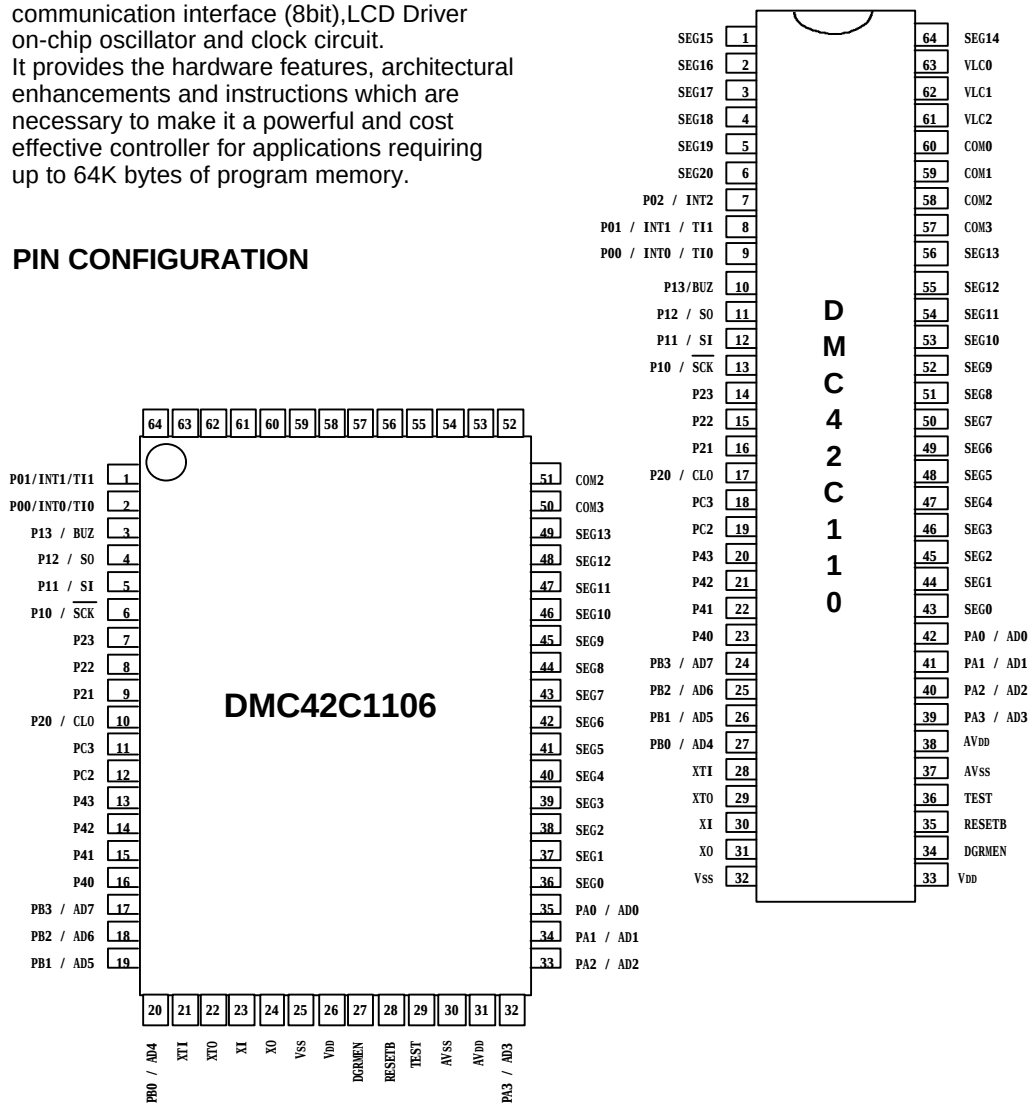
DESCRIPTION

The DMC42C1106 is a 4-bit single chip microcomputer designed with CMOS silicon gate technology.
The DMC42C1106 includes such peripherals as various timers, A/D converter (8ch), serial communication interface (8bit),LCD Driver on-chip oscillator and clock circuit.
It provides the hardware features, architectural enhancements and instructions which are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory.

PIN CONFIGURATION



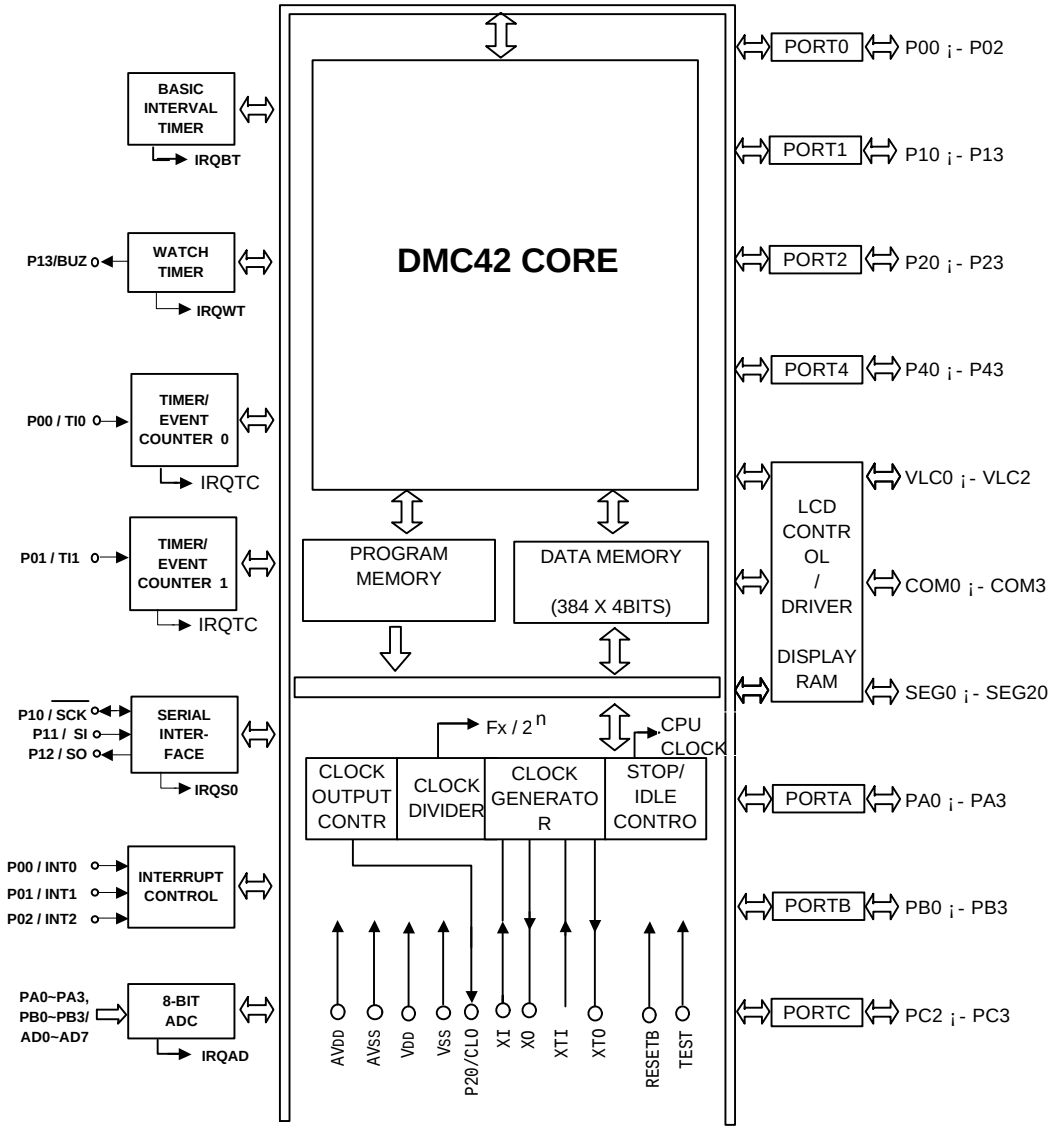
FEATURE

- Memory mapped I/O
- Program memory : 6144 x 10bits
- Data memory : 384 x 4bits
- Instructions
  - Various bit manipulation
  - 8-bit data operation
  - 7-bit relative branch
  - 1 byte absolute call
- Instruction cycle times
  - Main (XI = 4.19MHz)
    . 15.3 us (XI/64 = 65.5KHz)
    . 1.91 us (XI/8 = 524.0KHz)
    . 0.95 us (XI/4 = 1.05MHz)
  - Sub (XTI = 32.768KHz)
    . 122 us (XTI/4 = 8.19KHz)
- 4 Register Bank
- General register : 8 x 4-bit respectively
- Accumulator
  - Bit Accumulator (CY), 4 bit Accumulator (A), 8 bit Accumulator (XA)
- Multiple vectored interrupt source
  - External interrupt : 3
  - Internal interrupt : 6
- Watch timer
  - fast mode : 3.91 msec
  - normal mode : 0.5 sec
  - buzzer output : 1, 2, 4 KHz
- Basic interval timer
  - 8 kinds of period
  - Used stabilization wait timer to wake up Stop mode
- Two 8-bit timer / event counters
- 8-bit serial communication interface
  - External / Internal clock selection
  - Mode : Transmit ·Receive
    Receive only
    Clock continuous
- LCD controller/driver
  - selectable number of segments (21)
  - Display mode selection
    · Static
    · 1/2 duty (1/2 bias)
    · 1/3 duty (1/2 bias)
    · 1/3 duty (1/3 bias)
    · 1/4 duty (1/3 bias)
- 50 I/O Pins
  - LCD driver output pins : 25
    . Segment ouput pins : 9
    . Segment CMOS outputpins : 12
    . Common ounput pins : 4
  - CMOS input/output pins : 25
- Power saving mode
  - STOP : Main clock, CPU clock stop
  - STBY : Only CPU clock stop
    Main clock operation
- Package : 64 QFP, 64 SDIP

APPLICATION

VTR, Camera, Rice Cooker, Telephone
Blood Pressure Gauge, CD Player

BLOCK DIAGRAM



PROGRAM MEMORY (ROM)

	CONTENTS
0000H	VECTOR ADDRESS AREA
001FH	
0020H	ZERO-PAGE CALL AREA
002FH	
0060H	**6K Byte**
17FFH	

VECTOR ADDRESS

	Prioty	INTERRUPT SUORCE	
0000H	0	RESET	Reset Signal
0002H	1	IRQBT	Basic Interval Timer
0004H	2	IRQ0	External interrupt 0
0006H	3	IRQ1	External interrupt 1
0008H	4	IRQTC0	Timer Event Counter 0
000AH	5	IRQTC1	Timer Event Counter 1
000CH	6	IRQ2	External interrupt 2
000EH			
0010H			
0012H	9	IRQS0	Serial I/O 0
0014H	10	IRQAD	8 bit ADC
0016H			
0018H	12	IRQWT	Watch Timer
001AH	13	IRQKS	Key Scan
001CH			
001EH	15	-	reserved

DATA MEMORY (RAM)

		DIRECT	INDIRECT			STACK	GENERAL REGISTER	
		m	@HL		@DE @DL			
	$00 PAGE0 (256 Byte) $FF			**MP=0**		**SPS=0**	**RB=0 RB=2**	**RB=1 RB=4**
	$00 PAGE1 (128 Byte) $FF	**MB=0**	**MB=0**	**MP=1**		**SPS=1**		
BANK 0 (1K)	$00 PAGE2 (256 Byte) $FF			**MP=2**		**SPS=2**		
		LCD Display RAM (2E0~2F4)						
	$00 PAGE3 (256 Byte) $FF	**I/O MEMORY**		**MP=3**				

; Usable

I/O ADDRESS MAP

ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL VALUE
	b3	b2	b1	b0		1 bit	4 bit	8bit		
318H	Stack pointer low (SPL)				R/W			O	Stack pointer low	E
319H	Stack pointer high (SPH)				R/W			O	stack pointer high	F
31AH	SP3	SP2	SP1	SP0	R/W			O	Stack Page Select Low (SPSL)	0
31BH	-	-	SP5	SP4	R/W			O	Stack Page Select High (SPSh)	0
31CH	AC		IS1	IS0	R/W	O	O	O	Psw low (PSWL)	0
31DH	CY	Z	OV	T					Psw high (PSWH)	0
320H 321H	T/E counter mode register 0 (TMOD0)				W	320H.3		O	Clock source select. counter start (ch0)	00
322H 323H	T/E counter register 0 (TMCNT0)				R			O	readable count value (ch0)	00
324H 325H	T/E reference register 0 (TMREF0)				W			O	count reference register (ch0)	FF
326H 327H	T/E counter mode register 1 (TMOD1)				W	326H.3		O	clock source select. counter start (ch1)	00
328H 329H	T/E counter register 1 (TMCNT1)				R			O	readable count value (ch1)	00
32AH 32BH	T/E reference register 1 (TMREF1)				W			O	count reference register (ch1)	FF
332H	Basic Timer mode register(BMOD)				R/W	332H.3			clock select, Bit start	0
334H 335H	Basic interval timer count register(BITCNT)				R			O	readable count register	00
336H 337H	Watch timer mode register (WMOD)				R/W	336H.3		O	clock/buzzer select. bit3 readable	00
386H 387H	Adc8 mode register (ADCM8)				R/W	386H.3		O	analog input pin select. start & low 4bit readable	00
388H 389H	Adc8 output latch (ADCOL8)				R			O	8bit conversion data	00
390H 391H	Lcd display mode register (LCDMD)				W			O	duty/bias/clock/seg/bitport select	00
392H	Lcd control register (LCON)				W		O		display ON/OFF	0
3A0H	Power control register (PCON)				R/W		O		system clock select, idle, stop mode	00
3A2H	Operating mode register (SCMOD)				R/W	O			main/sub system clock select	0
3A4H	Clock output mode register (CLOMD)				W		O		cpu clock output select, clock out EN/DIS	00
3A8H 3A9H	Serial interface mode register0 (SIOM0)				W	3A8H.3		O	receive/transmit mode. clock select	00
3AAH 3ABH	Serial interface buffer0 (SBUFF0)				R/W				serial shift register 0	XX
3ACH 3ADH	Serial interface mode register1 (SIOM1)				W	3ACH.3		O	receive/transmit mode, clock select	00
3AEH 3AFH	Serial interface buffer1 (SBUFF1)				R/W			O	serial shift register 1	00
3B2H	Power on flag (PONF)				P/W	3B2H.0		O	power on reset flag	0

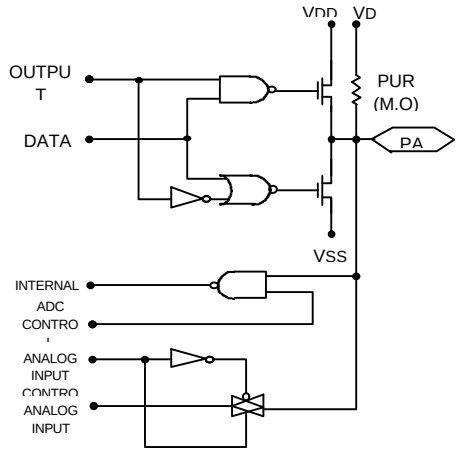
ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL
	b3	b2	b1	b0		1 bit	4 bit	8bit		VALUE
3C2H	IME				R/W	3C2H.3		O	Interrupt priorty select, IME flag.	00
3C3H	IPSR3	IPSR2	IPSR1	IPSR0						
3C4H	External interrupt mode register0 (IMOD0)				W		O		external interrupt 0 edge detection	00
3C5H	External interrupt mode register1 (IMOD1)				W		O		external interrupt 1 edge detection	00
3C6H	External interrupt mode register2 (IMOD2)				W		O		external interrupt 2 edge detection	00
3D8H	IE2	IRQ2	IEBT	IRQBT	R/W	O	O		Interrupt EN/IRQ flag	0
3D9H	IEAD8	IRQAD8	IEWT	IRQWT	R/W	O	O		Interrupt EN/IRQ flag	0
3DAH			IES0	IRQS0	R/W	O	O		Interrupt EN/IRQ flag	0
3DBH	IETC1	IRQTC1	IETC0	IRQTC0	R/W	O	O		Interrupt EN/IRQ flag	0
3DCH	IE1	IRQ1	IE0	IRQ0	R/W	O	O		Interrupt EN/IRQ flag	0
3DDH			IES1	IRQS1	R/W	O	O		Interrupt EN/IRQ flag	0
3DEH					R/W	O	O		Interrupt EN/IRQ flag	0
3E0H	PW03	PW02	PW01	PW00	W			O	port 0, 1 mode register (PMGA)	00
3E1H	PW13	PW12	PW11	PW10						
3E2H	PW23	PW22	PW21	PW20	W			O	port 2, 3 mode register (PMGB)	00
3E3H	PW33	PW32	PW31	PW30						
3E4H	PW43	PW42	PW41	PW40	W			O	port 4, 5 mode register (PMGC)	00
3E5H	PW53	PW52	PW51	PW50						
3EAH	PWA3	PWA2	PWA1	PWA0	W			O	port a, b mode register (PMGF)	00
3EBH	PWB3	PWB2	PWB1	PWB0						
3ECH	PWC3	PWC2	PWC1	PWC0	W			O	port c, d mode register (PMGG)	00
3EDH	PWD3	PWD2	PWD1	PWD0						
3F0H	PORT0 (R0)				R/W	O	O		R0 Port Data Register	0
3F1H	PORT1 (R1)				R/W	O	O		R1 Port Data Register	0
3F2H	PORT2 (R2)				R/W	O	O		R2 Port Data Register	0
3F3H	PORT3 (R3)				R/W	O	O		R3 Port Data Register	0
3F4H	PORT4 (R4)				R/W	O	O	O	R4 Port Data Register	0
3FAH	PORTA (RA)				R/W	O	O		RA Port Data Register	0
3FBH	PORTB (RB)				R/W	O	O		RB Port Data Register	0
3FCH	PORTC (RC)				R/W	O	O	O	RC Port Data Register	0

PIN DESCRIPTION

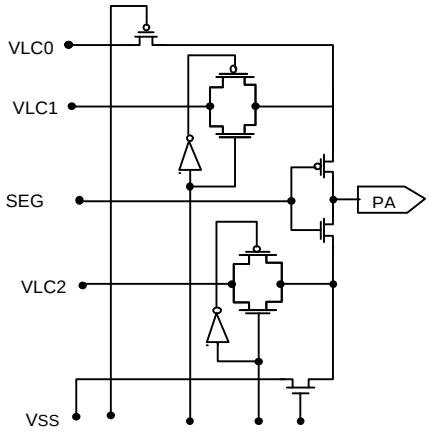
PIN SYMBOL	SHARED PIN	I/O	FUNCTION	RESET	PORT TYPE
P00	INT0/TI0	I/O	- 3 bit I/O Port (PORT0)	INPUT	BPS
P01	INT1/TI1		- INT0, 1, 2 pins are the external interrupt inputs		
P02	INT2		- TI0, 1 pins are the timer/event counter inputs		
P10	$\overline{SCK}$	I/O	- 4 bit I/O Port (PORT1)		BPS
P11	SI		- The $\overline{SCK}$ pin is the serial clock input		
P12	SO		- The SI pin is the serial data input		
P13	BUZ		- The SO pin is the serial data output		
			- The BUZ pin is the watch timer signal output		
P20	CLO	I/O	- 4 bit I/O Port (PORT2)		BPS
P21 ~ P23	-		- The CLO pin is the system clock output		BP
P40 ~ P43	-	I/O	4 bit I/O Port (PORT4)		BDR
PA0 ~ PA3	AD0~AD3		- 4 bit I/O Port (PORTA)		BPA
			- Analog input port		
PB0 ~ PB3	AD4~AD7		- 4 bit I/O Port (PORTB)		BPA
			- Analog input port		
PC2 ~ PC3	-		2 bit I/O Port		BDR
VLC0~VLC2	-	I	LCD bias inputs		
COM0~COM3	-	O	LCD common signal outputs		OCOM
SEG0~SEG19	-	O	LCD segment signal outputs		OSEG-A
SEG20	-	O	LCD segment signal output and 1 bit data output		OSEG-B
XI XO	-	-	XI, XO are main oscillator input pin, output pin, respectively		OSC1
XTI XTO	-	-	XTI, XTO are sub oscillator input, output pin respectively		OSC2
RESETB	-	I	Reset input pin		IP1
TEST	-	-	No connection (must be connect to V_{SS})		IP2
DGRMEN	-	-	No connection		
AV_{DD},	-	-	Power & ground for the A/D convertor		
V_{DD}, V_{SS}	-	-	Power & ground		

I/O CIRCUITS

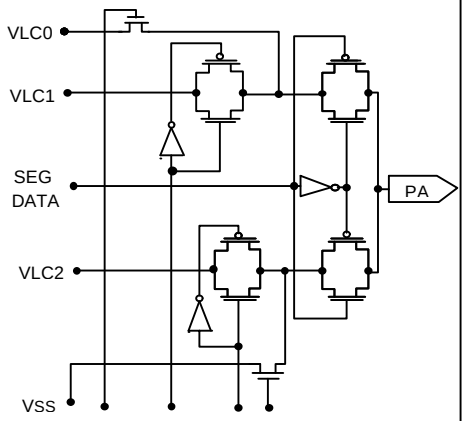
BPA



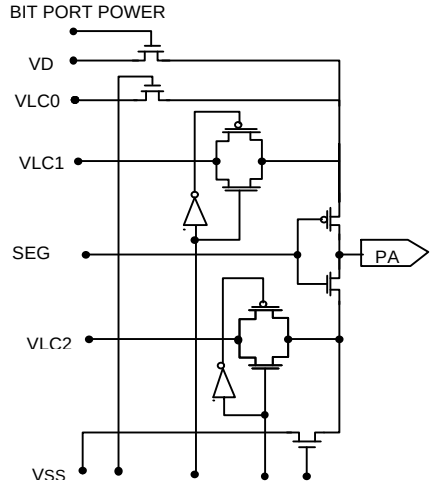
OSEG-A



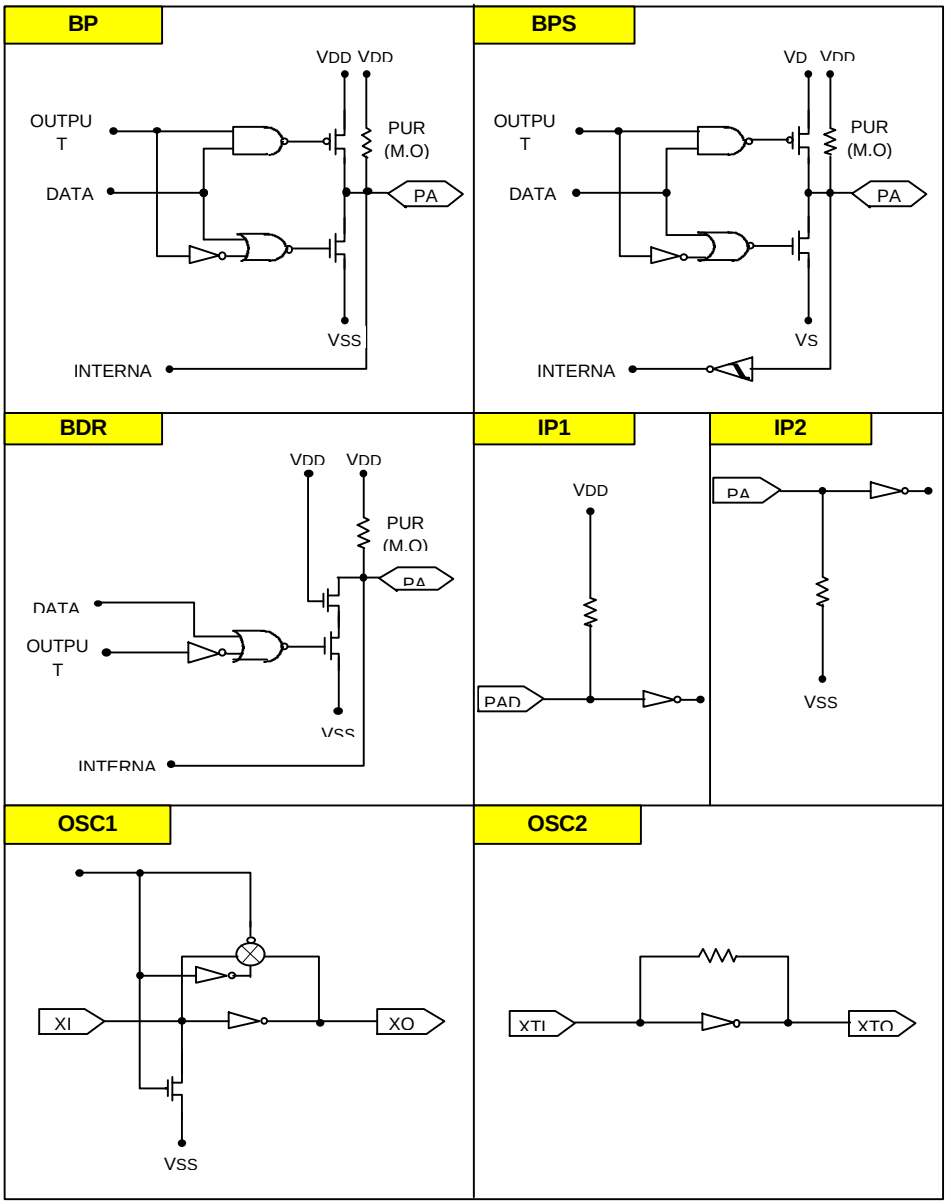
OCOM



OSEG-B



I/O CIRCUITS



NOTE) PUR : Pull-Up Resistor
M.O : Mask Option

ABSOLUTE MAXIMUM RATINGS

(T_A = 0¡É to 70¡É, V_{DD} = 5V ±10%, f_X = 4.19MHz)

PARAMETER	SYMBOL	CONDITION	RATING		UNIT
Supply Voltage	V_{DD}	-	-0.3 to +7.0		V
Input Voltage	V_I	All I/O ports	-0.3 to V_{DD}+0.3		V
Output Voltage	V_O	-	-0.3 to V_{DD}+0.3		V
Output Current High	I_{OH}	One I/O port active	-15		mA
		All I/O ports active	-30		
Output Current Low	I_{OL}	One I/O port active	Peak Value	+30	mA
		-	RMS Value	+15	
		Total value for ports P0, P1, P2, P4	Peak Value	+100	
			RMS Value	+60	
Operating Temperature	T_A	-	-40 to +85		¡É
Storage Temperature	T_{stg}	-	-55 to +125		¡É

* RMS values are calculated as peak value x $\sqrt{\text{Duty}}$
* Exceeding beyond those listed values under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC ELECTRICAL CHARACTERISTICS

(VSS = 0, VDD = 5V ±10%, TA = 25¡É, fx = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION		LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT
Low Level Input Voltage	VIL1	Port 0, 1 (Schmitt Input)		-	-	0.2	V
	VIL2	Port 2, 4, A, B, C, RESETB, TEST		-	-	0.3 VDD	
	VIL3	XI, XTI		-	-	0.4	
High Level Input Voltage	VIH1	Port 0, 1 (Schmitt Input)		0.8	-	VDD	V
	VIH2	Port 2, 4, A, B, C, RESETB, TEST		0.7	-	VDD	
	VIH3	XI, XTI		VDD -	-	VDD	
Low Level Output Voltage	VOL1	Port 4, C (Open Drain)		-	-	2	V
	VOL2	Port 0, 1, 2, A, B	IOL=1.6m	-	-	0.4	
	VOL3	VDD = 4.5V, SEG20		-	-	0.6	
High Level Output Voltage	VOH1	Port 0, 1, 2, A, B	IOH= -	VDD -	-	-	V
	VOH2	SEG20		VDD -	-	-	
Low Level Input Leakage Current	ILIL1	VDD = 6V, Port 0, 1, 2, 4, A, B, C VPPOEX, TEST, XTI		-	-1.2	-3	uA
	ILIL2	VDD = 6V, XI		-	-5	-15	
High Level Input Leakage Current	ILIH1	VDD = 6V, Port 0, 1, 2, 4, A, B, C VPPOEX, RESETB, XTI		-	1.2	3	uA
	ILIH2	VDD = 6V, XI		-	5	15	
Supply Current	IDD1 (1)	Normal Mode Xin = 4.19MHz Xtin = 32.768KHz	Vdd = 5V ±10%	-	-	8	mA
	IDD2 (1)	Standby Mode Xin = 0 Xtin = 32.768KHz	Vdd = 5V ±10%	-	-	2	mA
	IDD3 (2)	Standby Mode Xin = 0 Xtin = 32.768KHz	Vdd = 3V ±10%	-	30	50	uA
	IDD4 (2)	Stop Mode Xin = 0 Xtin = 0	Vdd = 5V ±10%	-	1	5	uA

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = 0, V_{DD} = 5V ±10%, T_A = 25¡É, f_X = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION			LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT
Supply Current	I_{DD5}	XTI = 0V	Stop Mode	V_{DD} = 5V ±10%	-	-	5	uA
		XI = 0V		V_{DD} = 5V ±10%	-	-	3	
Pull-up Resistor	R_{L1}	V_I = 0V, V_{DD} = 5V±10% RESETB			20	-	60	Kohm
Pull-down Resistor	R_{L2}	V_I = 5V, V_{DD} = 5V ±10% TEST			10	-	30	

NOTES) :

(1) Data Include power consumption for subsystem clock oscillation.

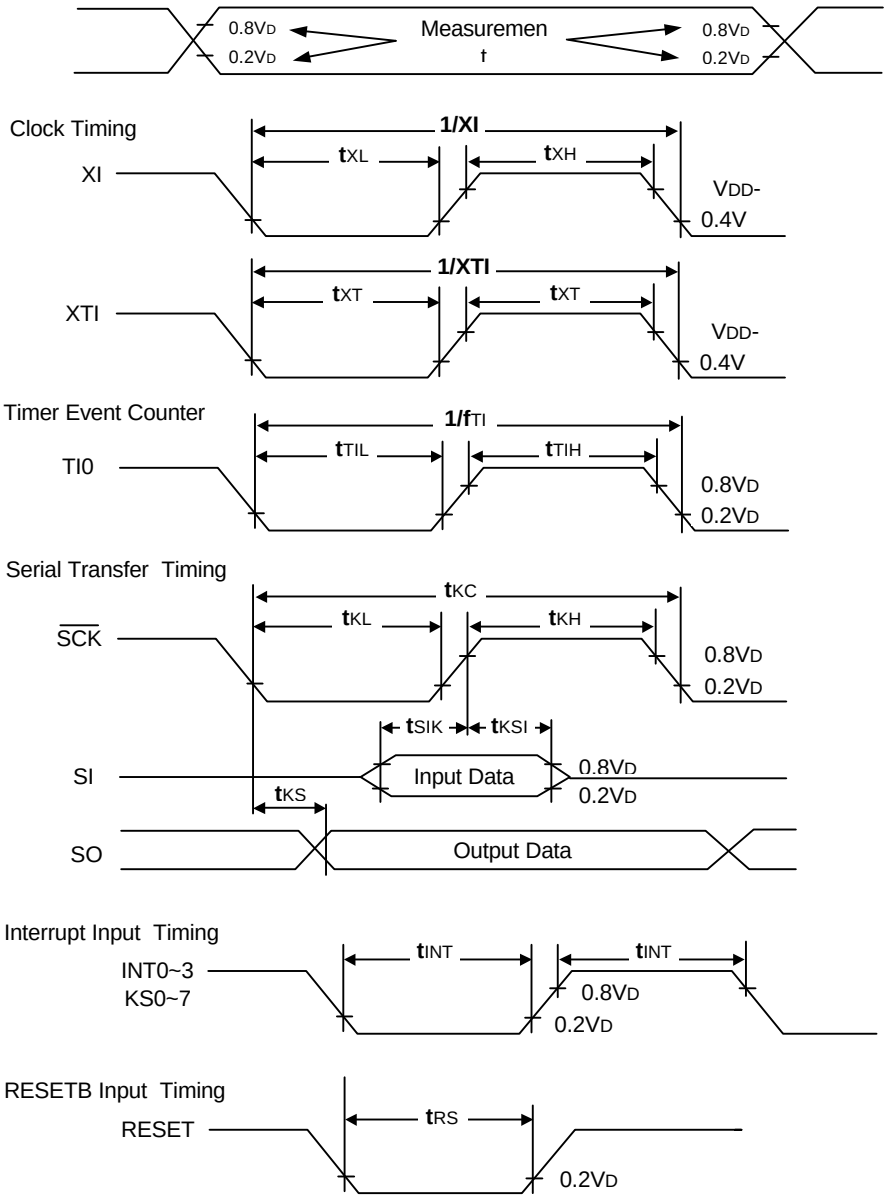
(2) Main system clock oscillation stops and the subsystem clock is used.

AC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85¡É, V_{DD} = 2.7 to 6.0V)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
System Clock Frequency	XI	Main	V_{DD} = 4.5 to 6.0V	0.4	4.19	4.5	MHz
	XTI	Sub		32	32.77	35	KHz
TI Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0V		0	-	1	MHz
		V_{DD} = 2.7 to 3.3V		0	-	275	KHz
TI Input High, Low Level Width	t_{TIH}	V_{DD} = 4.5 to 6.0V		0.48	-	-	us
	t_{TIL}			1.8	-	-	us
$\overline{SCK}$ Cycle Time	t_{KCY}	V_{DD} = 4.5 to	Input	0.8	-	-	us
			Output	0.95	-	-	us
		V_{DD} = 2.7 to	Input	3.2	-	-	us
			Output	3.8	-	-	us
$\overline{SCK}$ Input High, Low Level Width	t_{KH} t_{KL}	V_{DD} = 4.5 to	Input	0.4	-	-	us
			Output	t_{KCY}/2~50	-	-	us
		V_{DD} = 2.7 to	Input	1.6	-	-	us
			Output	t_{KCY}/2~150	-	-	us
SI Set up Time ($\overline{SCK}$ ↑	t_{SIK}			100	-	-	ns
SI Hold Time	t_{KSI}			400	-	-	ns
SO Output Delay Time	t_{KSO}	V_{DD} = 4.5 to		-	-	0.3	us
		V_{DD} = 2.7 to		-	-	1	us
INT0 ~ 2 High, Low Level Width	t_{INTH} t_{INTL}			5	-	-	us
RESETB Input Level L	t_{RSL}			10	-	-	us

AC Timing Measurement Points (Except XI and XTI)



RAM DATA RETENTION CHARACTERISTICS (in STOP Mode)

(T_A = -40 to +85¡É)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{DDDR}		2.0	-	6.0	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 2.0V	-	0.1	10	uA
Release Signal Set Time	t_{SREL}		0	-	-	uS
Oscillation Stabilization Wait Time	t_{WAIT}	When released by RESETB	-	2^{17}/fx	-	mS
		When released by interrupt Signal	-	NOTE 1)	-	mS

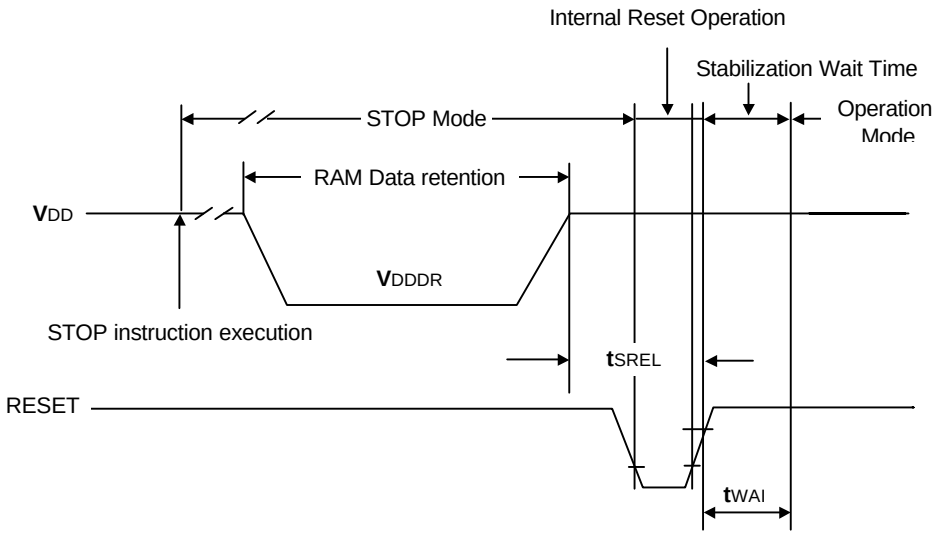
NOTE 1) Depends on the setting of the basic interval timer mode register.
(refer to the table below)

(fx = 4.19MHz)

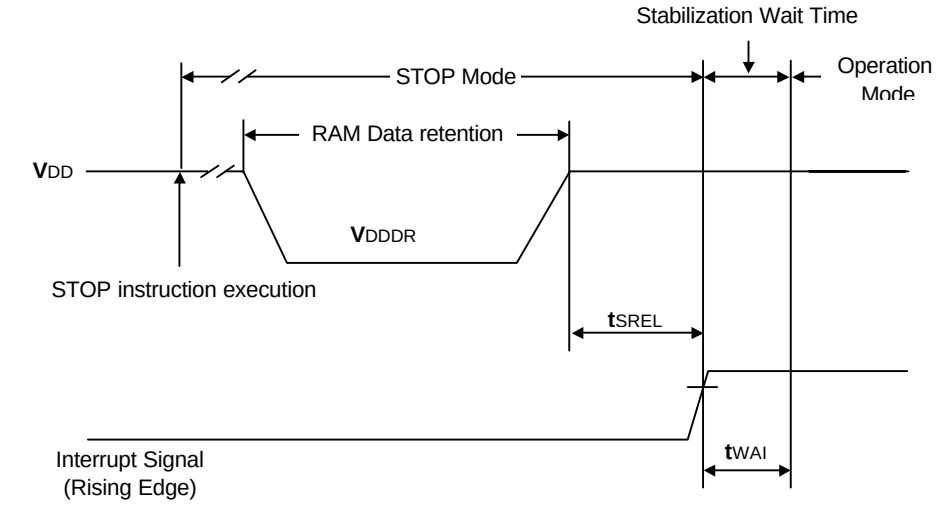
BMOD2	BMOD1	BMOD0	Oscillation Stabilization
0	0	0	2^{20}/fx (Approximately 250ms)
0	1	1	2^{17}/fx (Approximately 31.3ms)
1	0	0	2^{15}/fx (Approximately 7.82ms)
1	0	1	2^{13}/fx (Approximately 1.95ms)

RAM DATA RETENTION TIMING

When STOP mode is released by RESETB input



When STOP mode is released by interrupt signal

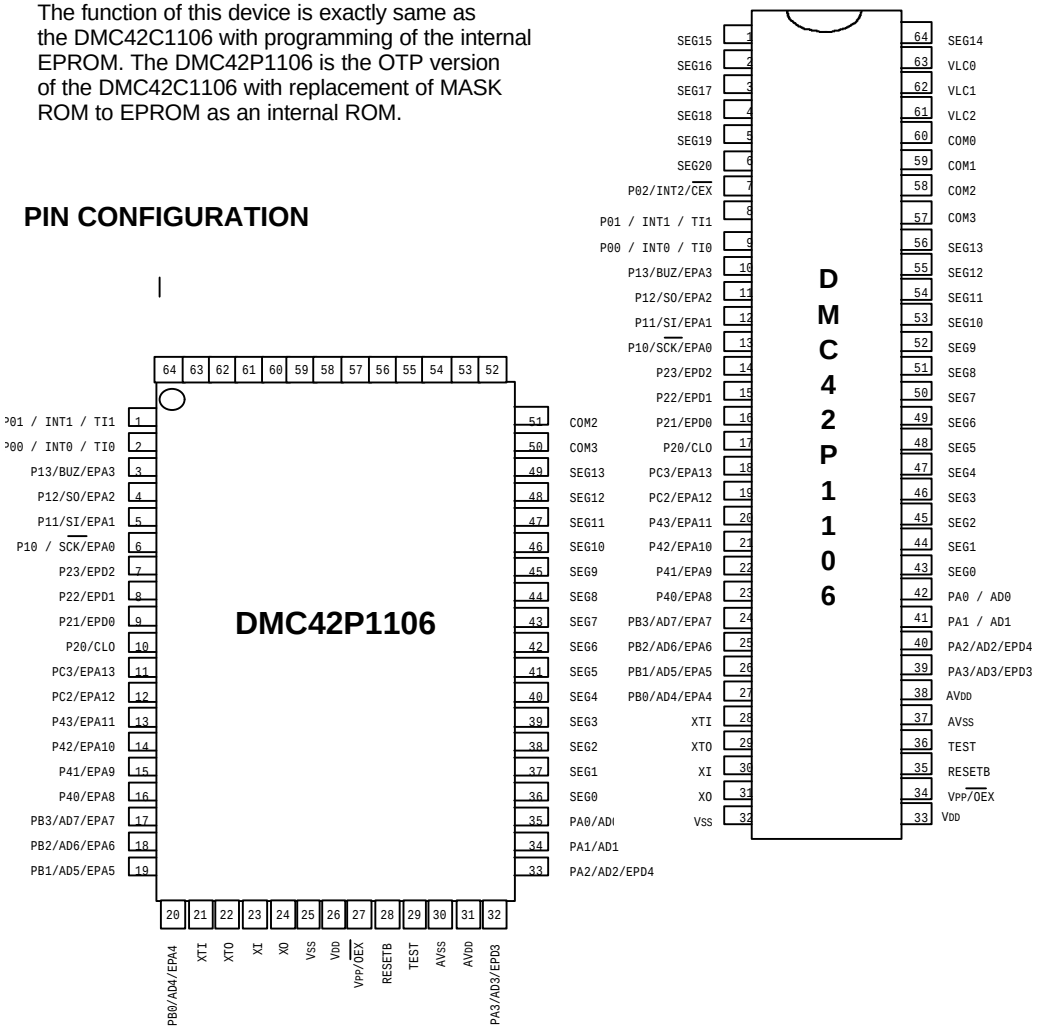


DMC42P1106

DESCRIPTION

The DMC42P1106 is a system evaluation LSI having a built in One-Time Programming circuit. A programming and verification for the internal EPROM is achieved by using a general EPROM programmer with an adapter socket.
The function of this device is exactly same as the DMC42C1106 with programming of the internal EPROM. The DMC42P1106 is the OTP version of the DMC42C1106 with replacement of MASK ROM to EPROM as an internal ROM.

PIN CONFIGURATION



DEVICE OPERATION

The operational modes of the DMC42P1106 are listed in Table 1.
A single 5V power supply is required in the read mode.
All inputs are TTL levels except for V_{PP} / $\overline{OEX}$.

V_{PP} = 12.5±0.5V

PINS / MODE	$\overline{CEX}$	V_{PP} / $\overline{OEX}$	V_{DD}	OUTPU
READ	V_{IL}	V_{IL}	5.0V	D_{OUT}
PROGRAM	V_{IL}	V_{PP}	6.0V	D_{IN}
VERIFY	V_{IL}	V_{IL}	6.0V	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	6.0V	High Z

TABLE 1. Operating Modes

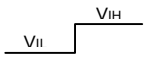
PIN NAME	MODE	
	EPROM MODE	USER MODE
TEST	V_{IL}	V_{IH}
RESETB	V_{IL}	

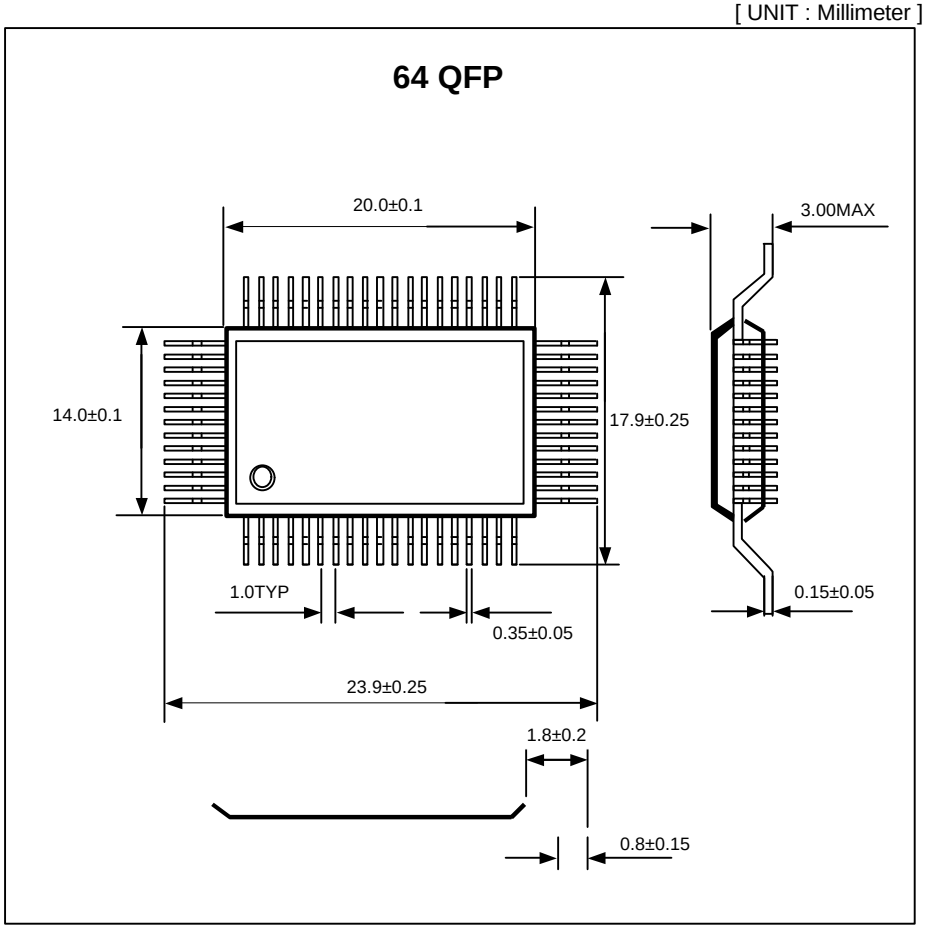
TABLE 2. The modes of DMC42P1106

DC PROGRAMMING CHARACTERISTICS

PARAMETER	SYMBO	TEST CONDITION	LIMIT		UNIT
			MIN.	MAX.	
Input Low Voltage	V_{IL}		-0.1	0.8	V
Input High Voltage	V_{IH}		2.0	V_{DD}	V
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	-	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = -400uA	2.4	-	V
Quick-pulse Programming	V_{PP}		12.5	13.0	V
Quick-pulse Programming	V_{DD}		6.0	6.5	V

PACKAGE DIMENSION

[UNIT : Millimeter]



PACKAGE DIMENSION

[UNIT : Millimeter]

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