Device
Engineering
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DEI1270A, DEI1271A
DUAL ARINC 429 LINE DRIVER WITH RATE SELECT and TRI-STATE

FEATURES

- Dual TTL/CMOS to ARINC 429 Line Driver
- HI/LO Speed Control Pins for Hi (100KBS) or Lo (12.5KBS) speed slew rates
- ±9.5V to ±16.5V supplies
- Drives full ARINC load
- Output resistor options: 0, 10 or 37.5 Ohms
- Tristate Output feature
- Thermally enhanced 5 x 7 mm MLP package
- The DEI1270A family is an improved version of the popular DEI1270 family

GENERAL DESCRIPTION

The DEI1270A/DEI1271A bipolar integrated circuits are dual line drivers designed to directly drive the ARINC 429 avionics serial digital data bus. The device converts TTL/CMOS serial input data to the tri-level RZ bipolar differential modulation format of the ARINC bus. A TTL/CMOS control input selects the output slew rate for HI (100KBS) and LOW (12.5KBS) speed operation. No external timing capacitors are required. A429 output tri-state capability is enabled by the TS_CTL input.

The DEI1270A/1A Line Drivers are an improved version of the popular DEI1270/1 family. They provide:

- Lower power consumption
- Excellent waveform fidelity
- Improved transient immunity. This improvement simplifies the equipment design for lightning and RF immunity requirements.

The Line Driver provides output resistor values and output tri-state capability (see table 1). There are three output resistor options: 0Ω, 10Ω and 37Ω. The 0Ω and 10Ω versions require external resistors to achieve the 37Ω output resistance of the ARINC 429 standard. The external resistors are normally used to simplify the external transient voltage protection network. The outputs are tri-state capable. This feature is useful in non-standard applications where there are multiple drivers on a wire pair.

TERMINAL DESCRIPTION

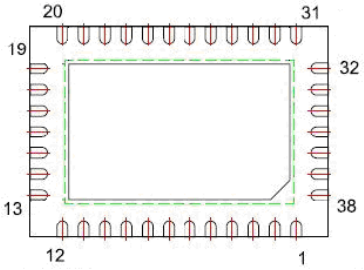


Table 1 Pin Description **Bottom View**

SIGNAL NAME	Channel 1 Pin	Channel 2 Pin	DESCRIPTION
HI/LO_n	**5**	**24**	**LOGIC INPUT.** Slew rate control. 1 = Hi speed. 0 = Low speed.
TTLIN0_n	**6**	**25**	**LOGIC INPUT.** Serial digital data input 0.
TTLIN1_n	**26**	**7**	**LOGIC INPUT.** Serial digital data input 1.
TS_CTL_n	**27**	**8**	**LOGIC INPUT.** Open or '1' disables output Tristate function. '0' Enables output Tristate function.
429OUTA_0_n	**34**	**15**	**429 OUTPUT.** ARINC 429 format serial digital data output A, 0 Ohm
429OUTA_10_n	**33**	**14**	**429 OUTPUT.** ARINC 429 format serial digital data output A, 10 Ohm
429OUTA_37_n	**32**	**13**	**429 OUTPUT.** ARINC 429 format serial digital data output A, 37 Ohm
429OUTB_0_n	**36**	**17**	**429 OUTPUT.** ARINC 429 format serial digital data output B, 0 Ohm
429OUTB_10_n	**37**	**18**	**429 OUTPUT.** ARINC 429 format serial digital data output B, 10 Ohm
429OUTB_37_n	**38**	**19**	**429 OUTPUT.** ARINC 429 format serial digital data output B, 37 Ohm
V+	**2**	**20**	**POWER INPUT.** +9.5 to +16.5 VDC.
GND	**28**	**9**	**POWER INPUT.** Ground.
V-	**30**	**12**	**POWER INPUT.** –9.5 to –16.5 VDC
NC	**1,3,4,10,11, 16, 21, 22, 23, 29, 31,35**		**No Internal Connect**

Note: The exposed pad is connected to the V- Supply on the DEI1270A and is electrically isolated on the DEI1271A.

FUNCTIONAL DESCRIPTION

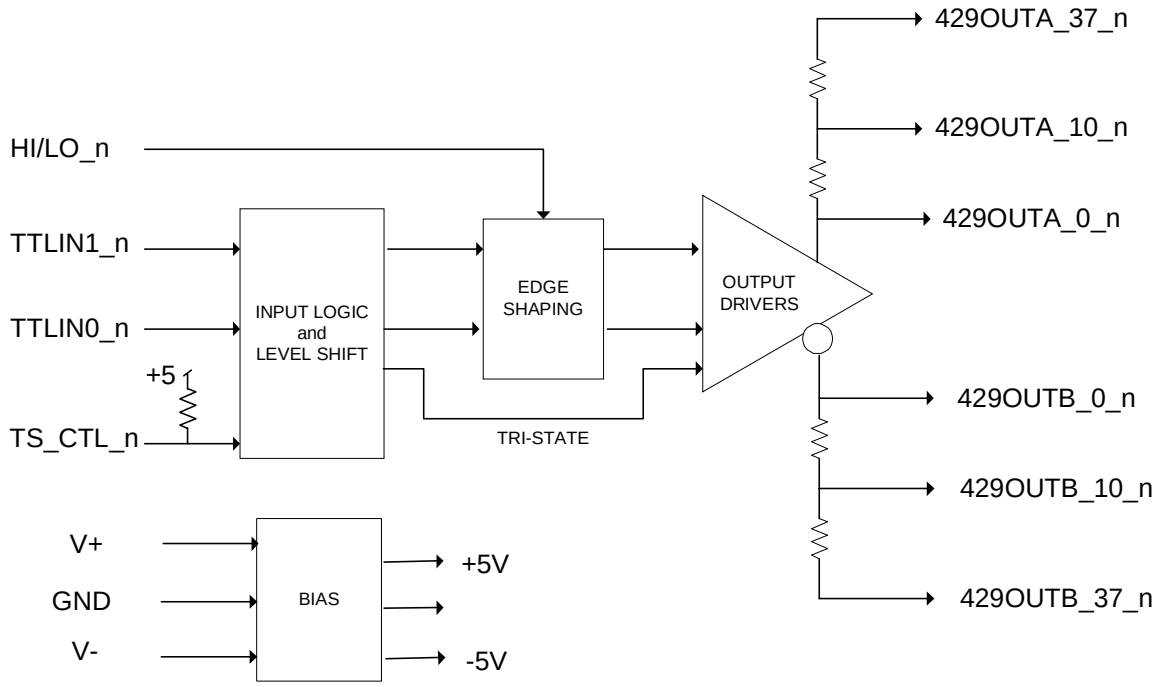


Figure 1 Block Diagram

One of Two Channels Shown

Table 2 Speed Control Function Table

HI/LO	OUTPUT TRANSITION TIME
L	10us (12.5KBS data)
H	1.5us (100KBS data)

Table 3 Transmit Data Function Table

TS_CTL_n	TTLIN1_n	TTLIN0_n	429OUTA	429OUTB	NOTES
X	0	0	0V	0V	Null output
X	0	1	-5V	5V	Zero output
X	1	0	5V	-5V	One output
1	1	1	0V	0V	Null output
0	1	1	Hi -Z	Hi-Z	Tri-state Output

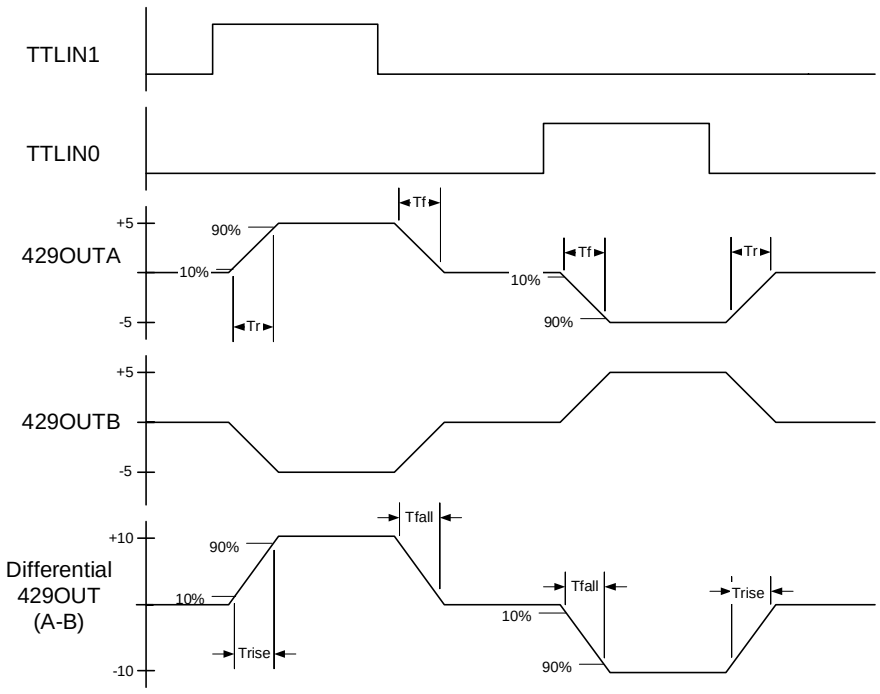


Figure 2 Line Driver Waveforms

ELECTRICAL DESCRIPTION

Table 4 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
V+ Supply Voltage	-0.3	+20	V
V- Supply Voltage	0.3	-20	V
Storage Temperature	-65	+150	°C
Input Voltage TTLIN, HI/LO, AND TS_CTL Inputs 429OUT Outputs (175us surge)	Gnd – 0.5	'V+' + 0.5	V
0 Ohm Output	'V-' – 1.0	'V+' + 1.0	V
10 Ohm Output	'V-' – 5.0	'V+' + 5.0	V
37 Ohm Output	'V-'– 20	'V-' – 20	V
Input Current 429OUT Outputs (175us surge)	-0.5	0.5	A
Power Dissipation @ 85°C 38L MLPQ, thermal pad soldered to heat spreader land		1.9	W
Junction Temperature: Tjmax		150	°C
ESD per JEDEC A114-A Human Body Model		2000	V
Peak body Temperature: 38L MLPQ		260	°C

Notes:
1. Stresses above absolute maximum ratings may cause permanent damage to the device.
2. The device is tolerant of one or both outputs shorted to Ground and of both outputs shorted together.
3. Voltages referenced to Ground

Table 5 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	V+ V-	9.5 to 16.5V -9.5 to –16.5V
Operating Temperature -xEx parts -xMx parts	T_{op}	 -55 to +85 °C -55 to +125 °C

Table 6 Electrical Characteristics

PARAMETER	TEST CONDITIONS (1)	SYMBOL	MIN	NOM	MAX	UNITS
LOGIC INPUTS						
Input Voltage, Logic 1		VIH	2.0		V+	V
Input Voltage, Logic 0		VIL	-0.3		0.8	V
Input Current, Logic 1	VIN = 5.0V	IIH	0	25	100	uA
Input Current, Logic 0	VIN = 0.0V	IIL	0	-20	-100	uA
ARINC OUTPUTS						
ARINC Output Voltage HI NULL LO	Single Ended Referenced to Ground No Load.	 VoHI VoNULL VoLO	 4.5 -0.25 -5.5	 5.0 0 -5.0	 5.5 +0.25 -4.5	 V V V
Output Tristate Leakage Current	Force output to -5V and +5V	Iz	-200		+200	uA
ARINC Output Short Circuit Current 0 Ohm output Output LO Output HI	External 37.5Ω resistor to GND	 IscLO IscHI	 100 -146	 133 -133	 146 -100	 mA mA
Output Resistance: 37 Ohm Output 10 Ohm Output 0 Ohm Output	Room Temperature Calculated from delta-Vout / delta-Iload Where Iload = 0 and 20mA See Figure 3	 Rout37 Rout10 Rout0	 24.3 6 0	 37.5 10 0.2	 50 13.5 2	 Ohms Ohms Ohms
Output Slew Rate, Hi Speed Lo to Hi and Hi to Lo transitions	HI/LO = 1 No Load, 10% to 90% single ended output	Tr/Tf	1		2	us
Output Slew Rate, Lo Speed Lo to Hi and Hi to Lo transitions	HI/LO = 0 No Load, 10% to 90% single ended output	Tr/Tf	5		15	us
SUPPLY CURRENT						
Quiescent Operating Supply Current, per channel IV+ IV-	V+ =15V, V- = -15V HI/LO = 0 or 1 TTLIN0=TTLIN1= 0V No Load	 IV+ IV-	 - -6.0	 3.0 -2.5	 6.0 -	 mA mA

Notes:

1. General Conditions: Tcase = rated operating temperature, -55/+85°C or -55/+125°C. V+/- = +/-9.5 to +/-16.5V
2. Unless otherwise noted, currents flowing in to DUT are positive, currents flowing out of DUT are negative, voltages are referenced to Ground.
3. Not production tested.

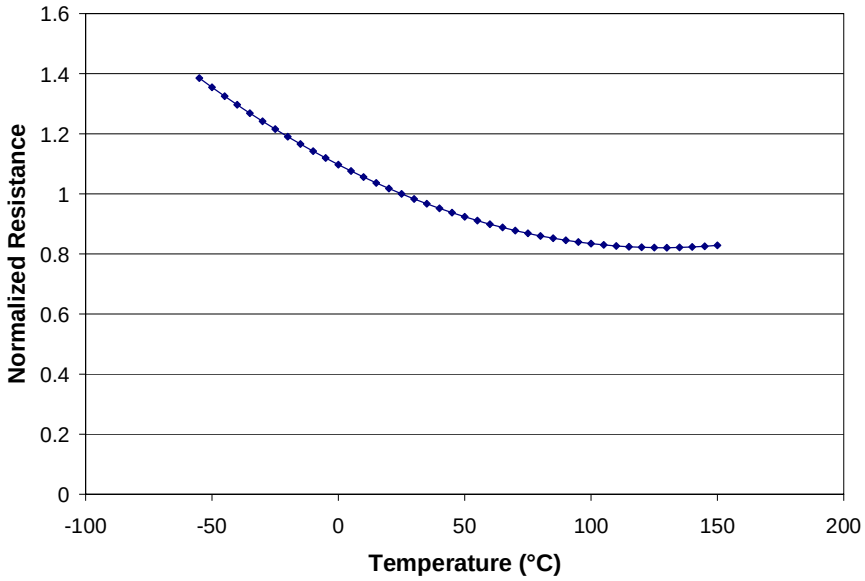


Figure 3 Normalized Output Resistance vs. Temperature

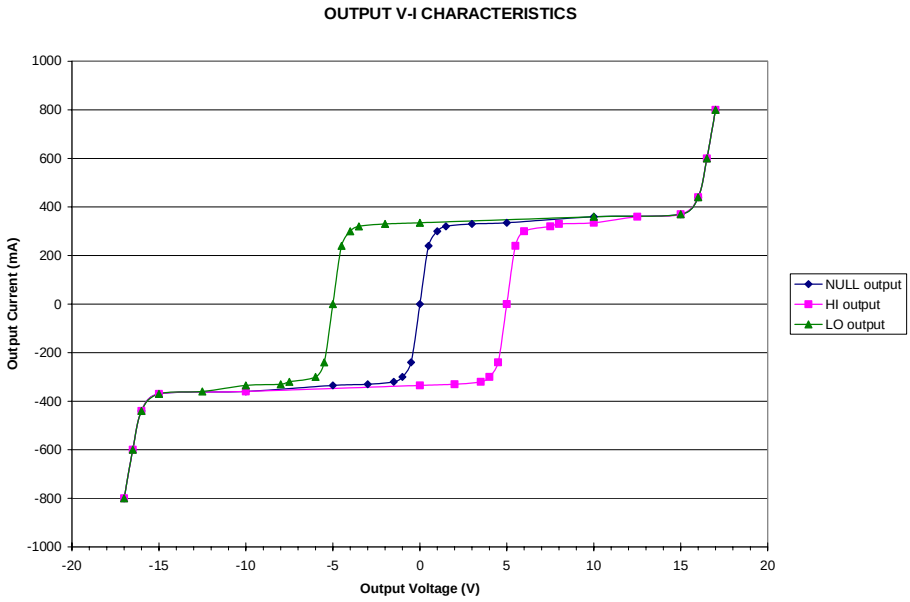


Figure 4 429OUT V-I Characteristics, ±15V supplies

DESIGN CONSIDERATIONS

Power Supplies and Bypass Capacitors

The DEI127XA Line Driver operates from ±9.5V to ±16.5V dual supplies. Proper bypassing ensures stability while driving large capacitive loads. The Line Driver requires a minimum of a 0.1uF bypass capacitor placed as close as possible to the V+ and V- pins.

Transient Voltage Protection

The DEI127xA Line Driver requires external components to achieve immunity from surges such as those defined by DO160D Section 22, "Lightning Induced Transient Susceptibility". Typical surge protection includes silicon Transient Voltage Suppressor (TVS) devices and may include all or part of the 37.5 Ohm output resistance as external resistors to limit the surge current.

The 127xA has a robust output stage which includes large driver devices and clamp diodes to the V+ and V- power rails as shown in Figure 5. It withstands surge currents of ±0.5A for 175us without damage when powered with ±15V supplies. At that surge current, the diodes clamp at ~1V above (below) the V+ (V-) supply rail. ~350mA flows to the V- (V+) supply through the output amplifier, and ~150ma flows to the V+ (V-) supply through the clamp diode. The outputs may be damaged by surges greater than 1A / 175us. At that current, the diodes clamp at ~1.8V above (below) the supply.

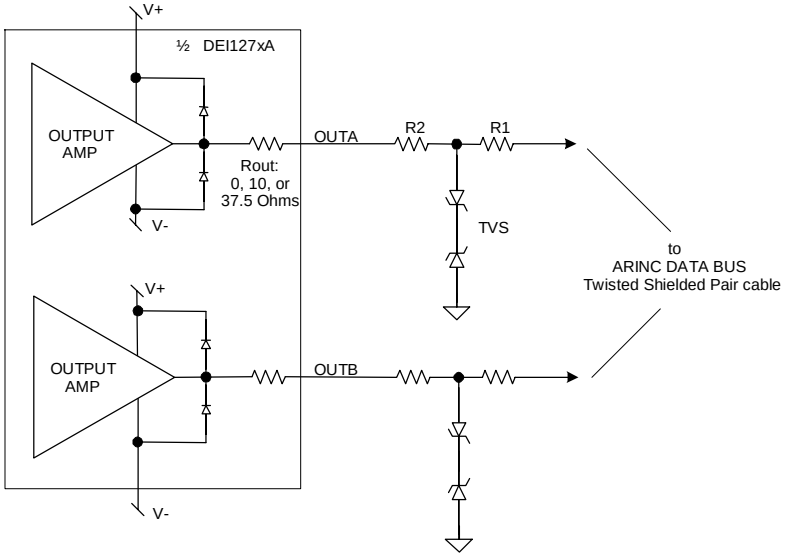


Figure 5 Surge Protection Network

The external lightning protection network should be designed to meet the specific requirements and constraints of the application equipment. The protection network should limit the OUTA/B pin surge current to the 0.5A / 175us maximum. The generalized circuit of Figure 5 represents several TVS protection network options:

- The on-chip Rout value is 0, 10, or 37 Ohms depending on the output pin used
- Select the total output resistance, Rout + R1 + R2, = 37 Ohms to meet ARINC bus requirements
  - Select R1 = 37Ω, R2 = 0Ω, Rout = 0Ω for lowest TVS surge current rating (smallest TVS devices)
  - Select R1 = 0Ω, Rout + R2 = 37Ω for highest TVS clamp voltage (20V + V+/-)
  - If the V+/V- supplies are un-powered or below operating voltage during the surge event, large currents may flow through the internal clamp diodes and damage the driver. If the application requires lightning immunity while un-powered, Select R1 = 0Ω, Rout + R2 = 37Ω, and select the TVS clamp voltage for <20V.
- Select TVS devices for the following
  - TVS Surge power/current rating must withstand the application requirements for Lightning Induced Transient Levels and Waveforms. Microsemi Corporation publishes an application note specific to the DO160 lightning requirements, available at: http://www.microsemi.com/micnotes/126.pdf
  - Select low capacitance TVS devices to minimize the load on the line driver. (Examples: Microsemi LC and HSMBJSA series TVS) This is a priority for Hi Speed ARINC applications where the low capacitance is important for optimum signal integrity and power consumption. Note that the maximum total capacitance on the ARINC bus is 30nF line to line.
  - Select the TVS clamp voltage at the lightning surge conditions such that the voltage/current into the 127XA OUT pin is within the safe region.
- If R1 is used to limit the TVS surge current, the resistor must withstand the surge current and voltage.

Alternate protection methods may be appropriate in some applications.

- External clamp diodes to the supply rails may be used to shunt surge current to the supply rails rather than to Ground.
- PTC "resetable fuses" may be used for R1 to protect the driver and TVS from shorts to 28V aircraft power.

Some general considerations related to Lightning Immunity:

- Analyze the TVS high current signal and ground return path to insure adequate surge current capability. The IR voltage and L*di/dt voltage in the ground return will add additional stress beyond the TVS clamp voltage.
- Observe suitable PCB design rules for traces subject to high voltage and high current surges.
- When possible, locate TVS devices close to the equipment connector to minimize the length of the surge voltage/current traces within the equipment.
- The shields of ARINC 429 data bus cables should be terminated to aircraft ground at all ends and at all bulkhead disconnects.

Thermal Management

Good thermal management is fundamental to Line Driver device reliability. It is particularly important in designs operating at the HI speed data rate (100KBS) with high capacitive loads as this produces maximum power dissipation. While the 127xA device will function at a junction temperature (Tj) above 190°C, it is inappropriate to continuously operate the plastic package above 150°C. Like all microcircuits, long term reliability is improved with lower operating temperatures.

The Line Driver's operating Tj is determined by internal power dissipation, package thermal resistance, and ambient temperature. The internal power dissipation (Pd) varies greatly with several variables:

- Data Rate – The Hi Speed (100kbs) rate produces maximum power dissipation
- Load – The maximum ARINC 429 load is 30nF||400 Ω line-to-line. Many applications only drive a fraction of the full load.
- Data Duty Cycle - ARINC bus activity, averaged over 10 seconds = Bits transmitted / total possible bits. Many applications are active <70%.
- Supply Voltage – V+/V- supply range is from ±9.5V to ±16.5V. Higher voltage => higher power
- Rout configuration - The power dissipated in the two 37Ω output resistors is internal to the IC for the 37 Ohm output configuration, and external for the 0 Ohm output configuration.

The internal power dissipation for 100kbs applications can be estimated from Figure 6. Pd for low speed operation (12.5kbs) is normally not an issue, so is not considered here. The curves in Figure 6 indicate Pd for various loads, supply voltage, and Rout configuration. It represents Pd for 100% Data Duty Cycle at 100KBS with no word gap null times. Thus the indicated Pd values are considered maximum values and should be reduced to account for the Data Duty Cycle as follows:

- Estimate DDC = total bits transmitted in 10 sec period / 1,000,000
  = 32 x total ARINC words transmitted in 10 sec period / 1,000,000
- Use Figure 6 to select an indicated Pd for the application supply voltage and load. This may involve estimating the Line Driver's load and interpolating between the curves.
- Calculate adjusted Pd = DDC * (Pd - 0.1) + 0.1 (W)
- **NOTE**: Apply this calculation to both channels. Total package power dissipation is the sum of the two channels.

The operating junction temperature is calculated as follows:

$Tj = Ta + Pd*\Theta ja$

where

Tj = junction temperature (°C)

Ta = Ambient temperature (°C)

Pd = Internal power dissipation (W)

Θja = IC package thermal resistance from junction to ambient (°C/W). Refer to package details.

The ARINC 429 Line Driver outputs may be subject to short circuit conditions due to cable wiring errors or faults which typically occur during equipment test and aircraft installation environments. The common cases are one or both outputs shorted to Ground, or both outputs shorted together. These conditions may cause considerable internal power dissipation depending on the following:

- Data Duty Cycle – The line-to-line and line-to-Ground shorts cause little or no power dissipation when the outputs are in the Null state. However when the output is driving a HI/LO state, the short circuit current is limited by the 37.5Ω Rout at about ~133mA. This is modulated by the ARINC waveform, producing an effective current of ~88mA* DDC. This current causes heating in the output amplifier and Rout resistor.

- Supply Voltage – A lower supply voltage results in lower Pd during short circuit conditions. The internal Pd for both outputs shorted while operating at 100% DDC is ~2W with ±15V supplies, but is reduced to ~1.5W with ±12V supplies. This is for 0Ω Rout configurations.
- Rout configuration – Each of the two 37.5Ω Rout resistors dissipates ~0.29W when shorted at 100% DDC. This power is dissipated in the external resistors for the 0 Ohm output configuration, and internal to the IC for the 37 Ohm output configuration. Thus the 0 Ohm and 10 Ohm configurations have a lower Tj and are more tolerant to short circuit conditions.

The PCB design and layout is a significant factor in determining thermal resistance (Θja) of the Line Driver IC package**.** Use maximum trace width on all power and signal connections at the IC. These traces serve as heat spreaders which improve heat flow from the IC terminals**.** The exposed heat sink pad of the MLP package should be soldered to a heat-spreader land pattern on the PCB designed to maximize heat flow to the inner layer Ground/Power planes. The land should include a grid of thermal VIAs, which drop down and connect to the buried copper plane(s). A typical VIA grid is 12mil holes on a 50mil pitch. The barrel is plated to about 1.0 ounce copper. Use as many VIAs as space allows. VIAs should be plugged to prevent voids being formed between the exposed pad and PCB heat-spreader land due to solder escaping by the capillary effect. This can be avoided by tenting the VIAs with solder mask. The 1271A exposed pad is electrically isolated, so the PCB land may be at any potential; typically Ground for the best heat sink. The 1270A exposed pad is electrically connected to the V- supply, so the PCB land must either be connected to that supply voltage or be electrically isolated. The thermal resistance of the 1270A package is lower than the 1271A because the electrically conductive die attach has superior thermal properties.

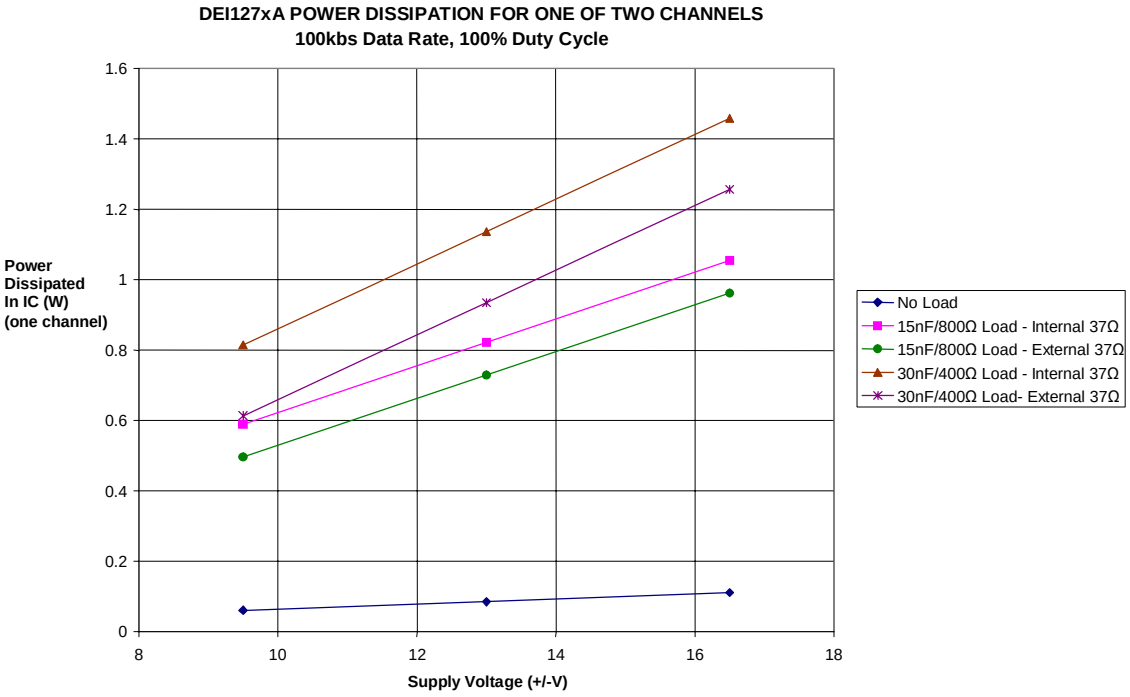


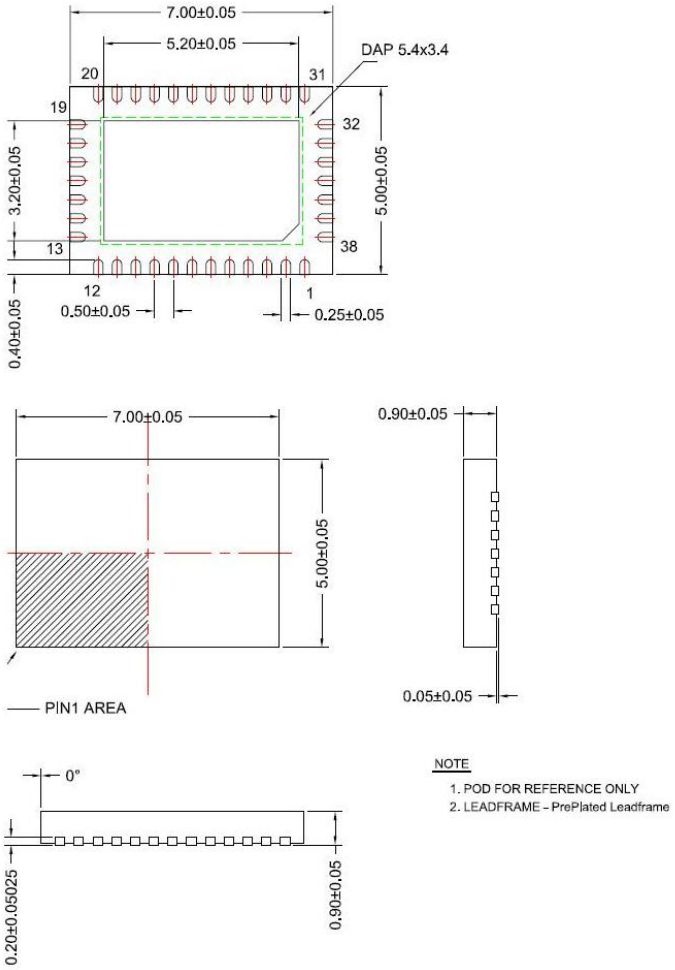
Figure 6 Internal Power Dissipation

ORDERING INFORMATION

Part Number	Marking	Package	Temperature
DEI1270A-MES-G	DE1270AMES	38L MLP - conductive	-55 / +85 ºC
DEI1271A-MES-G	DE1271AMES	38L MLP- isolated	-55 / +85 ºC
DEI1270A-MMS-G	DE1270AMMS	38L MLP - conductive	-55 / +125 ºC
DEI1271A-MMS-G	DE1271AMMS	38L MLP- isolated	-55 / +125 ºC

PACKAGE DESCRIPTION

38 Lead 5.0 x 7.0 MLP



Dimensions in mm

Table 7 38L MLP Characteristics Applicable to Both Packages

SYMBOL	DESCRIPTION	VALUE	UNITS
$Theta_{ja}$	Junction to Ambient. DEI1270A - Conductive pad DEI1271A - Isolated Pad 4 layer board with 2 internal power planes. Exposed pad soldered to PCB land with thermal vias to internal planes.	~34 ~40	°C/W
MSL	JEDEC Moisture Sensitivity Level Peak Body Temperature	1 260	- °C
	Lead Finish Pb Free Designation JEDEC Pb free code	NiPdAu RoHS compliant e4	