**CYIL1SM4000AA**

# LUPA 4000: 4 MegaPixel CMOS Image Sensor

## Features

- 2048 x 2048 active pixels
- 12 µm x 12 µm square pixels
- Optical format: 24.6 mm x 24.6 mm
- Monochrome or Color digital output
- 15 fps frame rate at full resolution
- 2 on-chip 10-bit ADCs
- Random programmable windowing and sub-sampling modes
- Full snapshot shutter
- Binning (voltage averaging in X-direction)
- Limited supplies: Nominal 2.5V (some supplies require 3.3V)
- Serial to Parallel Interface (SPI)
- 0°C to 60°C operational temperature range
- 127-pin PGA package
- Power dissipation: < 200 mW

## Applications

- Intelligent traffic system
- High speed machine vision

## Overview

This document describes the interfacing and driving of the LUPA 4000 image sensor. This 4 mega-pixel CMOS active pixel sensor features synchronous shutter and a maximal frame rate of 15 fps in full resolution. The readout speed can be boosted by sub-sampling and windowed Region of Interest (ROI) readout. High dynamic range scenes can be captured using the double and multiple slope functionality.

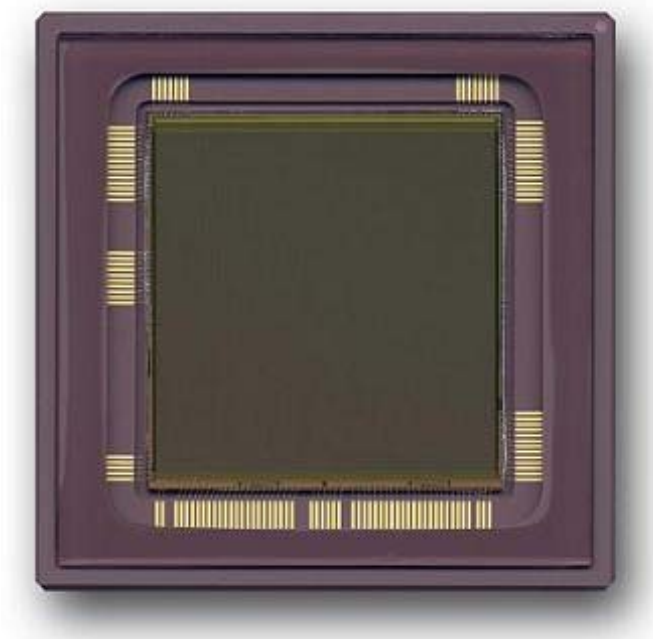
The sensor is used with one or two outputs. Two on-chip 10-bit ADCs are used to convert the analog data to a 10-bit digital word stream. The sensor uses a 3-wire SPI. It is housed in a 127-pin ceramic PGA package.

This data sheet allows the user to develop a camera system based on the described timing and interfacing.

The LUPA 4000 is available in color and monochrome without the cover glass.

For engineering samples, contact imagesensors@cypress.com.

**Figure 1. LUPA 4000 Photo**



### Part Number and Ordering Information

| Ordering Part Number | Monochrome/Color | Package |
|---|---|---|
| CYIL1SM4000AA-GDC | Monochrome with glass | 127-Pin PGA |
| CYIL1SM4000AA-GWCES | Monochrome windowless (Contact your local Cypress office) | |
| CYIL1SC4000AA-GDC | Color with glass | |
| CYIL1SM4000AA-GDCN | Nitrogen filled, monochrome with glass | |
| CYIL1SM4000-EVAL | LUPA 4000 demonstration kit | Demo Kit |

# Specifications

## General Specifications

**Table 1. General Specifications**

| Parameter | Specification |
|---|---|
| Active Pixels | 2048 (H) x 2048 (V) |
| Pixel Size | 12 μm x 12 μm |
| Pixel Type | 6 Transistor Pixel |
| Pixel Rate | 66 MHz using a 33 Mhz system clock and one or two parallel outputs |
| Shutter Type | Full Snapshot Shutter (integration during readout is possible) |
| Frame Rate | 15 fps at 4.0 Mpixel (can be boosted by sub sampling and windowing) |
| Master Clock | 33 MHz |
| Windowing (ROI) | Randomly programmable ROI read out |
| Read Out | Windowed, flipped, mirrored, and sub-sampled read out possible; voltage averaging in the x-direction |
| ADC Resolution | 2 on-chip, 10 bit |
| Sensitivity | 11.61 V/lux.s in the visible band only (180 lux=1 W/$m^2$) |
| Extended Dynamic Range | 66 dB (2000:1) in single slope operation and up to 90 dB in multiple slope operation |

## Electro-Optical Specifications

**Table 2. Electro-Optical Specifications**

| Parameter | Value |
|---|---|
| Conversion Gain | 13.5 uV/$e^-$ |
| Full Well Charge | 27000$e^-$ |
| Sensitivity | 2090 V.$m^2$/W.s Average white light |
| Fill Factor | 37.5% |
| Parasitic Light Sensitivity | <1/5000 |
| Dark Noise | 21$e^-$ |
| QE x FF | 37% at 680 nm |
| FPN | <1.25% rms of output signal amplitude of 1V |
| PRNU | <2.5% rms at 25% and 75% of output signal |
| Dark Signal | <140 mV/s at 21°C |
| Noise Electrons | < 40$e^-$ |
| S/N Ratio | 2000:1 at 66 dB (single slope operation) |
| MTF | 64% |
| Power Dissipation | <200 mW (typical without ADCs) |

**Figure 2. Spectral Response Curve for Mono**

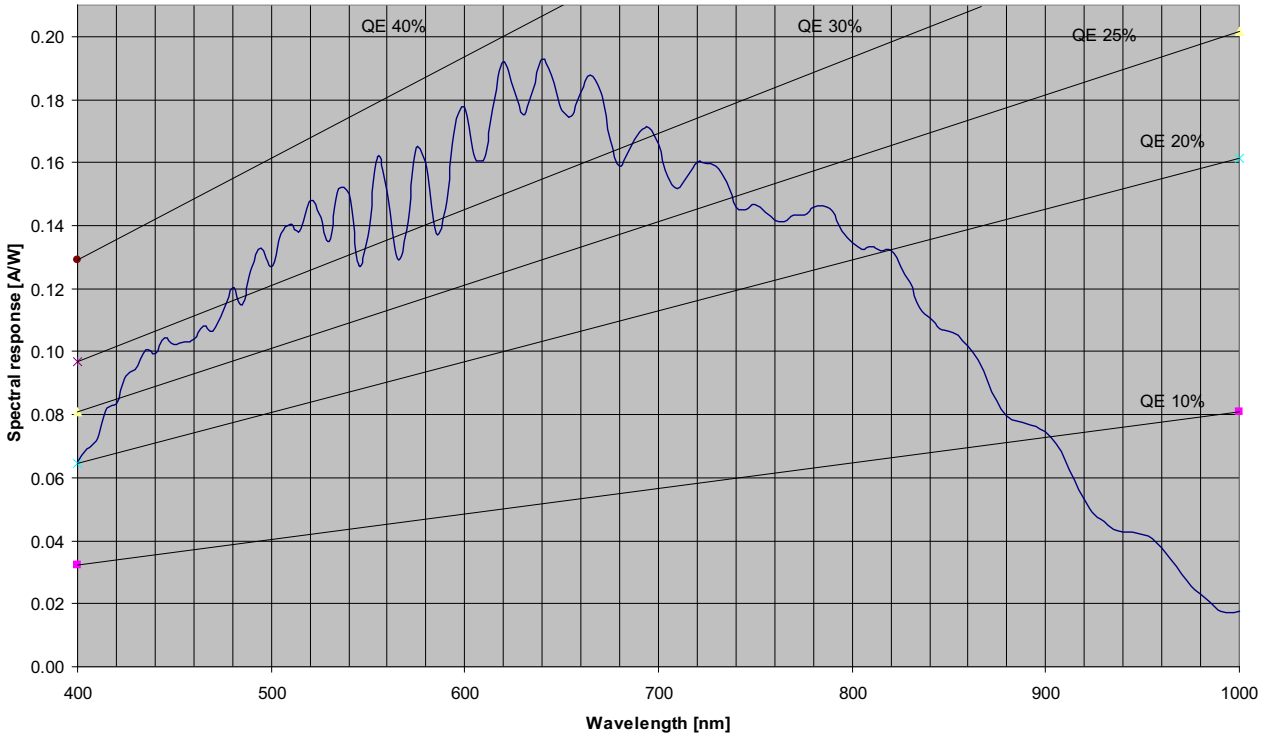



**Figure 3. Spectral Response Curve for Color**

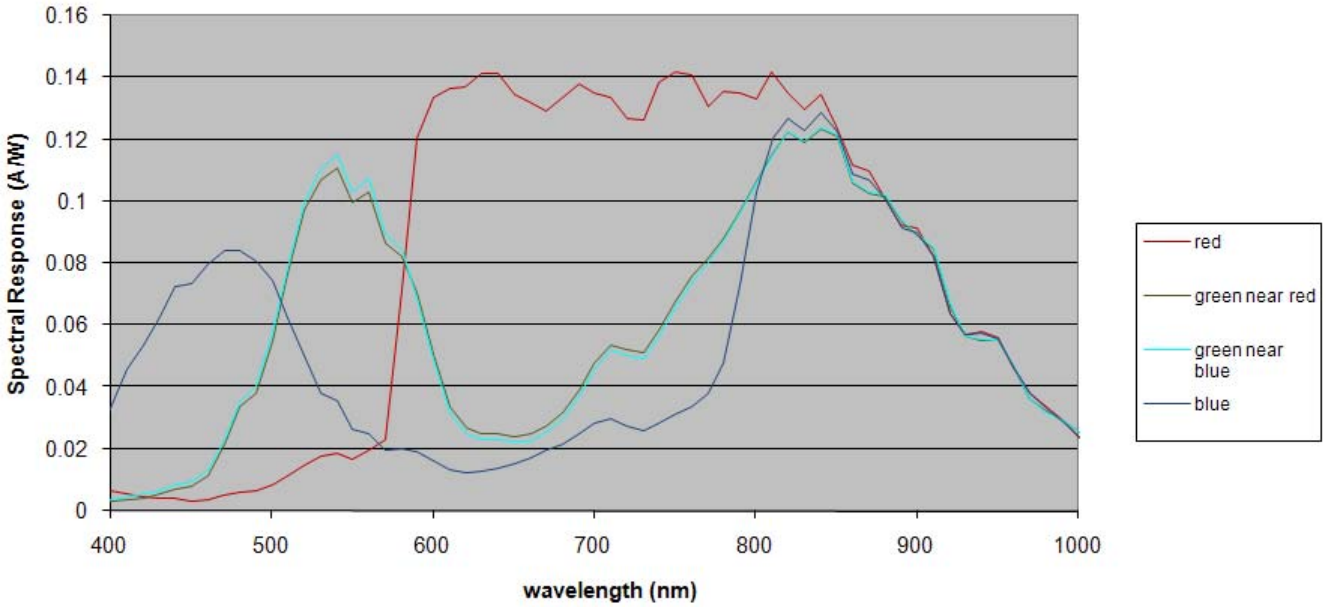



Figure 2 and Figure 3 show the spectral response characteristic. The curve is measured directly on the pixels. It includes effects of non sensitive areas in the pixel such as interconnection lines. The sensor is light sensitive between 400 nm and 1000 nm. The peak QE * FF is 37.5% approximately between 500 nm and 700 nm. In view of a fill-factor of 60%, the QE is thus larger than 60% between 500 nm and 700 nm.

**Figure 4. Photo-Voltaic Response Curve**

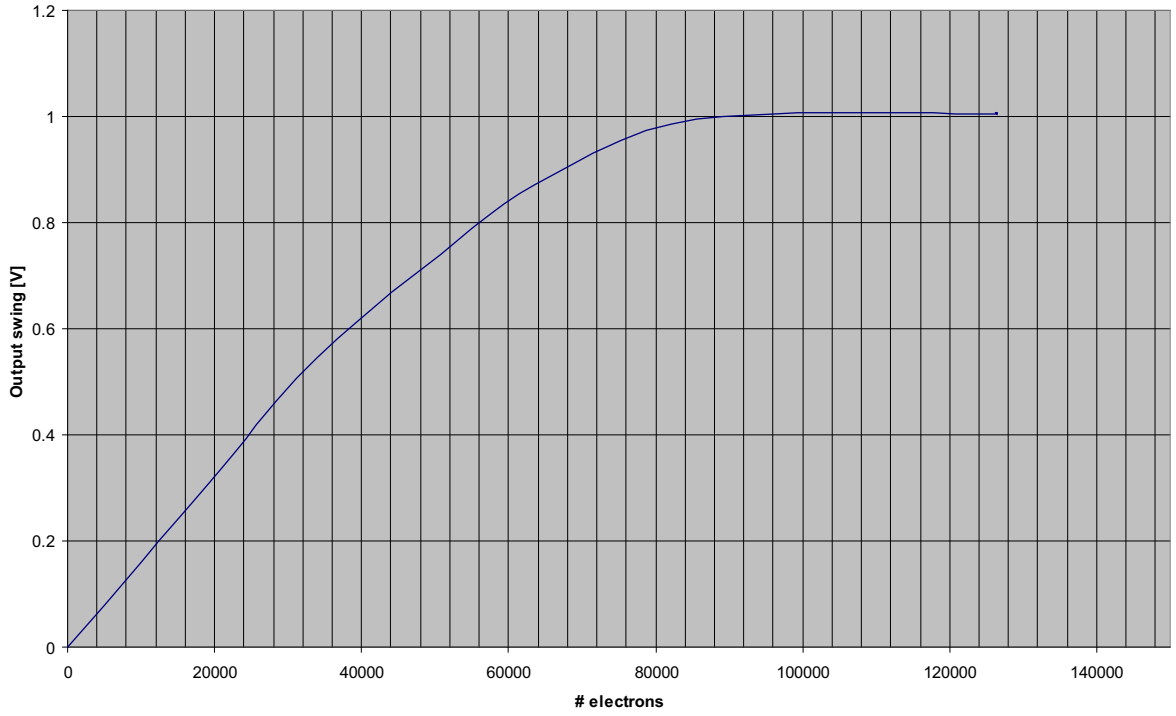



Figure 4 shows the pixel response curve in linear response mode. This curve is the relation between the electrons detected in the pixel and the output signal. The resulting voltage-electron curve is independent of any parameters. The voltage to electrons conversion gain is 13.5 µV/$e^-$.

Note that the upper part of the curve (near saturation) is actually a logarithmic response.

# Electrical Specifications

## Absolute Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device.

**Table 3. Absolute Maximum Ratings**[1]

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| Vdd | Core digital supply voltage | -0.5 | 2.9 | V |
| Voo | Output stage power supply | -0.5 | 2.9 | V |
| Vaa | Analog supply voltage | -0.5 | 2.9 | V |
| Va3 | Column readout module | -0.5 | 4.0 | V |
| Vpix | Pixel supply voltage | -0.5 | 2.9 | V |
| Vmem_l | Power supply memory element (low level) | -0.5 | 2.9 | V |
| Vmem_h | Power supply memory element (high level) | -0.5 | 4.0 | V |
| Vres | Power supply to the reset drivers | -0.5 | 4.0 | V |
| Vres_ds | Power supply to the multiple slope reset drivers | -0.5 | 2.9 | V |
| Vddd | Digital supply ADC circuitry | -0.5 | 2.9 | V |
| Vdda | Analog supply ADC circuitry | -0.5 | 2.9 | V |
| $I_{IO}$ | DC supply current drain per pin, any single input or output | -50 | 50 | mA |
| $T_L$ | Lead temperature (5 sec soldering) | | 350 | °C |
| $T_A$ | Ambient temperature range | 0 | 60 | °C |
| | ESD: Human Body Model and Charged Device Model | See Note [2] | | |

## Recommended Operating Conditions

The following specifications apply for $V_{DD}$= +2.5V. Boldface limits apply for $T_A$=$T_{MIN}$ to $T_{MAX}$, all other limits $T_A$=+25°C.

**Table 4. Recommended Operating Conditions**

| Symbol | Power Supply | Min Supply Tolerance | Recommended Supply Voltage for Optimal Performance (V) | Max Supply Tolerance |
|---|---|---|---|---|
| Vdd | Core digital supply voltage | -10% | 2.5 | +10% |
| Voo | Output stage power supply | -10% | 2.5 | +10% |
| Vaa | Analog supply voltage | -10% | 2.5 | +10% |
| Va3 | Column readout module | -1% | 3.3 | +1% |
| Vpix | Pixel supply voltage | -5% | 2.6 | +5% |
| Vmem_l | Power supply memory element (low level) | -5% | 2.6 | +5% |
| Vmem_h | Power supply memory element (high level) | -5% | 3.3 | +5% |
| Vres | Power supply to the reset drivers | -5% | 3.5 | +5% |
| Vres_ds | Power supply to the multiple slope reset drivers | -5% | 2.5 | +5% |
| Vddd | Digital supply ADC circuitry | -10% | 2.5 | +10% |
| Vdda | Analog supply ADC circuitry | -5% | 2.5 | +5% |
| Vpre_l | Power supply for precharge off-state | - 0.4V | 0 | 0V |

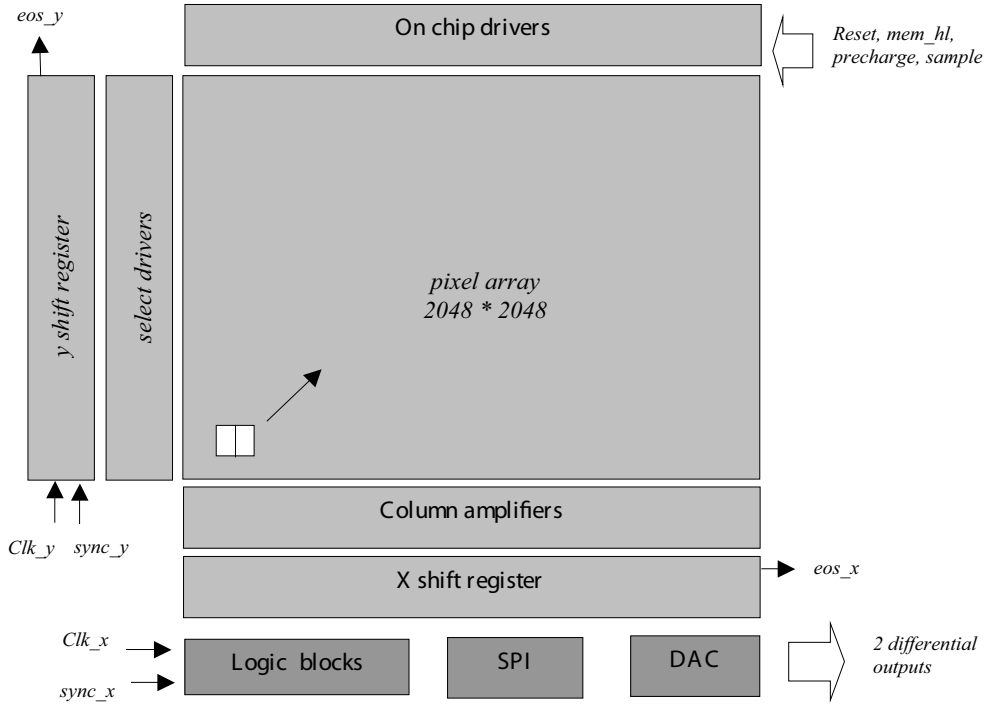
**Notes**
1. Absolute ratings are those values beyond which damage to the device may occur.
2. The LUPA 4000 complies with JESD22-A114 HBM Class 0 and JESD22-C101 Class I. It is recommended that extreme care be taken while handling these devices to avoid damages due to ESD event.

## Sensor Architecture

A schematic drawing of the architecture is given in Figure 5. The image core consists of a pixel array, one X-addressing and two Y-addressing registers (only one drawn), pixel array drivers and column amplifiers. The image sensor of 2048 x 2048 pixels is read out in progressive scan. One or two output amplifiers read out the image sensor. The output amplifiers are working at 66 MHz pixel rate nominal speed or each at 33 MHz pixel rate in case the two output amplifiers are used to read out the imager. The complete image sensor is designed for operation up to 66 MHz.

The structure allows having a programmable addressing in the x-direction in steps of two and in the y-direction in steps of two (only even start addresses in X-direction and Y-direction are possible). The starting point of the address is uploadable by means of the SPI

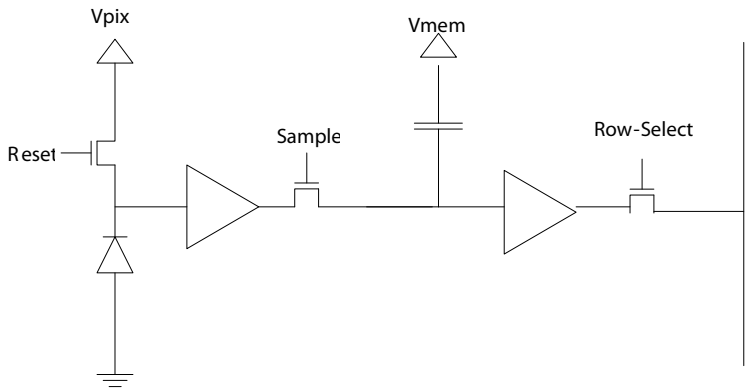
**Figure 5. Block Diagram of Image Sensor**




### The 6T Pixel

To obtain the global shutter feature combined with a high sensitivity and good Parasitic Light Sensitivity (PLS), the pixel architecture given in Figure 6 is implemented.

**Figure 6. 6T Pixel Architecture**




This pixel architecture is designed in a 12 μm x 12 μm pixel pitch. The pixel is designed to meet the specifications described in Table 1 and Table 2.

## Frame Rate and Windowing

*Frame Rate*

To acquire a frame rate of 15 frames/sec, the output amplifier should run at 66 MHz pixel rate or two output amplifiers should run at 33 MHz each, assuming a Row Overhead Time (ROT) of 200 ns.

The frame period of the LUPA 4000 sensor is calculated as follows:

Frame period = FOT + (Nr. Lines * (ROT + pixel period * Nr. Pixels) with: FOT: Frame Overhead Time = 5 µs.

Nr. Lines: Number of Lines read out each frame (Y).

Nr. Pixels: Number of pixels read out each line (X).

ROT: ROT = 200 ns (nominal; can be further reduced).

Pixel period: 1/66 MHz = 15.15 ns.

Example read out of the full resolution at nominal speed (66 MHz pixel rate):

Frame period = 5 µs + (2048 x (200 ns + 15.15 ns x 2048) = 64 ms ≥ 15 fps.

*ROI Readout (Windowing)*

Windowing is achieved by a SPI in which the starting point of the x-address and y-address is uploaded. This downloaded starting point initiates the shift register in the x-direction and y-direction triggered by the Sync_x and Sync_y pulse. The minimum step size for the x-address and the y-address is 2 (only even start addresses can be chosen). The size of both address registers is 10-bits. For instance, when the addresses 0000000001 and 0000000001 are uploaded, the readout starts at line 2 and column 2.

**Table 5. Frame Rate as Function of ROI Read Out and Sub Sampling**

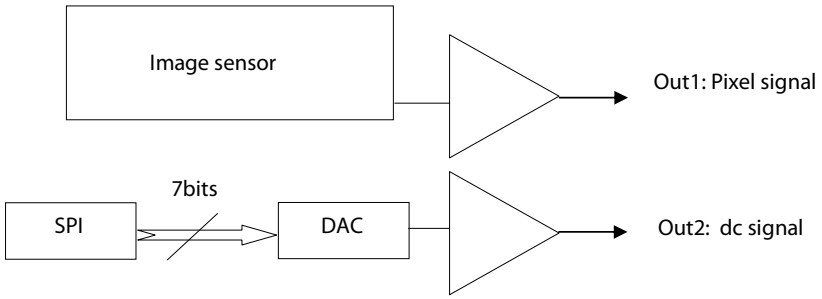
| Image Resolution (X*Y) | Frame Rate [frames f/S] | Frame Readout Time [mS] | Comment |
|---|---|---|---|
| 2048 x 2048 | 15 | 67 | Full resolution. |
| 1024 x 2048 | 31 | 32 | Subsample in X-direction. |
| 1024 x 1024 | 62 | 16 | ROI read out. |
| 640 x 480 | 210 | 4.7 | ROI read out. |

## Output Amplifier

The sensor has two output amplifiers. A single amplifier can be operated at 66 Mpixels/sec to bring the whole pixel array of 2048 by 2048 pixels at the required frame rate to the outside world. The second output amplifier can be enabled in parallel if the clock frequency is decreased to 33 Msamples/sec. Using only one output-stage, the output signal is the result of multiplexing between the two internal buses. When using two output-stages, both outputs are in phase.

Each output-stage has two outputs. One output is the pixel signal; the second output is a DC signal which offset can be programmed using a 7-bit word. The DC signal is used for common mode rejection between the two signals. The disadvantage is an increase in power dissipation. However, this can be reduced by setting the highest DAC voltage by means of the SPI

**Figure 7. Output Stage Architecture.**




The output voltage of Out1 is between 1.3V (dark level) and 0.3V (white level) and depends on process variations and voltage supply settings. The output voltage of Out2 is determined by the DAC.

## Pixel Array Drivers

We have foreseen on this image sensor on-chip drivers for the pixel array signals. Not only the driving on system level is easy and flexible, also the maximum currents applied to the sensor are controlled on chip. This means that the charging on sensor level is fixed and that the sensor cannot be overdriven from externally. The operation of the on-chip drivers is explained in detail in Timing and Readout of Image Sensor on page 13.

## Column Amplifiers

The column amplifiers are designed for minimum power dissipation and minimum loss of signal; for this reason, multiple biasing signals are required.

The column amplifiers also have the "voltage-averaging" feature integrated. In case of voltage averaging mode, the voltage average between two columns is taken and read out. In this mode only 2:1 pixels must be read out.

To achieve the voltage-averaging mode, an additional external digital signal called "voltage-averaging" is required in combination with a bit from the SPI.

## Analog to Digital Converter

The LUPA 4000 has two 10-bit Flash analog to digital converters running nominally at 10 Msamples/s. The ADC block is electrically separated from the image sensor. The inputs of the ADC must be tied externally to the outputs of the output amplifiers. If the internal ADC is not used, then the power supply pins to the ADC and the I/Os must be grounded.

Even in this configuration, the internal ADCs are not able to sustain the 66 Mpixel/sec provided by the output amplifier when run at full speed.

One ADC samples the even columns and the other samples the odd columns. Although the input range of the ADC is between 1V and 2V and the output range of the analog signal is only between 0.3V and 1.3V, the analog output and digital input may be tied to each other directly. This is possible because there is an on-chip level-shifter located in front of the ADC to lift up the analog signal to the ADC range.

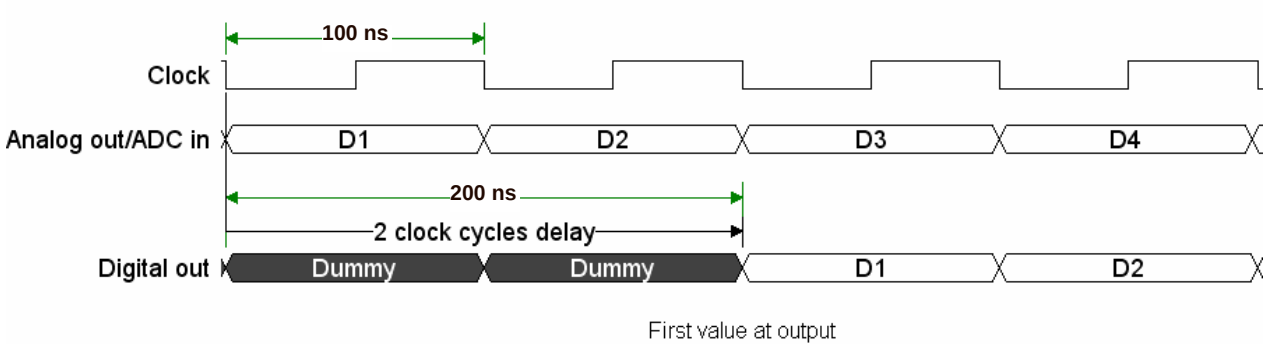
**Table 6. ADC Specifications**

| Parameter | Specification |
|---|---|
| Input range | 1V - 2V [3] |
| Quantization | 10 Bits |
| Nominal data rate | 10 Msamples/s |
| DNL (linear conversion mode) | Typ < 0.4 LSB RMS |
| INL (linear conversion mode) | Typ < 3.5 LSB |
| Input capacitance | < 2 pF |
| Power dissipation at 33 MHz | 50 mW |
| Conversion law | Linear/Gamma-corrected |

*ADC Timing*

The ADC converts the pixel data on the falling edge of the ADC_CLOCK but it takes 2 clock cycles before this pixel data is at the output of the ADC. This pipeline delay is shown in Figure 8.

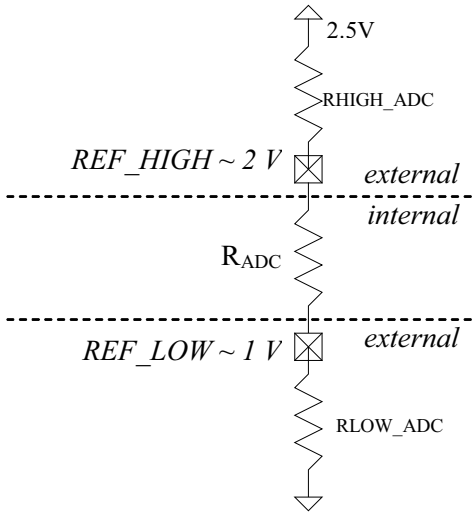
**Figure 8. ADC Timing**




**Note**
3. The internal ADC range is typ. 50 mV lower then the external applied ADC_VHIGH and ADC_VLOW voltages due to voltage drops over parasitic internal resistors in the ADC.

*Setting the ADC Reference Voltages*

**Figure 9. Internal and External ADC Connections**




The internal resistor $R_{ADC}$ has a value of approximately 300Ω. This value of this resistor is not tested at sort or at final test. Tweaking may be required as the recommended resistors in Figure 9 are determined by trade-off between speed and power consumption.

| Resistor | Typical Value (Ω) |
|---|---|
| $R_{ADC\_VHIGH}$ | 75 |
| $R_{ADC}$ | 300 |
| $R_{ADC\_VLOW}$ | 220 |

## Synchronous Shutter

In a synchronous (snapshot) shutter, light integration takes place on all pixels in parallel although subsequent readout is sequential.

**Figure 10. Synchronous Shutter Operation**

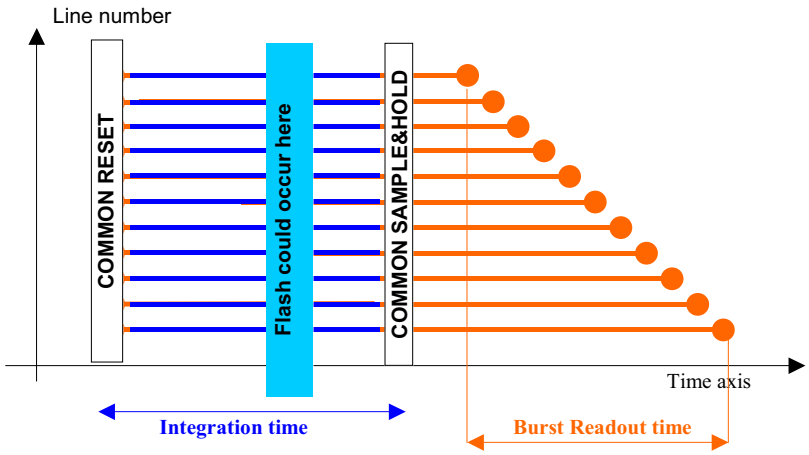
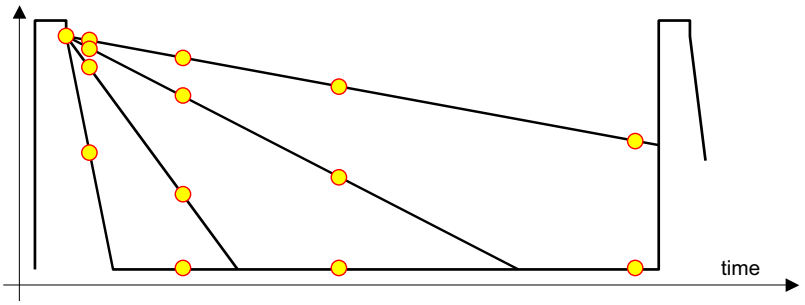



Figure 10 shows the integration and read out sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and read out cycle can occur in parallel or in sequential mode (see Timing and Readout of Image Sensor on page 13).

## Non Destructive Readout (NDR)

The sensor can also be read out in a non destructive way. After a pixel is initially reset, it can be read multiple times, without resetting. The initial reset level and all intermediate signals can be recorded. High light levels saturates the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, use the latest samples.

**Figure 11. Principle of NDR**




Essentially an active pixel array is read multiple times and reset only once. The external system intelligence takes care of the interpretation of the data. Table 7 summarizes the advantages and disadvantages of non-destructive readout.

**Table 7. Advantages and Disadvantages of NDR**

| Advantages | Disadvantages |
|---|---|
| Low noise, because it is true CDS. | System memory required to record the reset level and the intermediate samples. |
| High sensitivity, because the conversion capacitance is kept rather low. | Requires multiples readings of each pixel, thus higher data throughput. |
| High dynamic range, because the results includes signal for short and long integrations times. | Requires system level digital calculations. |

## Operation and Signalling

The different signals are classified into the following groups:

- Power supplies and grounds
- Biasing and analog signals
- Pixel array signals
- Digital signals
- Test signals

*Power Supplies and Ground*

Every module on chip including column amplifiers, output stages, digital modules, and drivers has its own power supply and ground. Off chip, the grounds can be combined, but not all power supplies may be combined. This results in several different power supplies, but this is required to reduce electrical cross-talk and to improve shielding, dynamic range, and output swing.

On chip, the ground lines of every module are kept separately to improve shielding and electrical cross talk between them.

An overview of the supplies is given in Table 8 and Table 9. Table 9 summarizes the supplies related to the pixel array signals and Table 8 summarizes the supplies related to all other modules

**Table 8. Power Supplies**

| Name | DC Current | Max Current | Typ | Description |
|---|---|---|---|---|
| Vaa | 7 mA | 50 mA | 2.5V | Power supply column readout module. |
| Va3 | 10 mA | 50 mA | 3.3V | Power supply column readout module. Should be tuneable to 3.3V max. |
| Vdd | 1 mA | 200 mA | 2.5V | Power supply digital modules |
| Voo | 20 mA | 20 mA | 2.5V | Power supply output stages |
| Vdda | 1 mA | 200 mA | 2.5V | Analog supply of ADC circuitry |
| Vddd | 1 mA | 200 mA | 2.5V | Digital supply of ADC circuitry |

**Table 9. Power Supplies Related to Pixel Signals**

| Name | DC Current | Max Current | Typ | Description |
|---|---|---|---|---|
| Vres | 1 mA | 200 mA | 3.5V | Power supply reset drivers. |
| Vres_ds | 1 mA | 200 mA | 2.5V | Power supply dual slope reset drivers. |
| Vmem_h | 1 mA | 200 mA | 3.3V | Power supply memory elements in pixel for high voltage level |
| Vmem_l | 1 mA | 200 mA | 2.6V | Power supply memory elements in pixel for low voltage level. Should be tuneable |
| Vdd | 1 mA | 200 mA | 2.5V | Core digital supply voltage |
| Vpix | 12 mA | 500 mA | 2.5V | Power supply pixel array |
| Vpre_l | 1 mA | 200 mA | 0V | Power supply for Precharge in off-state. This pin may be connected to ground. |

The maximum currents mentioned in Table 8 and Table 9 are peak currents which occur once per frame (except for Vres_ds in multiple slope mode). All power supplies should be able to deliver these currents except for Vmem_l and Vpre_l, which must be able to sink this current.

The maximum peak current for Vpix should not be higher than 500 mA. It is important to notice that no power supply filtering on chip is implemented and that noise on these power supplies can contribute immediately to the noise on the signal. The voltage supplies Vpix and Vaa must be noise free.

*Startup Sequence*

The LUPA 4000 goes in latch up (draw high current) as soon as all power supplies are turned on at the same time. The sensor comes out of latch up and starts working normally as soon as it is clocked. A power supply with a 400 mA limit is recommended to avoid damage to the sensor. It is recommended to avoid the time that the device is in the latch up state, so clocking of the sensor should start as soon as the system is turned on.

To completely avoid latch up of the image sensor, the following sequence should be taken into account:

1. Apply Vdd
2. Apply clocks and digital pulses to the sensor to count 1024 clock_x and 2048 clock_y pulses to empty the shift registers
3. Apply other supplies

*Biasing and Analog Signals*

The analog output levels that may be expected are between 0.3V for a white, saturated, pixel and 1.3V for a black pixel.

Two output stages are foreseen, each consisting of two output amplifiers, resulting in four outputs. One output amplifier is used for the analog signal resulting from the pixels. The second amplifier is used for a DC reference signal. The DC level from the buffer is defined by a DAC, which is controlled by a 7-bit word downloaded in the SPI. Additionally, an extra bit in the SPI defines if one or two output stages are used.

Table 10 summarizes the biasing signals required to drive this image sensor. To optimize biasing of column amplifiers to power dissipation, several biasing resistors are required. This optimisation results in an increase of signal swing and dynamic range.

**Table 10. Overview of Bias Signals**

| Signal | Comment | Related Module | DC Level |
|---|---|---|---|
| Out_load | Connect with 60 KΩ to Voo and capacitor of 100 nF to Gnd | Output stage | 0.7 V |
| dec_x_load | Connect with 2 MΩ to Vdd and capacitor of 100 nF to Gnd | X-addressing | 0.4 V |
| muxbus_load | Connect with 25 KΩ to Vaa and capacitor of 100 nF to Gnd | Multiplex bus | 0.8 V |
| nsf_load | Connect with 5 KΩ to Vaa and capacitor of 100 nF to Gnd | Column amplifiers | 1.2 V |
| uni_load_fast | Connect with 10 KΩ to Vaa and capacitor of 100 nF to Gnd | Column amplifiers | 1.2 V |
| uni_load | Connect with 1 MΩ to Vaa and capacitor of 100 nF to Gnd | Column amplifiers | 0.5 V |
| pre_load | Connect with 3 KΩ to Vaa and capacitor of 100 nF to Gnd | Column amplifiers | 1.4 V |
| col_load | Connect with 1 MΩ to Vaa and capacitor of 100 nF to Gnd | Column amplifiers | 0.5 V |
| dec_y_load | Connect with 2 MΩ to Vdd and capacitor of 100 nF to Gnd | Y-addressing | 0.4 V |
| psf_load | Connect with 1 MΩ to Vaa and capacitor of 100 nF to Gnd | Column amplifiers | 0.5 V |
| precharge_bias | Connect with 1kΩ to Vdd and capacitor of at least 200 nF to Gnd | Pixel drivers | 1.4V |

Each biasing signal determines the operation of a corresponding module in the sense that it controls speed and dissipation. Some modules have two biasing resistors: one to achieve the high speed and another to minimize power dissipation.

## Pixel Array Signals

The pixel array of the image sensor requires digital control signals and several different power supplies. This section explains the relation between the control signals and the applied supplies and the internal generated pixel array signals.

Figure 12 illustrates that the internal generated pixel array signals are Reset, Sample, Precharge, Vmem, and Row_select. These are internal generated signals derived by on-chip drivers from external applied signals. Row_select is generated by the y addressing and is not be discussed in this section.

The function of each of the signals is:

**Reset:** Resets the pixel and initiates the integration time. If reset is high, then the photodiode is forced to a certain voltage. This depends on Vpix (pixel supply) and the high level of reset signal. The higher these signals or supplies, the higher the voltage-swing. The limitation on the high level of Reset and Vpix is 3.3V. Nevertheless, there is no use increasing Vpix without increasing the reset level. The opposite is true. Additionally, it is this reset pulse that also controls the dual or multiple slope feature inside the pixel. By giving a reset pulse during integration, but not at full reset level, the photodiode is reset to a new value, only if this value is sufficient decreased due to light illumination.

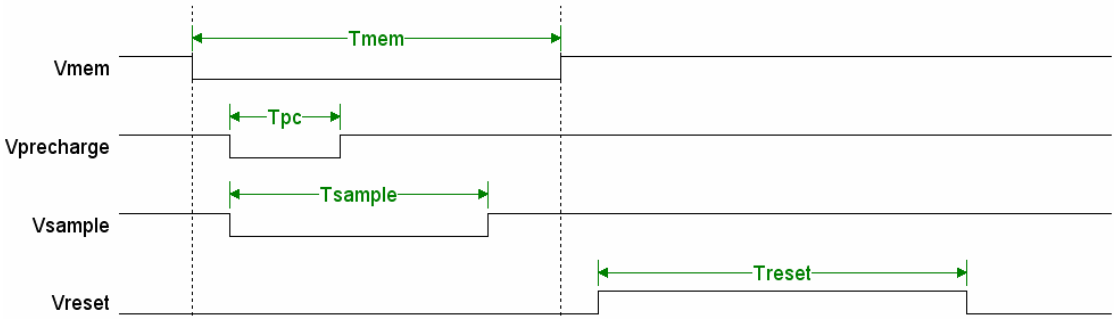
The low level of reset is 0V, but the high level is 2.5V or higher (3.3V) for the normal reset and a lower (<2.5V) level for the multiple slope reset.

**Precharge:** Precharge serves as a load for the first source follower in the pixel and is activated to overwrite the current information on the storage node by the new information on the photodiode. Precharge is controlled by an external digital signal between 0 and 2.5V.

**Sample:** Samples the photodiode information onto the memory element. This signal is also a standard digital level between 0 and 2.5V.

**Vmem:** This signal increases the information on the memory element with a certain offset. This increases the output voltage variation. Vmem changes between Vmem_l (2.5V) and Vmem_h (3.3V).

**Figure 12. Internal Timing of Pixel**
**(Levels are defined by the pixel array voltage supplies; for correct polarities of the signals refer to Table 11)**




The signals in Figure 12 are generated from the on-chip drivers. These on-chip drivers need two types of signals to generate the exact type of signal. It needs digital control signals between 0 and 3.3V (internally converted to 2.5V) with normal driving capability and power supplies. The control signals are required to indicate the moment they need to occur and the power supplies indicate the level.

Vmem is made of a control signal Mem_hl and 2 supplies Vmem_h and Vmem_l. If the signal Mem_hl is the logic '0' than the internal signal Vmem is low, if Mem_hl is logic '1' the internal signal Vmem is high.

Reset is made by means of two control signals: Reset and Reset_ds and two supplies: Vres and Vres_ds. Depending on the signal that becomes active, the corresponding supply level is applied to the pixel.

Table 11 summarizes the relation between the internal and external pixel array signals.

**Table 11. Overview of Internal and External Pixel Array Signals**

| Internal Signal | Vlow | Vhigh | External Control Signal | Low DC Level | High DC Level |
|---|---|---|---|---|---|
| Precharge | 0 | 0.45V | Precharge (AL) | Vpre_l | Controlled by bias-resistor |
| Sample | 0 | 2.5V | Sample (AL) | Gnd | Vdd |
| Reset | 0 | 2.5 to 3.3V | Reset (AH) and Reset_ds (AH) | Gnd | Vres and Vres_ds |
| Vmem | 2.0 to 2.5V | 2.5 to 3.3V | Mem_hl (AL) | Vmem_l | Vmem_h |

In case the dual slope operation is desired, you need to give a second reset pulse to a lower reset level during integration. This is done by the control signal Reset_ds and by the power supply Vres_ds that defines the level to which the pixel has to be reset.

Note that Reset is dominant over Reset_ds, which means that the high voltage level is applied for reset, if both pulses occur at the same time.

Note that multiple slopes are possible having multiple Reset_ds pulses with a lower Vres_ds level for each pulse given within the same integration time

The rise and fall times of the internal generated signals are not very fast (200 ns). In fact they are made rather slow to limit the maximum current through the power supply lines (Vmem_h, Vmem_l, Vres, Vres_ds, Vdd). Current limitation of those power supplies is not required. Nevertheless, it is advisable to limit the currents not higher than 400 mA.

The power supply Vmem_l must be able to sink this current because it must be able to discharge the internal capacitance from the level Vmem_h to the level Vmem_l. The external control signals should be capable of driving input capacitance of about 10 pF.

*Digital Signals*

The digital signals control the readout of the image sensor. These signals are:

- Sync_y (AH[4]): Starts the readout of the frame. This pulse synchronises the y-address register: active high. This signal is at the same time the end of the frame or window and determines the window width.
- Clock_y (AH[4]): Clock of the y-register. On the rising edge of this clock, the next line is selected.
- Sync_x (AH[4]): Starts the readout of the selected line at the address defined by the x-address register. This pulse synchronises the x-address register: active high. This signal is at the same time the end of the line and determines the window length.
- Clock_x (AH[4]): Determines the pixel rate. A clock of 33 MHz is required to achieve a pixel rate of 66MHz.
- Spi_data (AH[4]): the data for the SPI.
- Spi_clock (AH[4]): clock of the SPI. This clock downloads the data into the SPI register.
- Spi_load (AH[4]): when the SPI register is uploaded, then the data is internally available on the rising edge of SPI_load.
- Sh_kol (AL[5]): control signal of the column readout. Is used in sample and hold mode and in binning mode.
- Norowsel (AH[4]): Control signal of the column readout. (see Timing and Readout of Image Sensor).
- Pre_col (AL[5]): Control signal of the column readout to reduce row blanking time.
- Voltage averaging (AH[4]): Signal required obtaining voltage averaging of 2 pixels.

*Test Signals*

The test structures implemented in this image sensor are:

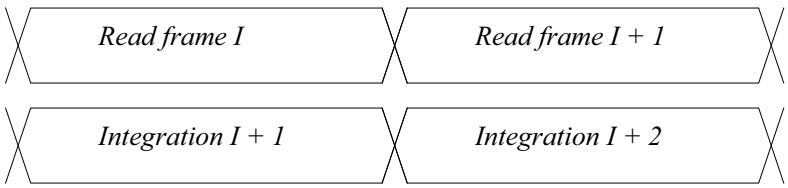
- Array of pixels (6*12) which outputs are tied together: used for spectral response measurement.
- Temperature diode (2): Apply a forward current of 10 µA to 100 µA and measure the voltage $V_T$ of the diode. $V_T$ varies linear with the temperature ($V_T$ decreases with approximately 1.6 mV/°C).
- End of scan pulses (do not use to trigger other signals):
  - Eos_x: end of scan signal: is an output signal, indicating when the end of the line is reached. Is not generated when doing windowing.
  - Eos_y: end of scan signal: is an output signal, indicating when the end of the frame is reached. Is not generated when doing windowing.
  - Eos_spi: output signal of the SPI to check if the data is transferred correctly through the SPI.

## Timing and Readout of Image Sensor

The timing of the LUPA 4000 sensor consists of two parts. The first part is related to the control of the pixels, the integration time, and the signal level. The second part is related to the readout of the image sensor. As full synchronous shutter is possible with this image sensor, integration time and readout can be in parallel or sequential.

In the parallel mode the integration time of the frame I is ongoing during readout of frame I-1. Figure 13 shows this parallel timing structure

**Figure 13. Integration and Readout in Parallel**

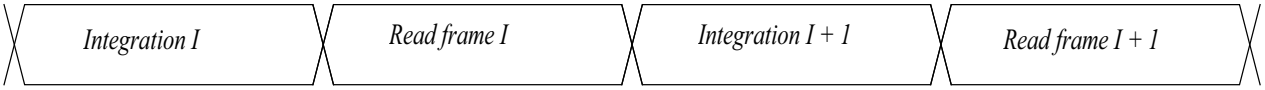



**Notes**
4. AH: Active High
5. AL: Active Low

The control of the frame's readout and integration time are independent of each other with the only exception that the end of the integration time from frame I+1 is the beginning of the readout of frame I+1.

The LUPA 4000 sensor is also used in sequential mode (triggered snapshot mode) where readout and integration is sequential. Figure 14 shows this sequential timing.

**Figure 14. Integration and Readout in Sequence**

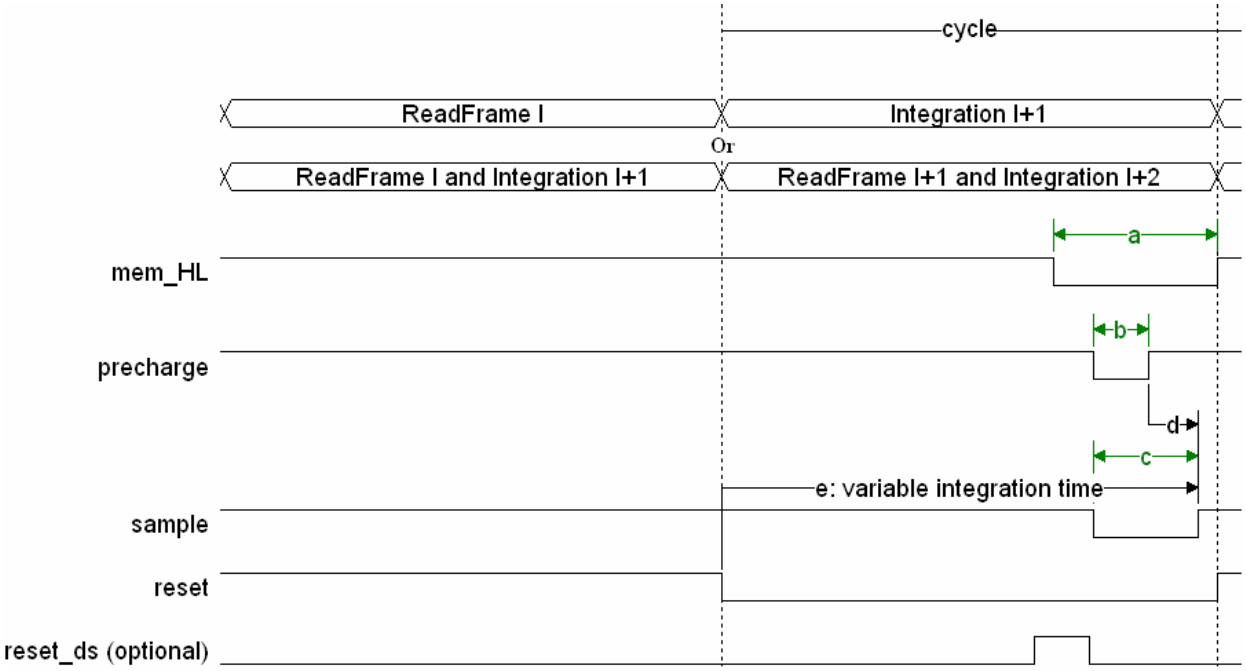



## Timing of Pixel Array

The first part of the timing is related to the timing of the pixel array. This implies control of integration time, synchronous shutter operation, and sampling of the pixel information onto the memory element inside each pixel. The signals required for this control are described in Pixel Array Signals and in Figure 12.

Figure 15 shows the external applied signals required to control the pixel array. At the end of the integration time from frame I+1, the signals Mem_hl, Precharge, and Sample must be given. The reset signal controls the integration time, which is defined as the time between the falling edge of reset and the rising edge of sample.

**Figure 15. Pixel Array Timing**
**(The integration time is determined by the falling edge of the reset pulse. The longer the pulse is high, the shorter the integration time. At the end of the integration time, the information has to be stored onto the memory element for readout.)**




Timing Specifications for each signal are shown in Table 12.

- Falling edge of Precharge is equal or later than falling edge of Vmem.
- Sample is overlapping with precharge.
- Rising edge of Vmem is more than 200 ns after rising edge of Sample.
- Rising edge of reset is equal or later than rising edge of Vmem.

**Table 12. Timing specifications**

| Symbol | Name | Value |
|---|---|---|
| a | Mem_HL | 5 - 8.2 µs |
| b | Precharge | 3 - 6 µs |
| c | Sample | 5 - 8 µs |
| d | Precharge-Sample | > 2 µs |
| e | Integration time | > 1 µs |

The timing of the pixel array is straightforward. Before the frame is read, the information on the photodiode must be stored onto the memory element inside the pixels. This is done with the signals Mem_hl, Precharge, and Sample. When Precharge is activated, it serves as a load for the first source follower in the pixel. Sample stores the photodiode information onto the memory element. Mem_hl pumps up this value to reduce the loss of signal in the pixel and this signal must be the envelop of Precharge and Sample. After Mem_hl is high again, the readout of the pixel array starts. The frame blanking time or frame overhead time is thus the time that Mem_hl is low, which is about 5 μs. After the readout starts, the photodiodes can all be initialised by reset for the next integration time. The minimal integration time is the minimal time between the falling edge of reset and the rising edge of sample. Keeping the slow fall times of the corresponding internal generated signals in mind, the minimal integration time is about 2 μs.

An additional reset pulse of minimum 2 μs can be given during integration by asserting Reset_ds to implement the double slope integration mode.

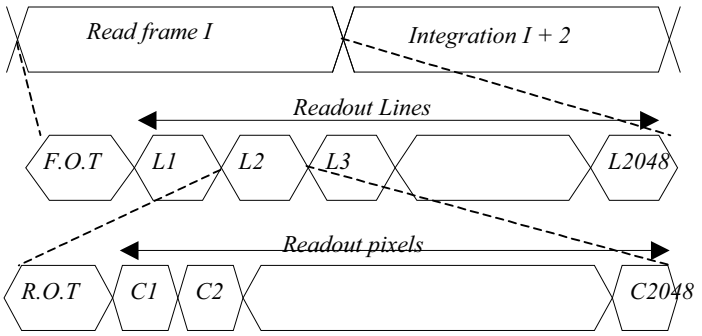
## Readout of Image Sensor

As soon as the information of the pixels is stored in to the memory element of each pixel, it can be readout sequentially. Integration and readout can also be done in parallel.

The readout timing is straightforward and is basically controlled by sync and clock pulses.

Figure 16 shows the top level concept of this timing. The readout of a frame consists of the frame overhead time, the selection of the lines sequentially, and the readout of the pixels of the selected line.

**Figure 16. Readout of Image Sensor**
**(F.O.T: Frame Overhead Time. R.O.T: Row Overhead Time. L: Selection of Line, C: Selection of Column)**




The readout of an image consists of the FOT (Frame overhead time) and the sequential selection of all pixels. The FOT is the overhead time between two frames to transfer the information on the photodiode to the memory elements. Figure 15 shows that at this time Mem_hl is low (typically 5 μs). After the FOT, the information is stored into the memory elements and a sequential selection of rows and columns makes sure the frame is read.

*X and Y Addressing*

To readout a frame the lines are selected sequentially. Figure 17 gives the timing to select the lines sequentially. This is done with a Clock_y and Sync_y signal. The Sync_y signals synchronises the y-addressing and initialises the y-address selection registers. The start address is the address downloaded in the SPI multiplied by two.

On the rising edge of Clock_y the next line is selected. The Sync_y signal is dominant and from the moment it occurs the y-address registers are initialised. If a Sync_y pulse is given before the end of the frame is reached, only a part of the frame is read. To obtain a correct initialisation, Sync_y must contain at least one rising edge of Clock_y when it is active.

**Figure 17. X and Y Addressing**

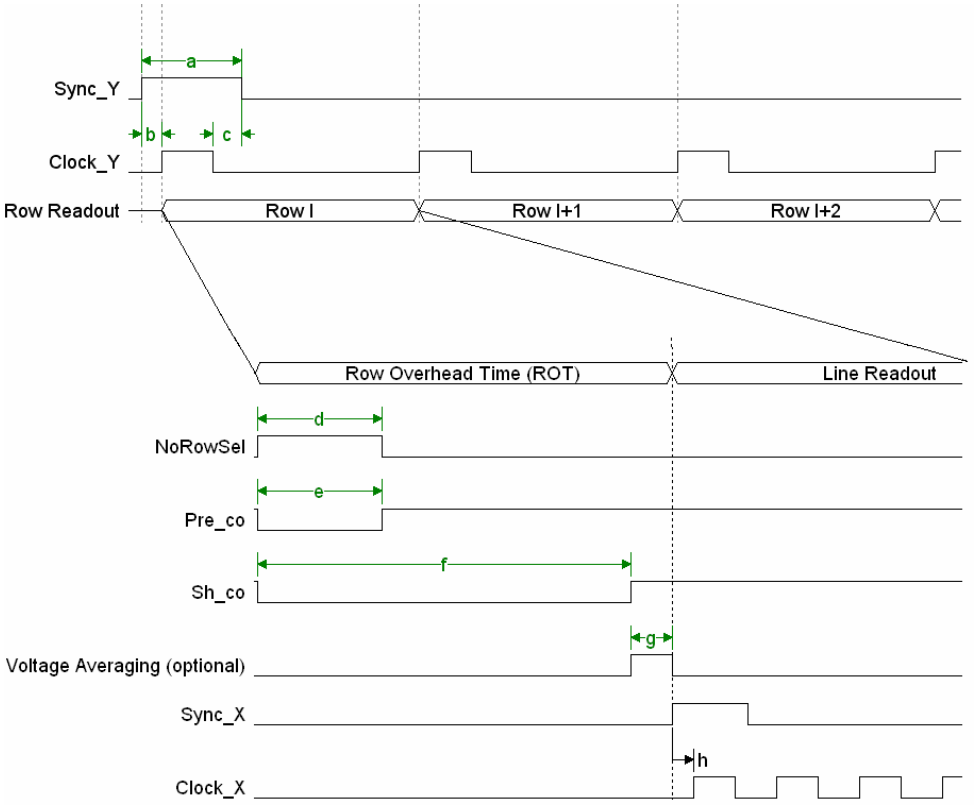



**Table 13. Readout Timing Specifications**

| Symbol | Name | Value |
|---|---|---|
| a | Sync_Y | >20 ns |
| b | Sync_Y-Clock_Y | >0 ns |
| c | Clock_Y-Sync_Y | >0 ns |
| d | NoRowSel | >50 ns |
| e | Pre_col | >50 ns |
| f | Sh_col | 200 ns |
| g | Voltage averaging | >20 ns |
| h | Sync_X-Clock_X | >0 ns |

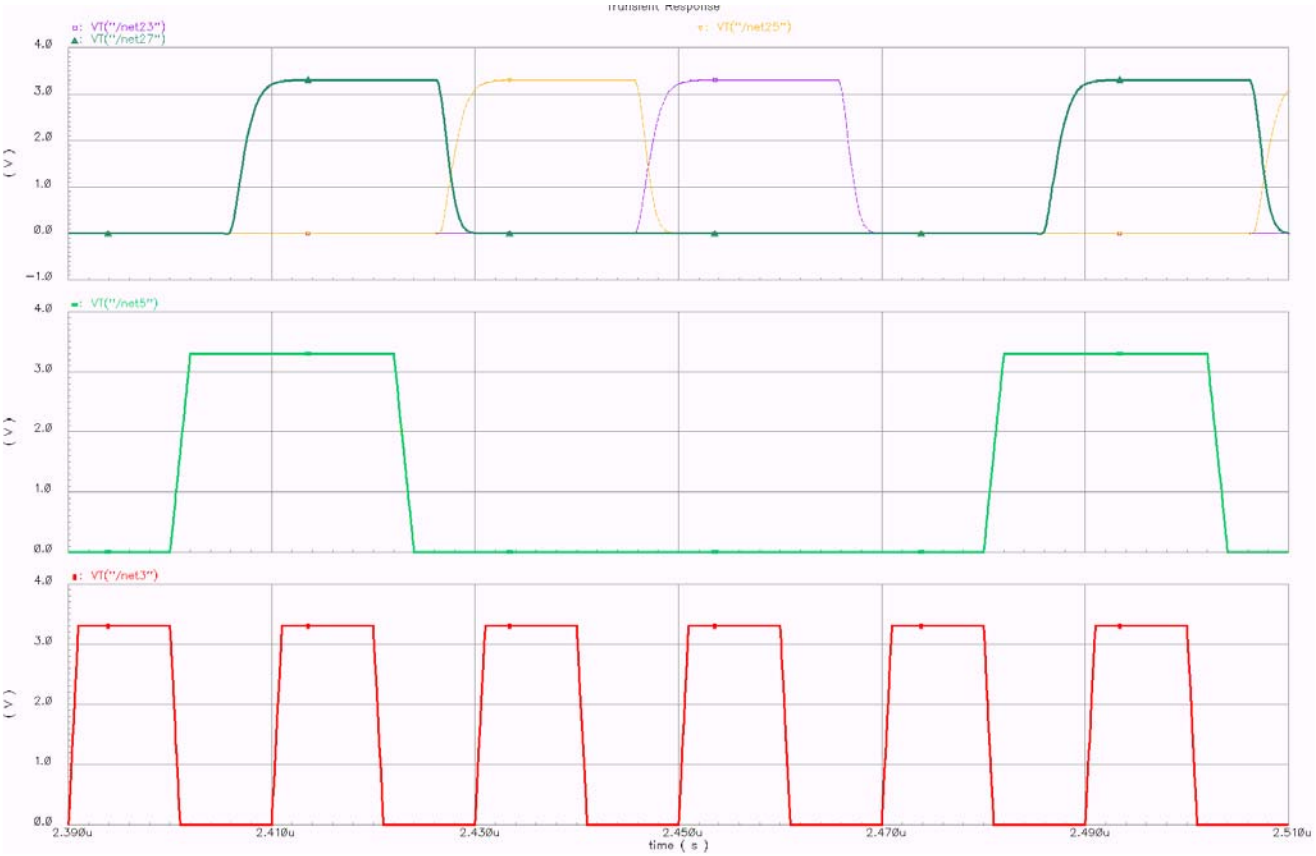
As soon as a new line is selected, it must be read out by the output amplifiers. Before the pixels of the selected line can be multiplexed onto the output amplifiers, wait for a certain time, indicated as the ROT or Row overhead time shown in Figure 17. This is the time to get the data stable from the pixels to the output bus before the output stages. This ROT is in fact lost time and rather critical in a high speed sensor. Different timings to reduce this ROT are explained later in this section.

During the selection of one line, 2048 pixels are selected. These 2048 pixels must be read out by one (or two) output amplifier.

Note that the pixel rate is the double frequency of the Clock_x frequency. To obtain a pixel rate of 66 MHz, apply a pixel clock Clock_x of 33MHz. When only one analog output is used, two pixels are output every Clock_x period. When Clock_x is high, the first pixel is selected; when Clock_x is low, the next pixel is selected. Consequently, during one complete period of Clock_x two pixels are read out by the output amplifier.

If two analog outputs are used each Clock-X period one pixel is presented at each output.

**Figure 18. X-Addressing**
**Clock_x, Sync_x, internal selection pixel 1 and 2, internal selection pixel 3 and 4, internal selection pixel 5 and 6**



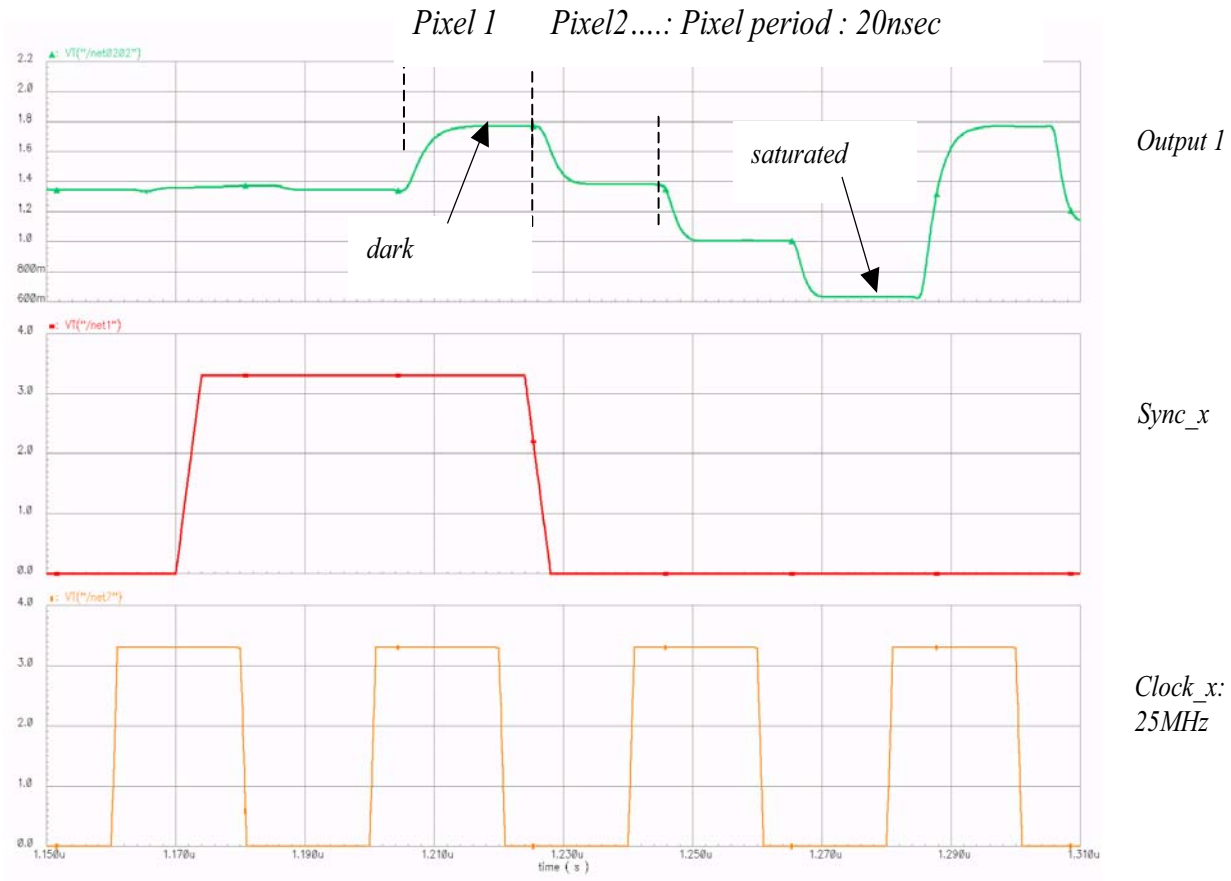

The first pixel selected is the x-address downloaded in the SPI. The starting address is the number downloaded into the SPI, multiplied with 2.

Windowing is achieved by a starting address downloaded in the SPI and the size of the window. In the x-direction, the size is determined by the moment a new Clock_y is given. In the y-direction, the sync_y pulse determines the size. The best way to obtain a certain window is by using an internal counter in the controller.

Figure 18 is the simulation result after extraction of the layout module from a different sensor to show the principle. In this figure the pixel clock has a frequency of 50 MHz, which results in a pixel rate of 100 Msamples/sec.

Figure 19 shows the relation between the applied Clock_x and the output signal.

**Figure 19. Output Signal Related to Clock_x Signal**
**From bottom to top: Clock_x, Sync_x and output. Output level before the first pixel is the level of the last pixel on previous line**




As soon as Sync_x is high and one rising edge of Clock_x occurs, the pixels are brought to the analog outputs. This is again the simulation result of a comparable sensor to show the principle.

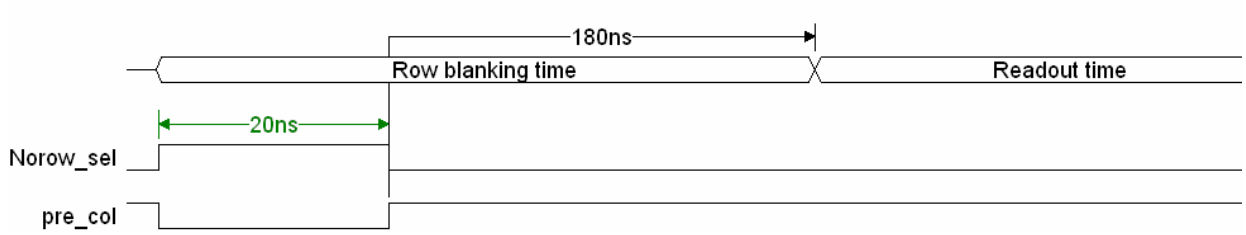
Note the time difference between the clock edge and the moment the data is seen at the output. As this time difference is very difficult to predict in advance, it is advisable to have the ADC sampling clock flexible to set an optimal Add sampling point. The time differences can easily vary between 5 ns and 15 ns and must be tested on the real devices.

*Reduced ROT Timing*

The row overhead time is the time between the selection of lines that you must wait to get the data stable at the column amplifiers. It is a loss in time, which should be reduced as much as possible.

### Standard Timing (200 ns)

**Figure 20. Standard Timing for the ROT**
**Only pre_col and Norowsel control signals are required**




In this case, the control signals Norowsel and pre_col are made active for about 20 ns from the moment the next line is selected. The time these pulses must be active is related to the biasing resistance Pre_load. The lower this resistance, the shorter the pulse duration of Norowsel and pre_col may be. After these pulses are given, wait for at least 180 ns before the first pixel is sampled. For this mode Sh_col must be made active (low) all the time.

#### Backup Timing (ROT =100-200 ns)

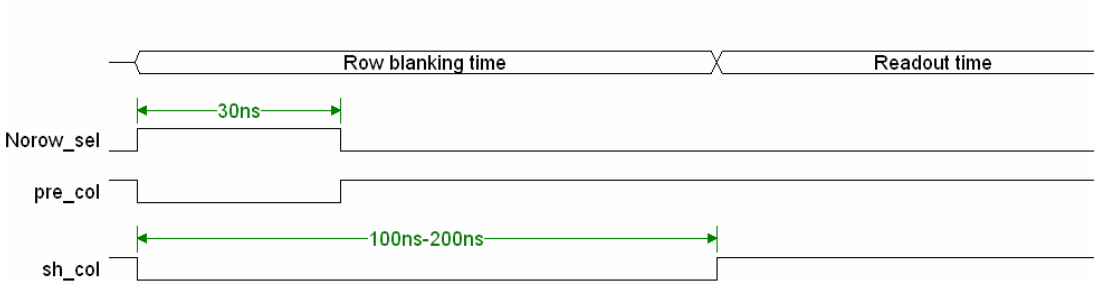
A straightforward way of reducing the ROT is by using a sample and hold function.

By means of Sh_col the analog data is tracked during the first 100 ns during the selection of a new set of lines. After 100 ns, the analog data is stored. The ROT is in this case reduced to 100 ns, but as the internal data is not stable yet, dynamic range is lost because not the complete analog levels are reached yet after 100 ns.

Figure 21 shows this principle. Sh_col is now a pulse of 100 ns-200 ns starting at the same moment as pre_col and Norowsel. The duration of Sh_col is equal to the ROT. The shorter this time the shorter the ROT; however, this also lowers the dynamic range.

In case "voltage averaging" is required, the sensor must work in this mode with Sh_col signal and a "voltage averaging" signal must be generated after Sh_col drops and before the readout starts (see Figure 17)

**Figure 21. Reduced Standard ROT with Sh_col Signal**
**pre_col (short pulse), Norowsel (short pulse) and Sh_col (large pulse)**




*Precharging the Buses*

This timing mode is exactly the same as the mode without sample and hold, except that the prebus1 and prebus2 signals are activated. Note that precharging of the buses can be combined with all of the timing modes discussed earlier. The idea is to have a short pulse of about 5 ns to precharge the output buses to a well known level. This mode makes the ghosting of bad columns impossible.

In this mode, Nsf_load must be made much larger (at least 1 MΩ).

**Figure 22. X and Y Addressing with Precharging of the Buses**

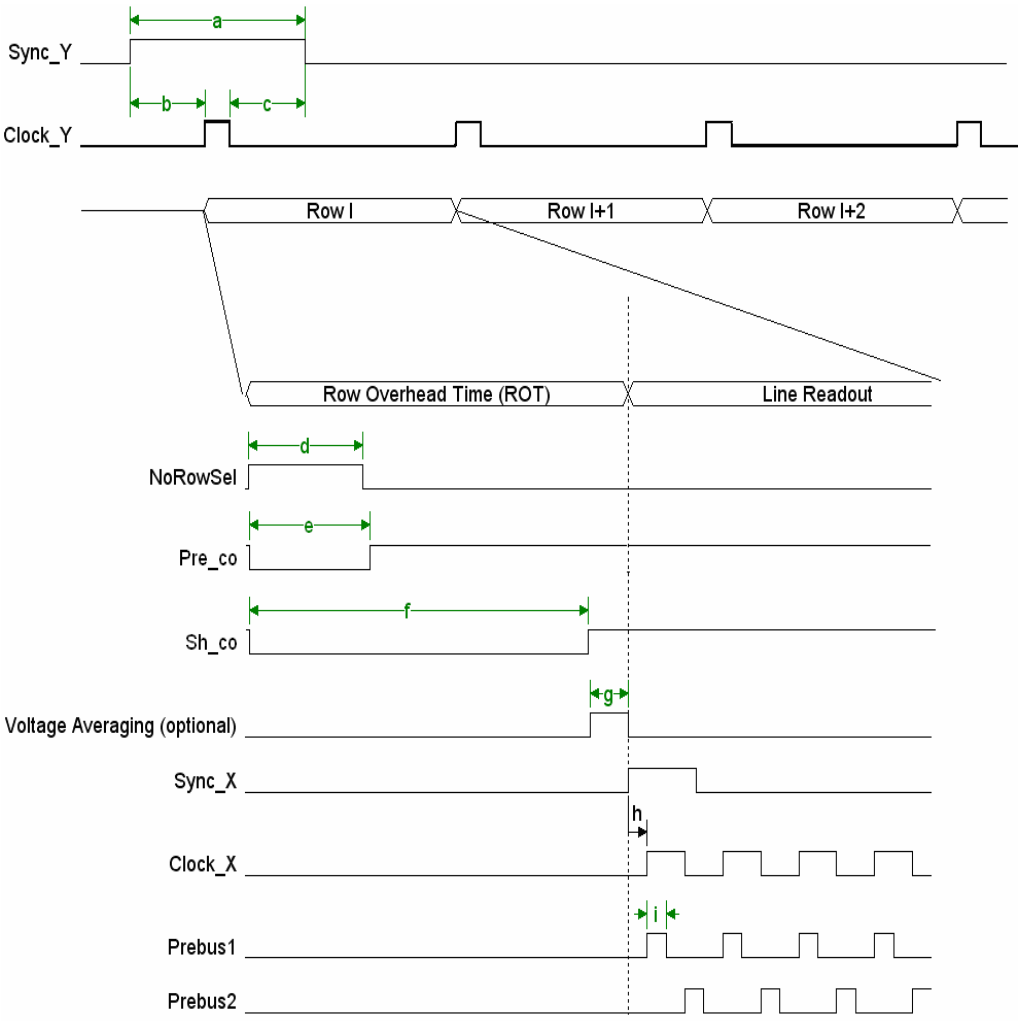



**Table 14. Readout Timing Specifications with Precharching of the Buses**

| Symbol | Name | Value |
|---|---|---|
| a | Sync_Y | >20 ns |
| b | Sync_Y-Clock_Y | >0 ns |
| c | Clock_Y-Sync_Y | >0 ns |
| d | NoRowSel | >50 ns |
| e | Pre_col | >50 ns |
| f | Sh_col | 200 ns (or cst low, depending on timing mode) |
| g | Voltage averaging | >20 ns |
| h | Sync_X-Clock_X | >0 ns |
| i | Prebus pulse | As short as possible |

### Serial-Parallel-Interface (SPI)

The SPI is required to upload the different modes. Table 15 shows the parameters and their bit position

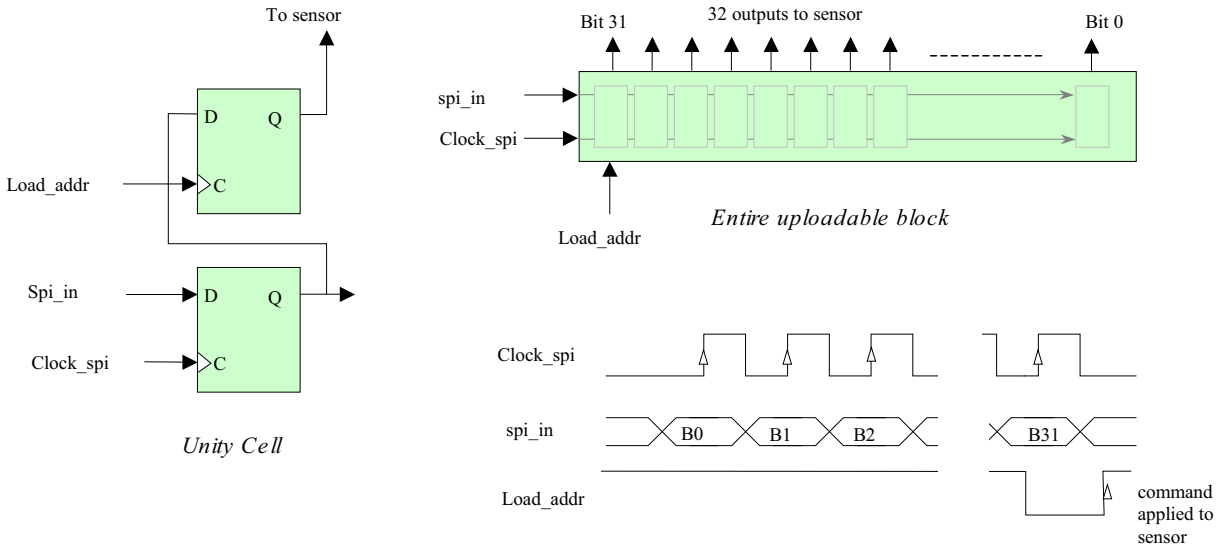
**Table 15. SPI parameters**

| Parameter | Bit # | Remarks |
|---|---|---|
| Y-direction | 0 | 1: From bottom to top |
| Y-address | 1-10 | Bit 1 is LSB |
| X-voltage averaging enable | 11 | 1: Enabled |
| X-subsampling | 12 | 1: Subsampling |
| X-direction | 13 | 0: From left to right |
| X-address | 14-23 | Bit 14 is LSB |
| Nr output amplifiers | 24 | 0: 1 Output |
| DAC | 25-31 | Bit 25 is LSB |

When all zeros are loaded into the SPI, the sensor starts at pixel 0,0. The scanning is from left to right and from top to bottom. There is no sub sampling or voltage averaging and only one output is used. The DAC has the lowest level at its output.

When using sub sampling, only even X-addresses may be applied.

**Figure 23. SPI Block Diagram and Timing**



## Pin List

Table 16 is a list of all the pins and their functionalities.

**Table 16. Pin List**[6, 7, 8]

| Pad | Pin | Pin Name | Pin Type | Description |
|---|---|---|---|---|
| 1 | E1 | sync_x | Input | Digital input. Synchronises the X-address register. |
| 2 | F1 | eos_x | Testpin | Indicates when the end of the line is reached. |
| 3 | D2 | vdd | Supply | Power supply digital modules. |
| 4 | G2 | clock_x | Input | Digital input. Determines the pixel rate. |
| 5 | G1 | eos_spi | Testpin | Checks if the data is transferred correctly through the SPI. |
| 6 | F2 | spi_data | Input | Digital input. Data for the SPI. |
| 7 | H1 | spi_load | Input | Digital input. Loads data into the SPI. |
| 8 | H2 | spi_clock | Input | Digital input. Clock for the SPI. |
| 9 | J2 | gndo | Ground | Ground output stages |
| 10 | J1 | out2 | Output | Analog output 2. |
| 11 | K1 | out2DC | Output | Reference output 2. |
| 12 | M2 | voo | Supply | Power supply output stages |
| 13 | L1 | out1DC | Output | Reference output 1. |
| 14 | M1 | out1 | Output | Analog output 1. |
| 15 | N2 | gndo | Ground | Ground output stages. |
| 16 | P1 | vaa | Supply | Power supply analog modules. |
| 17 | P2 | gnda | Ground | Ground analog modules. |
| 18 | N1 | va3 | Supply | Power supply column modules. |
| 19 | P3 | vpix | Supply | Power supply pixel array. |
| 20 | Q1 | psf_load | Input | Analog reference input. Biasing for column modules. Connect with R=1 MΩ to Vaa and decouple with C=100 nF to gnda. |
| 21 | Q2 | nsf_load | Input | Analog reference input. Biasing for column modules. Connect with R=5 kΩ to Vaa and decouple with C=100 nF to gnda. |
| 22 | R1 | muxbus_load | Input | Analog reference input. Biasing for multiplex bus. Connect with R=25 kΩ to Vaa and decouple with C=100 nF to gnda. |
| 23 | R2 | uni_load_fast | Input | Analog reference input. Biasing for column modules. Connect with R=10 kΩ to Vaa and decouple with C=100 nF to gnda. |
| 24 | Q3 | pre_load | Input | Analog reference input. Biasing for column modules. Connect with R=3 kΩ to Vaa and decouple with C=100 nF to gnda. |
| 25 | Q4 | out_load | Input | Analog reference input. Biasing for output stage. Connect with R=60 kΩ to Vaa and decouple with C=100 nF to gnda. |
| 26 | N3 | dec_x_load | Input | Analog reference input. Biasing for X-addressing. Connect with R=2 MΩ to Vdd and decouple with C=100 nF to gndd. |
| 27 | Q5 | uni_load | Input | Analog reference input. Biasing for column modules. Connect with R=1 MΩ to Vaa and decouple with C=100 nF to gnda. |
| 28 | Q6 | col_load | Input | Analog reference input. Biasing for column modules. Connect with R=1 MΩ to Vaa and decouple with C=100 nF to gnda. |
| 29 | Q7 | dec_y_load | Input | Analog reference input. Biasing for Y-addressing. Connect with R=2 MΩ to Vdd and decouple with C=100 nF to gndd. |
| 30 | R3 | vdd | Supply | Power supply digital modules. |
| 31 | M3 | gndd | Ground | Ground digital modules. |
| 32 | L2 | prebus1 | Input | Digital input. Control signal to reduce readout time. |

**Table 16. Pin List**[6, 7, 8] (continued)

| Pad | Pin | Pin Name | Pin Type | Description |
|---|---|---|---|---|
| 33 | L3 | prebus2 | Input | Digital input. Control signal to reduce readout time. |
| 34 | Q8 | sh_col | Input | Digital input. Control signal of the column readout. |
| 35 | R4 | pre_col | Input | Digital input. Control signal of the column readout to reduce row-blanking time. |
| 36 | R5 | norowsel | Input | Digital input. Control signal of the column readout. |
| 37 | R6 | clock_y | Input | Digital input. Clock of the Y-addressing. |
| 38 | R7 | sync_y | Input | Digital input. Synchronises the Y-address register. |
| 39 | K2 | eos_y_r | Testpin | Indicates when the end of frame is reached when scanning in the 'right' direction. |
| 40 | Q9 | temp_diode_p | Testpin | Anode of temperature diode. |
| 41 | Q10 | temp_diode_n | Testpin | Cathode of temperature diode. |
| 42 | R8 | vpix | Supply | Power supply pixel array. |
| 43 | R9 | vmem_l | Supply | Power supply Vmem drivers. |
| 44 | R10 | vmem_h | Supply | Power supply Vmem drivers. |
| 45 | R11 | vres | Supply | Power supply reset drivers. |
| 46 | Q11 | vres_ds | Supply | Power supply reset drivers. |
| 47 | R12 | adc1_ref_low | Input | Analog reference input. Low reference voltage of ADC (see Figure 9 for exact resistor value). |
| 48 | Q12 | adc1_linear_conv | Input | Digital input. 0= linear conversion; 1= gamma correction. |
| 49 | P15 | adc1_bit_9 | Output | Digital output 1 <9> (MSB). |
| 50 | Q14 | adc1_bit_8 | Output | Digital output 1 <8>. |
| 51 | Q15 | adc1_bit_7 | Output | Digital output 1 <7>. |
| 52 | R13 | adc1_bit_6 | Output | Digital output 1 <6>. |
| 53 | R14 | adc1_bit_5 | Output | Digital output 1 <5>. |
| 54 | R15 | adc1_bit_4 | Output | Digital output 1 <4>. |
| 55 | P14 | adc1_bit_3 | Output | Digital output 1 <3>. |
| 56 | Q13 | adc1_bit_2 | Output | Digital output 1 <2>. |
| 57 | R16 | adc1_bit_1 | Output | Digital output 1 <1>. |
| 58 | Q16 | adc1_bit_0 | Output | Digital output 1 <0> (LSB). |
| 59 | P16 | adc1_clock | Input | ADC clock input. |
| 60 | N14 | adc1_gndd | Supply | Digital GND of ADC circuitry. |
| 61 | N15 | adc1_vddd | Supply | Digital supply of ADC circuitry (nominal 2.5V). |
| 62 | L16 | adc1_gnda | Supply | Analog GND of ADC circuitry. |
| 63 | L15 | adc1_vdda | Supply | Analog supply of ADC circuitry (nominal 2.5V). |
| 64 | N16 | adc1_bit_inv | Input | Digital input. 0=no inversion of output bits; 1 = inversion of output bits. |
| 65 | M16 | adc1_CMD_SS | Input | Analog reference input. Biasing of second stage of ADC. Connect to $V_{DDA}$ with R=50 kΩ and decouple with C=100 nF to GNDa. |
| 66 | L14 | adc1_nalog_in | Input | Analog input of first ADC. |
| 67 | M15 | adc1_CMD_FS | Input | Analog reference input. Biasing of first stage of ADC. Connect to $V_{DDA}$ with R=50 kΩand decouple with C=100 nF to GNDa. |
| 68 | M14 | adc1_ref_high | Input | Analog reference input. High reference voltage of ADC. (see Figure 9 for exact resistor value) |
| 69 | K14 | vres_ds | Supply | Power supply reset drivers. |
| 70 | J14 | vres | Supply | Power supply reset drivers. |

**Table 16. Pin List**[6, 7, 8] (continued)

| Pad | Pin | Pin Name | Pin Type | Description |
|---|---|---|---|---|
| 71 | J15 | vpre_l | Supply | Power supply precharge drivers. Must be able to sink current. Can also be connected to ground. |
| 72 | J16 | vdd | Supply | Power supply digital modules. |
| 73 | K15 | vmem_h | Supply | Power supply Vmem drivers. |
| 74 | K16 | vmem_l | Supply | Power supply Vmem drivers. |
| 75 | H15 | adc2_ref_low | Input | Analog reference input. Low reference voltage of ADC. (see Figure 9 for exact resistor value) |
| 76 | H16 | adc2_linear_conv | Input | Digital input. 0= linear conversion; 1= gamma correction. |
| 77 | G16 | adc2_bit_9 | Output | Digital output 2 <9> (MSB). |
| 78 | F16 | adc2_bit_8 | Output | Digital output 2 <8>. |
| 79 | E16 | adc2_bit_7 | Output | Digital output 2 <7>. |
| 80 | G15 | adc2_bit_6 | Output | Digital output 2 <6>. |
| 81 | G14 | adc2_bit_5 | Output | Digital output 2 <5>. |
| 82 | F14 | adc2_bit_4 | Output | Digital output 2 <4>. |
| 83 | E14 | adc2_bit_3 | Output | Digital output 2 <3>. |
| 84 | D16 | adc2_bit_2 | Output | Digital output 2 <2>. |
| 85 | E15 | adc2_bit_1 | Output | Digital output 2 <1>. |
| 86 | F15 | adc2_bit_0 | Output | Digital output 2 <0> (LSB). |
| 87 | D15 | adc2_clock | Input | ADC clock input. |
| 88 | C15 | adc2_gndd | Supply | Digital GND of ADC circuitry. |
| 89 | D14 | adc2_vddd | Supply | Digital supply of ADC circuitry (nominal 2.5V). |
| 90 | B16 | adc2_gnda | Supply | Analog GND of ADC circuitry. |
| 91 | B14 | adc2_vdda | Supply | Analog supply of ADC circuitry (nominal 2.5V). |
| 92 | C16 | adc2_bit_inv | Input | Digital input. 0=no inversion of output bits; 1 = inversion of output bits. |
| 93 | A16 | adc2_CMD_SS | Input | Biasing of second stage of ADC. Connect to $V_{DDA}$ with R=50 kΩ and decouple with C=100 nF to GNDa. |
| 94 | B15 | adc2_analog_in | Input | Analog input 2nd ADC. |
| 95 | A15 | adc2_adc2_CMD_FS | Input | Analog reference input. Biasing of first stage of ADC. Connect to $V_{DDA}$ with R=50 kΩ and decouple with C=100 nF to GNDa. |
| 96 | A14 | adc2_ref_high | Input | Analog reference input. High reference voltage of ADC. (see Figure 9 for exact resistor value) |
| 97 | C14 | vres_ds | Supply | Power supply reset drivers. |
| 98 | B13 | vres | Supply | Power supply reset drivers. |
| 99 | A13 | vmem_h | Supply | Power supply Vmem drivers. |
| 100 | A9 | vmem_l | Supply | Power supply Vmem drivers. |
| 101 | A10 | vpix | Supply | Power supply pixel array. |
| 102 | A11 | reset | Input | Digital input. Control of reset signal in the pixel. |
| 103 | A12 | reset_ds | Input | Digital input. Control of double slope reset in the pixel. |
| 104 | B7 | mem_hl | Input | Digital input. Control of Vmem signal in pixel. |
| 105 | B8 | precharge | Input | Digital input. Control of Vprecharge signal in pixel. |
| 106 | B9 | sample | Input | Digital input. Control of Vsample signal in pixel. |
| 107 | B10 | temp_diode_n | Testpin | Cathode of temperature diode. |
| 108 | B11 | temp_diode_p | Testpin | Anode of temperature diode. |

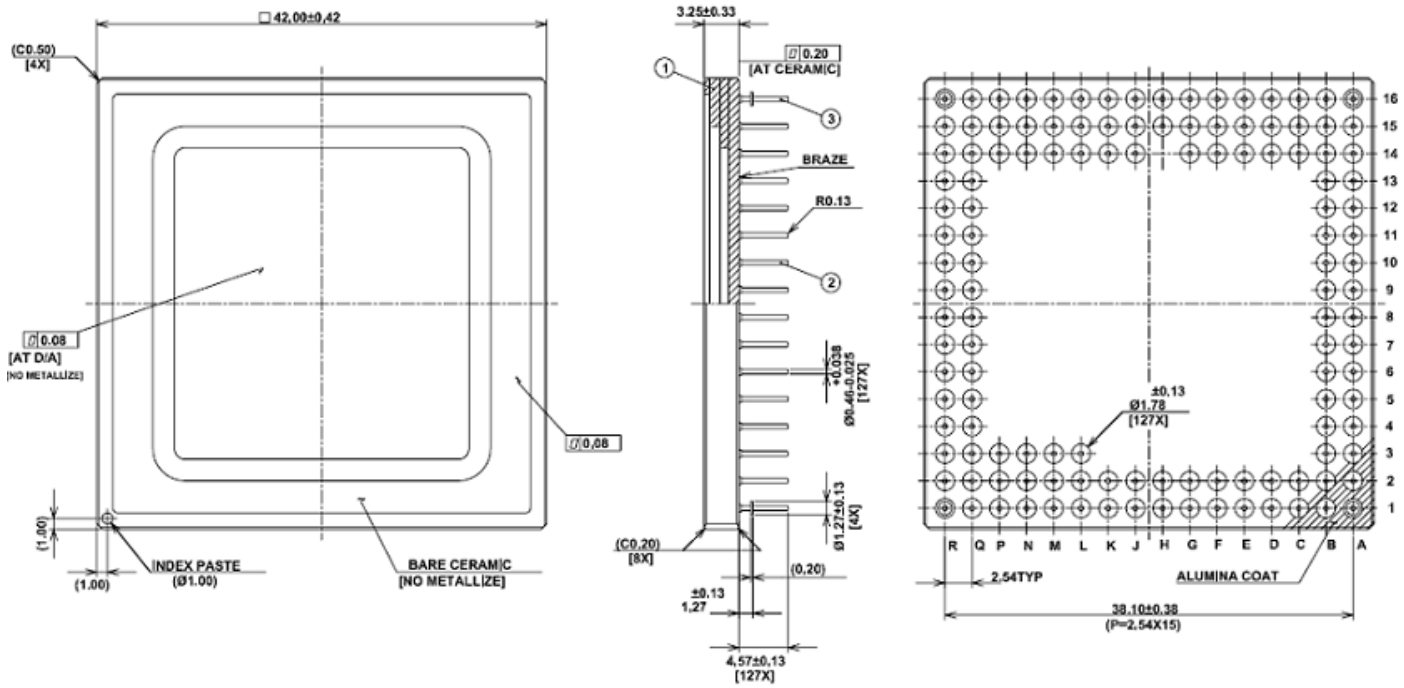
**Table 16. Pin List**[6, 7, 8] (continued)

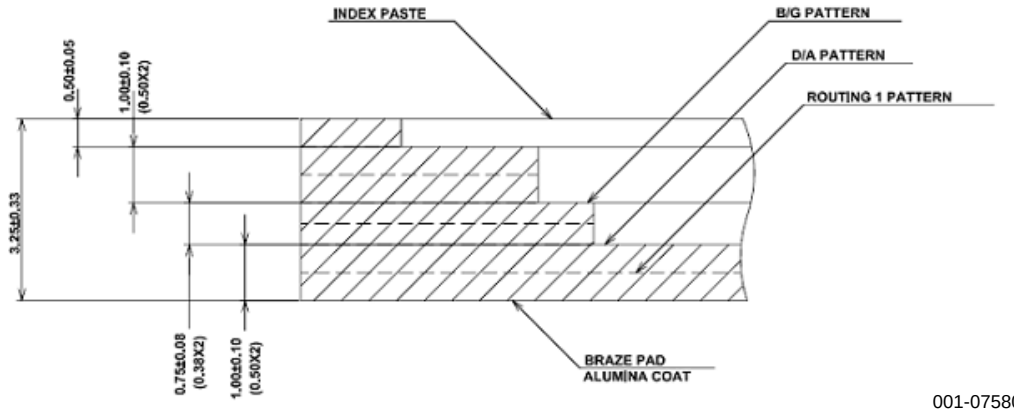
| Pad | Pin | Pin Name | Pin Type | Description |
|---|---|---|---|---|
| 109 | B6 | precharge_bias | Input | Analog reference input. Biasing for pixel array. (see Table 10 for exact resistor and capacitor value). |
| 110 | A8 | photodiode | Testpin | Output photodiode. |
| 111 | A7 | gndd | Ground | Ground digital modules. |
| 112 | B12 | vdd | Supply | Power supply digital modules. |
| 113 | A6 | eos_y_l | Testpin | Indicates when the end of frame is reached when scanning in the 'left' direction. |
| 114 | A1 | sync_y | Input | Digital input. Synchronises the Y-address register. |
| 115 | A5 | clock_y | Input | Digital input. Clock of the Y-addressing. |
| 116 | A2 | norowsel | Input | Digital input. Control signal of the column readout. |
| 117 | A3 | volt. averaging | Input | Digital input. Control signal of the voltage averaging in the column readout. |
| 118 | B5 | pre_col | Input | Digital input. Control signal of the column readout to reduce row-blanking time. |
| 119 | A4 | sh_col | Input | Digital input. Control signal of the column readout. |
| 120 | B1 | prebus2 | Input | Digital input. Control signal to reduce readout time. |
| 121 | B2 | prebus1 | Input | Digital input. Control signal to reduce readout time. |
| 122 | C1 | dec_y_load | Input | Analog reference input. Biasing for Y-addressing. |
| 123 | D1 | vpix | Supply | Power supply pixel array. |
| 124 | B4 | va3 | Supply | Power supply column modules. |
| 125 | B3 | gnda | Ground | Ground analog modules. |
| 126 | C2 | vaa | Supply | Power supply analog modules. |
| 127 | E2 | gndd | Ground | Ground digital modules. |

**Notes**
6. All pins with the same name can be connected together.
7. All digital input are active high (unless mentioned otherwise).
8. All unused inputs should be tied to a non active level (For example, $V_{DD}$ or GND).

## Package Drawing

**Figure 24. LUPA 4000: 127 Pin PGA Package Drawing**




001-07580 *A

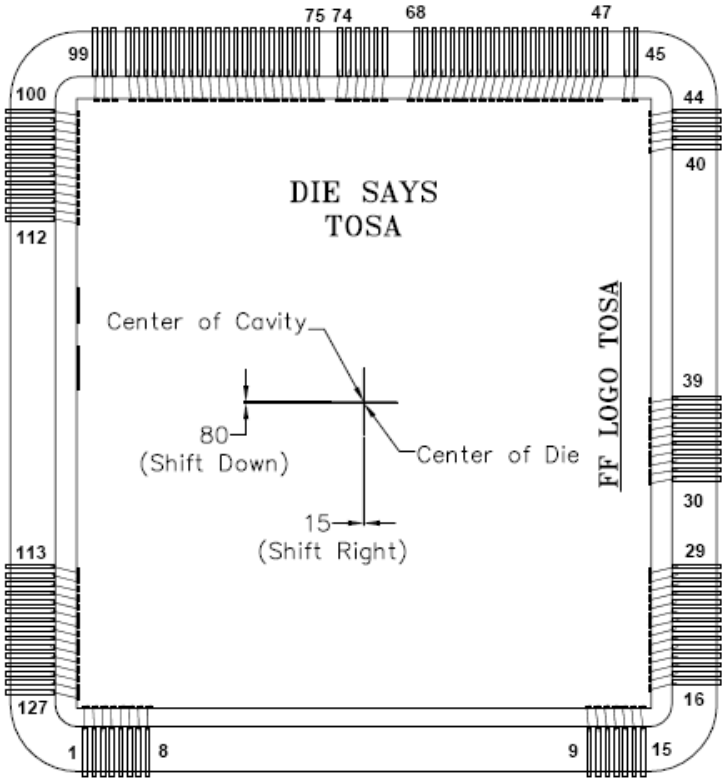
## Bonding Diagram

The die is bonded to the bonding pads of the package as shown in Figure 25.

**Additional Package Information**

- Die size: 25610 um X 27200 um
- Cavity pad: 27000 um X 29007 um
- Pixel 0,0 is located at 478 um from the left hand side of the die and 1366 um from the bottom side of the die.

**Figure 25. Bonding Pads Diagram of the LUPA 4000 Package**




TOLERANCES:

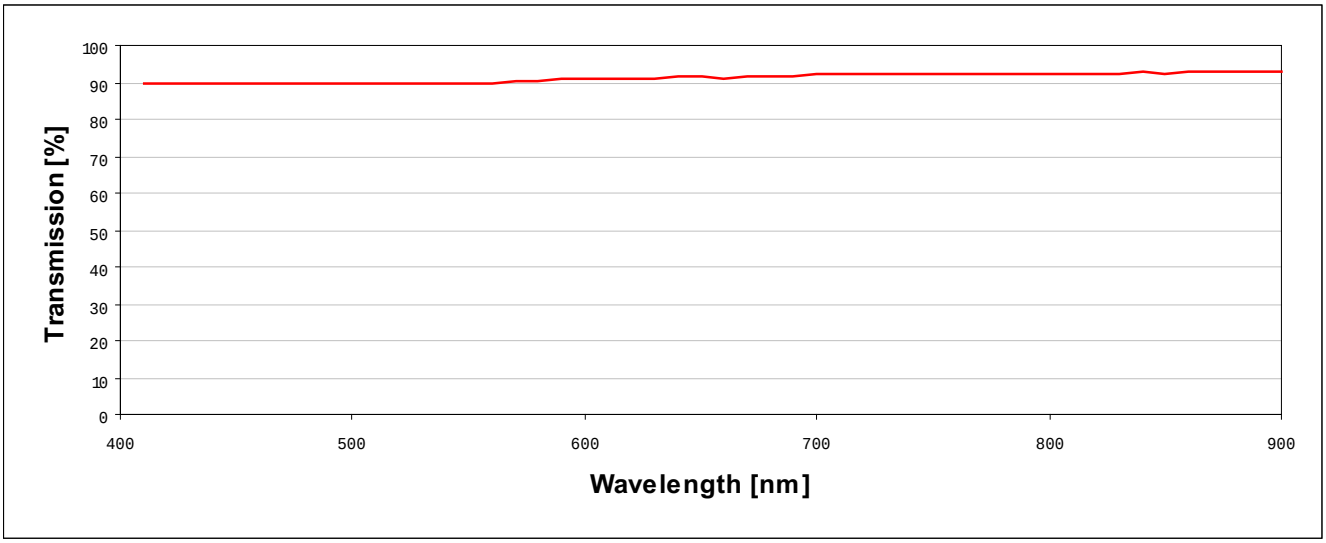
1. Placement accurary: ± 50um
2. Tilt = ± 1 degree
3. Rotation = ± 1 degree
4. Center of die is exactly at 50% between the 2 outsides of two outer seal rings.
5. Center of cavity is exactly at 50% between the inside edges of the finger pads.
6. All dimensions are in um unless otherwise noted.

001-48359 **

## Glass Transmittance

A D263 glass is used as protection glass lid on top of the LUPA 4000 monochrome sensors. Figure 26 shows the transmission characteristics of the D263 glass.

**Figure 26. Transmission Characteristics of the D263 Glass used for LUPA 4000 Sensors**




## Handling Precautions and Recommended Storage Conditions

For proper handling and storage conditions, refer to the Cypress application note, AN52561 on www.cypress.com.

## Limited Warranty

Cypress Image Sensor Business Unit warrants that the image sensor products mentioned here, if properly used and serviced, conform to the seller's published specifications. They are free from defects in material and workmanship for one (1) year following the date of shipment. If a defect is identified within the one (1) year period, Cypress will either replace the product or give credit for the product.

## Appendix A: LUPA 4000 Evaluation System

An LUPA 4000 evaluation kit is available for evaluation purposes. This kit consists of a multifunctional digital board (memory, sequencer, and Ethernet) and an analog image sensor board.

Bench Tools software (under Win 2000 or XP) allows the grabbing and display of images and movies from the sensor. All acquired images and movies can be stored in different file formats (8 or 16 bit). All setting can be adjusted on the fly to evaluate the sensors specifications. Default register values can be loaded to start the software in a desired state.

**Figure 27. Contents of LUPA 4000 Evaluation Kit**

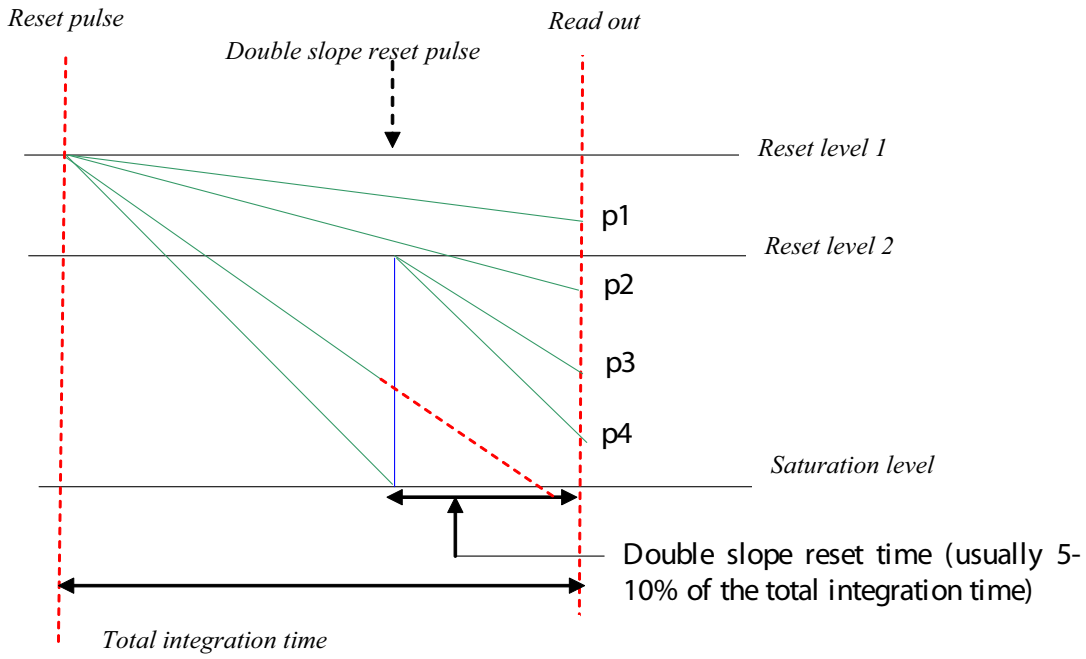

For more information on Image Sensors, contact imagesensors@cypress.com.

## Appendix B: Frequently Asked Questions

Q: How does the dual (multiple) slope extended dynamic range mode works?

A: The green lines in Figure 28 are the analog signal on the photodiode, which decrease as a result of exposure. The slope is determined by the amount of light at each pixel (the more light the steeper the slope). When the pixels reach the saturation level the analog signal does not change despite further exposure. Without any double slope, pulse pixels p3 and p4 reaches saturation before the sample moment of the analog values, no signal is acquired without double slope. When double slope is enabled a second reset pulse is given (blue line) at a certain time before the end of the integration time. This double slope reset pulse resets the analog signal of the pixels BELOW this level to the reset level. After the reset the analog signal starts to decrease with the same slope as before the double slope reset pulse. If the double slope reset pulse is placed at the end of the integration time (90% for instance) the analog signal that reaches the saturation levels are not saturated anymore (this increases the optical dynamic range) at read out. Note that pixel signals above the double slope reset level are not influenced by this double slope reset pulse (p1 and p2).

**Figure 28. Dual Slope Diagram**



## Document History Page

| Document Title: CYIL1SM4000AA LUPA 4000: 4 MegaPixel CMOS Image Sensor<br>Document Number: 38-05712 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 310396 | FPW | See ECN | Initial Cypress Release |
| *A | 497132 | QGS | See ECN | Converted to Frame file |
| *B | 649219 | FPW | See ECN | Ordering information update+ title update + package spec label |
| *C | 2738057 | NVEA/PYRS | 07/16/09 | Updated template, extensive content edits |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress offers standard and customized CMOS image sensors for consumer as well as industrial and professional applications. Consumer applications include solutions for fast growing high speed machine vision, motion monitoring, medical imaging, intelligent traffic systems, security, and barcode applications. Cypress's customized CMOS image sensors are characterized by very high pixel counts, large area, very high frame rates, large dynamic range, and high sensitivity.

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