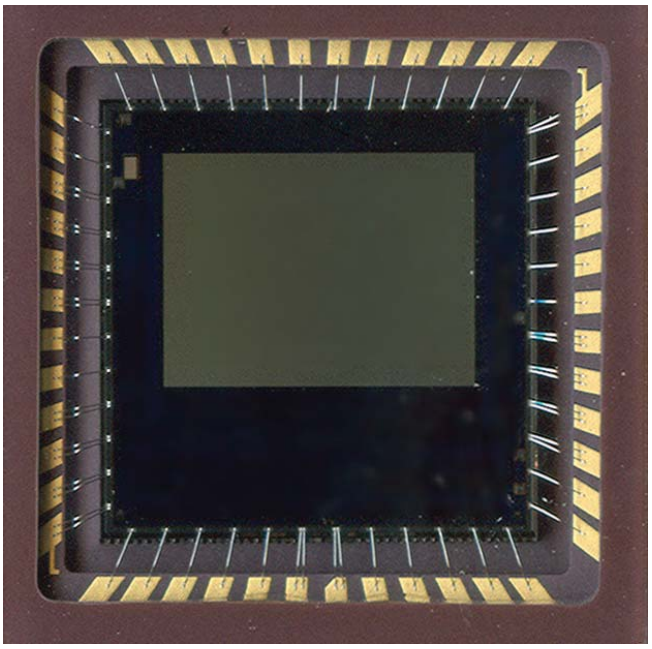
CYIL1SM0300AA

LUPA-300 CMOS Image Sensor



Features

- This VGA-resolution CMOS active pixel sensor features
  - Synchronous shutter.
  - A maximal frame-rate of 250 fps in full resolution.
- Readout speed can be boosted by means of sub sampling and windowed Region Of Interest (ROI) readout.
- High dynamic range scenes can be captured using the double and triple slope functionality.
- User programmable row and column start/stop positions allow windowing and sub sampling
- Reduces resolution while maintaining the constant field of view and an increased frame rate.
- The programmable gain and offset amplifier maps the signal swing to the ADC input range.
- A 10-bit ADC converts the analog data to a 10-bit digital word stream.
- Sensor uses a 3-wire Serial-Parallel (SPI) interface.
- Sensor operates with a 3.3V and 2.5V power supply and requires only one master clock for operation up to 80 MHz pixel rate.
- Available in a 48-pin ceramic LCC package.
- The sensor is available in a Monochrome version or Bayer (RGB) patterned color filter array.

Applications

- Machine vision
- Motion tracking

Parameter	Typical View
Optical Format	½ inch
Active Pixels	640 (H) x 480 (V)
Pixel Size	9.9 µm x 9.9 µm
Shutter Type	Electronic Snapshot Shutter
Maximum Data Rate/Master Clock	80 MPS/80 MHz
Frame Rate	250 fps (640 x 480)
ADC Resolution	10-bit, on-chip
Responsivity	3200 V.m2/W.s 17 V/lux.s
Dynamic Range	61 dB
Supply Voltage	Analog: 2.5V-3.3V Digital: 2.5V I/O: 2.5V
Power Consumption	190 mWatt
Operating Temperature	–40C to 70C
Color Filter Array	Mono RGB Bayer Pattern
Packaging	48-pins LCC

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Preamble

Overview

This document describes the interfacing and the driving of the LUPA-300 image sensor. This VGA-resolution CMOS active pixel sensor features synchronous shutter and a maximal frame-rate of 250 fps in full resolution. The readout speed can be boosted by means of sub sampling and windowed Region Of Interest (ROI) readout. High dynamic range scenes can be captured using the double and multiple slope functionality. User programmable row and column start/stop positions allow windowing and sub sampling reduces resolution while maintaining the constant field of view and an increased frame rate. The programmable gain and offset amplifier maps the signal swing to the ADC input range. A 10-bit ADC converts the analog data to a 10-bit digital word stream. The sensor uses a 3-wire Serial-Parallel (SPI) interface. It operates with a 3.3V and 2.5V power supply and requires only one master clock for operation up to 80 MHz pixel rate. It is housed in an 48-pin ceramic LCC package.

The sensor is available in a Monochrome version or Bayer (RGB) patterned color filter array.

This data sheet allows the user to develop a camera-system based on the described timing and interfacing.

Main Features

The main features of the image sensor are identified as:

- 640 x 480 active pixels (VGA resolution).
- 9.9 μm^2 square pixels (based on the high-fill factor active pixel sensor technology of FillFactory (US patent No. 6,225,670 and others)).
- Optical format: ½ optical inch
- Pixel rate of 80 MHz
- On-chip 10 bit ADC's
- Full snapshot shutter.
- Random programmable windowing.
- 48-pin LCC package
- Sub sampling (Y direction)
- Programmable read out direction (X and Y)

Part Number and ordering information

Name	Package	Mono-chrome/Color
CYIL1SM0300AA-QDC	48-pin ceramic LCC	Monochrome
CYIL1SE0300AA-QDC	48-pin ceramic LCC	Color

The LUPA-300 is also available in color or monochrome without the cover glass. Please contact Cypress for more information.

Specifications

General Specifications

Table 1. General Specification

Parameter	Specifications	Remarks
Pixel Architecture	6 transistor pixel	
Pixel Size	9.9 µm x 9.9 µm	The pixel size and resolution result in a 6.3 mm x 4.7 mm optical active area (1/2 inch).
Resolution	640 x 480	
Pixel Rate	80 MHz	
Shutter Type	Pipelined snapshot shutter	Integration during read out is possible
Frame Rate	250 fps	Frame rate can be boosted by sub sampling and windowing

Electro-Optical Specifications

Overview

Table 2. Electro-Optical Specifications

Parameter	Typical Specifications	Remarks
FPN	2.5% RMS	10% peak-to-peak, min: NA, max: 3.1%
PRNU	2.5% RMS	min:NA, max: 3.1%
Conversion gain	34 uV/e-	@ output, min: NA, max: NA
Saturation charge	35.000 e-	min: NA, max: NA
Sensitivity	3200 V.m2/W.s	min: NA, max: NA
	17V/lux.s	Visible band only (180 lux = 1 W/m2)
Peak QE * FF	45%	
Dark current (@ 21 °C)	300mV/s	min: NA, max: NA
Noise electrons	32e-	min: NA, max: NA
S/N ratio	60.7 dB	min: NA, max: NA
Parasitic sensitivity	1/5000	min: NA, max: NA
MTF	60%	min:NA, max: NA
Power dissipation	160 mW	Typical, not including output load
	190 mW	Typical, including output loads of 15 pF

Spectral Response Curve

Figure 1. Special Response of LUPA-300

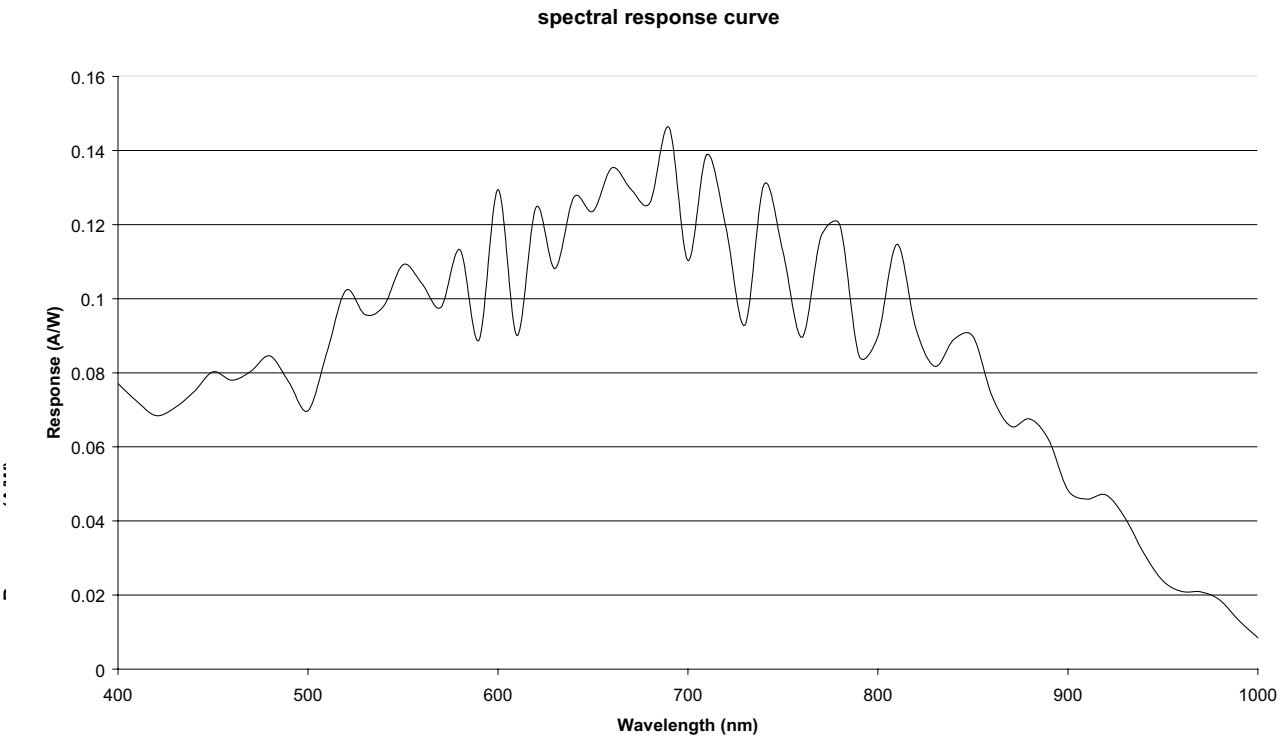
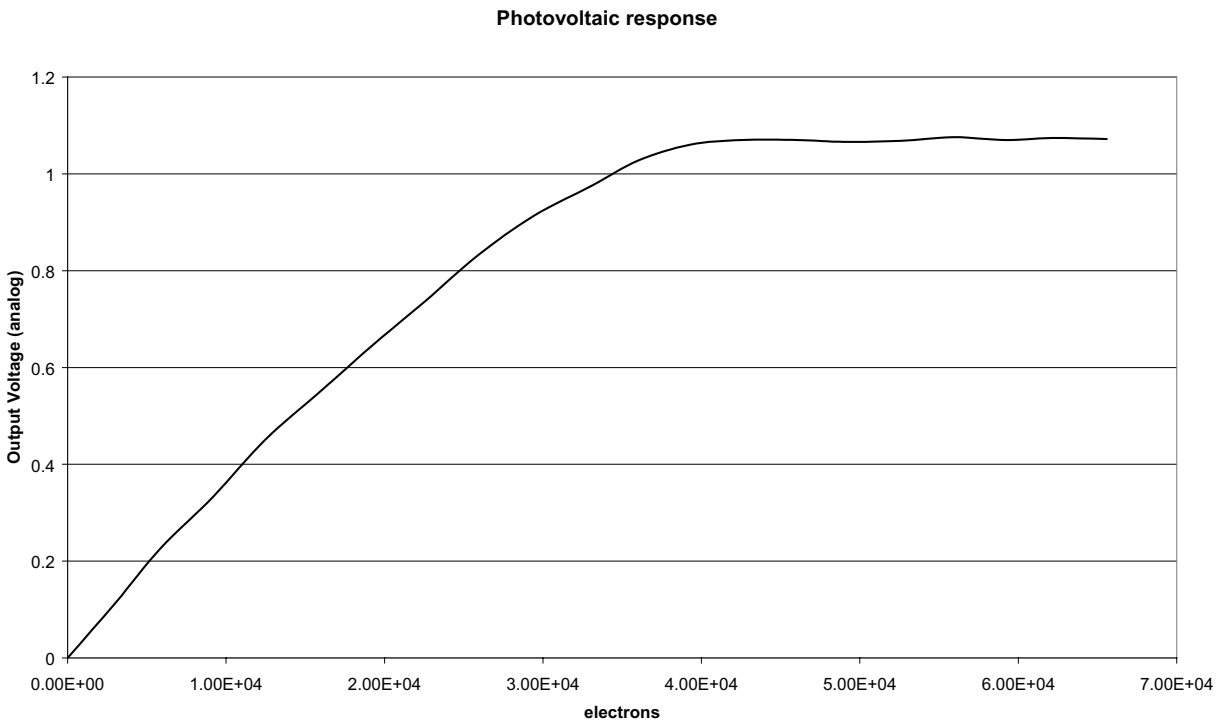


Photo-voltaic Response Curve

Figure 2. Photo-voltaic response LUPA-300



Features and General Specifications

Table 3. General Specifications

Feature	Specification/Description
Electronic shutter type	Full snapshot shutter (integration during read out is possible).
Windowing (ROI)	Randomly programmable ROI read out. Implemented as scanning of lines/columns from an uploaded position.
Sub-sampling	Sub sampling is possible (only in the Y-direction) Sub-sampling pattern: Y0Y0Y0Y0
Read out direction	Read out direction can be reversed in X and Y.
Extended dynamic range	Multiple slope (up to 90 dB optical dynamic range).
Programmable gain	range x1 to x16, in 16 steps using 4-bits programming.
Programmable offset	256 steps (8 bit)
Digital output	On-chip 10-bit ADCs @ 80 Msamples/s.
Supply voltage VDD	Nominal 2.5V (some supplies require 3.3V).
Logic levels	2.5V.
Operational temperature range	–40°C to 70°C; with degradation of dark current.
Interface	Serial-to Parallel Interface (SPI).
Package	48-pin LCC
Power dissipation	<190 mW
Mass	±1g

Electrical Specifications

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	DC supply voltages	–0.5 to 3.5	V
V_{IN}	DC input voltage	–0.5 to 3.5	V
V_{OUT}	DC output voltage	–0.5 to 3.5	V
I_{IO}	DC current on any single pin	+/– 50	mA
T_L	Lead temperature (5 seconds soldering)	350	ºC

Absolute Ratings are those values beyond which damage to the device may occur.

$V_{DD} = V_{DDD} = V_{DDA}$ (V_{DDD} is supply to digital circuit, V_{DDA} to analog circuit).

Recommended Operating Conditions:

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDA}	Power supply of the analog readout circuitry.		2.5		V
V_{DDD}	Digital power supply		2.5		V
V_{PIX}	Power supply of the analog pixel array		2.5		V
V_{RES}	Power supply reset drivers	2.5	3.3	3.5	V
V_{MEM_H}	Power supply of the pixels memory element (high level)	2.5	3.3	3.5	V
V_{ADC}	Power supply of the on-chip ADCs		2.5		V
T_A	Commercial operating temperature.	–40	30	70	°C
A_L	Maximum lens angle			25	°

Notes
1. All parameters are characterized for DC conditions after thermal equilibrium has been established.
2. Unused inputs must always be tied to an appropriate logic level, e.g. either VDD or GND.
3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high-impedance circuit.

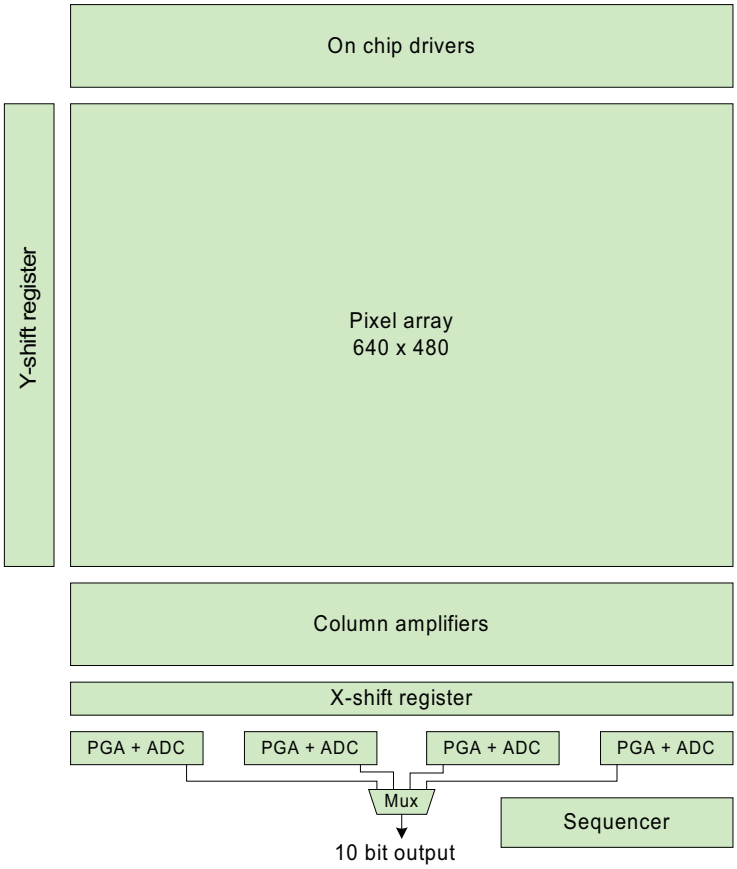
Sensor Architecture

The floor plan of the architecture is shown in the block diagram below. The image core consists of a pixel array, an X- and Y-addressing register, pixel array drivers and column amplifiers. The image sensor of 640 x 480 pixels is read out in progressive scan.

The architecture allows programmable addressing in the x-direction in steps of 8 pixels and in the y-direction in steps of 1 pixel. The starting point of the address is uploadable by means of the Serial Parallel Interface (SPI).

The PGAs amplify the signal from the column and add an offset so the signal fits in the input range of the ADC. The four ADCs then convert the signal to the digital domain. Pixels are selected in a 4 * 1 kernel. Every ADC samples the signal from one of the 4 selected pixels. Sampling frequency is 20 MHz. The digital outputs of the 4 ADCs are multiplexed to one output bus operating at 80 MHz.

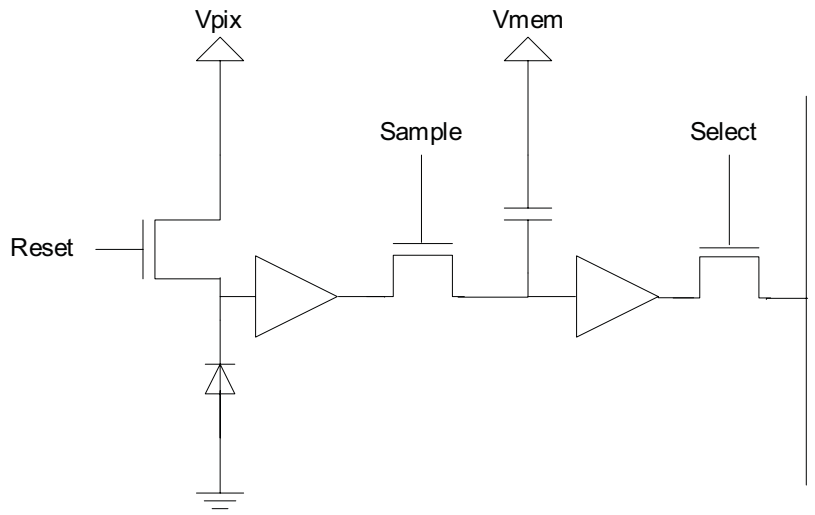
Figure 3. Floor Plan of the Sensor



The 6-T pixel

To obtain the global shutter feature combined with a high sensitivity and good Parasitic Light Sensitivity (PLS), the pixel architecture given in the figure below is implemented. This pixel architecture is designed in a 9.9 x 9.9 m2 pixel pitch. The pixel is designed to meet the specifications as described in *Table 1*, *Table 2* and *Table 3*.

Figure 4. 6T-Pixel Architecture.



Frame Rate and Windowing

Frame Rate

The frame rate depends on the input clock, the Frame Overhead Time (FOT) and the Row Overhead Time (ROT). The frame period can be calculated as follows

Frame period = FOT + Nr. Lines * (ROT + Nr. Pixels * clock period)

Table 6. Frame Rate Parameters

Parameter	Comment	Clarification
FOT	Frame Overhead Time	1200 clock periods for GRAN<1:0> = 11
		624 clock periods for GRAN<1:0> = 10
		336 clock periods for GRAN<1:0> = 01
		192 clock periods for GRAN<1:0> = 00
ROT	Row Overhead Time	48 clock periods for GRAN<1:0> = 11
		32 clock periods for GRAN<1:0> = 10
		24 clock periods for GRAN<1:0> = 01
		20 clock periods for GRAN<1:0> = 00
Nr. Lines	Number of Lines read out each frame	
Nr. Pixels	Number of pixels read out each line.	
clock period	1/80 MHz = 12.5 ns.	

Example: read out of the full resolution at nominal speed (80 MHz pixel rate = 12.5 ns, GRAN<1:0>=10):

Frame period = 7.8 μs + (480 * (400 ns + 12.5 ns * 640) = 4.039 ms => 247.6 fps.

In case the sensor operates in subsampling, the ROT is enlarged with 8 clock periods.

Windowing

Windowing can easily be achieved by the SPI interface. The starting point of the x- and y-address is uploadable, as well as the window size. The minimum step size in the x-direction is 8 pixels (only multiples of 8 can be chosen as start/stop addresses). The minimum step size in the y-direction is 1 line every line can be addressed) in normal mode and 2 lines in sub sampling mode.

The window size in the x-direction is uploadable in register NB_OF_PIX, the window size in the y-direction is determined

by the register FT_TIMER. Section 3.1 explains the use of this register.

Table 7. Typical frame rates for 80-MHz clock and GRAN<1:0>=10

Image resolution (X * Y)	Frame rate (fps)	Frame readout (us)	Comment
640 x 480	247.5	4038	
640 x 240	488.3	2048	sub sampling
256 x 256	1076	929	windowing

Analog to Digital Converter

The sensor has four 10-bit pipelined ADC on board. The ADCs are nominally operating at 20 Msamples/s. The input range of the ADC is between 0.75 and 1.75V. The analog input signal is sampled at 2.1 ns delay from the rising edge of the ADC clock.

The digital output data appears at the output at 5.5 cycles later. This is at the 6th falling edge succeeding the sample moment. The data is delayed by 3.7 ns with respect to this falling edge. This is illustrated in *Figure 5*.

Figure 5. ADC Timing

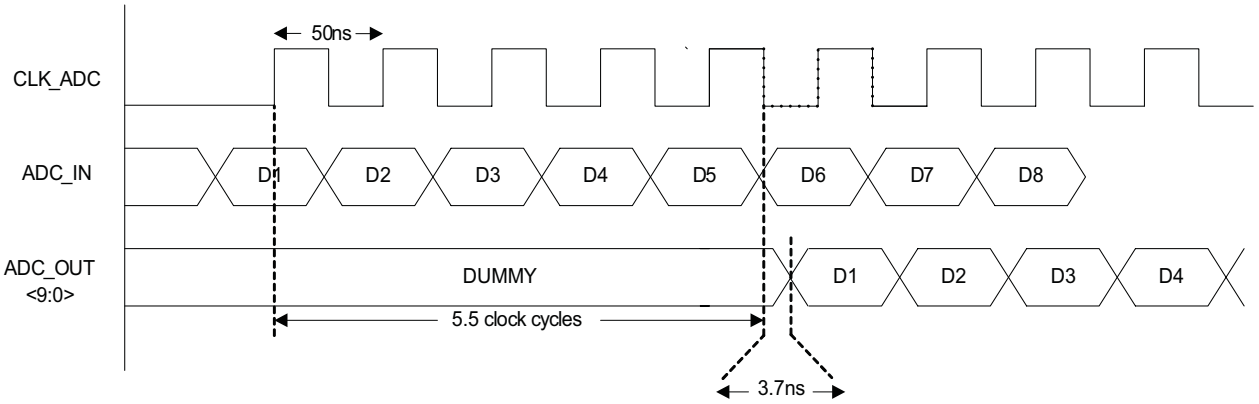


Table 8. ADC Parameters

Parameter	Specification
Data rate	20 Msamples/s
Input range	0.75V - 1.75 V
Quantization	10 bit
DNL	Typ. < 0.3 LSB
INL	Typ. < 0.7 LSB

Programmable Gain Amplifiers

The programmable gain amplifiers have two functions:

Adding an offset to the signal to fit it into the range of the ADC. This is controlled by the VBLACK and VOFFSET SPI settings.

Amplifying the signal after the offset has been added.

Offset Regulation

The purpose of the offset regulation is to bring the signal in the input range of the ADC.

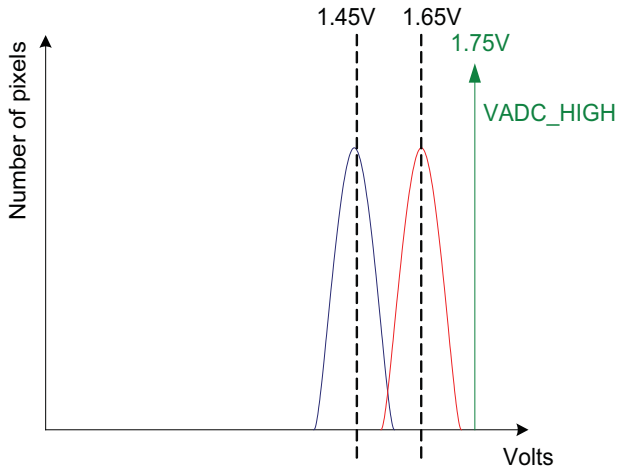
After the column amplifiers the signal from the pixels has a range from 0.1V (bright) to 1.3V (black). The input range of the ADC is from 0.75V to 1.75V. The amount of offset added is controlled by two SPI settings: VBLACK<7:0> and VOFFSET<7:0>. The formula for adding offset is:

Voutput = Vsignal + (Voffset - Vblack)

One should know that the FPN (fixed pattern noise) of the sensor causes a spread of about 100 mV on the dark level. To allow FPN correction during post processing of the image, this spread on the dark level needs to be covered by the input range of the ADC. This is the reason why the default settings of the SPI are programmed to add an offset of 200 mV. This way the dark level goes from 1.3V to 1.5V and is the FPN information still converted by the ADC. To even better match the ADC range we advice to program a offset of 340 mV. To program this offset the Voffset and Vblack registers can be used. See section 3.8 for more explanation. *Figure 6* illustrates the operation of the offset regulation with an example. The blue histogram is the histogram of the image taken after the column amplifiers. Let's say the device has a black level of

1.45V and a swing of 100 mV. With this swing it fits in the input range of the ADC, but a large part of the range of the ADC is not used in this case. For this reason an offset will be added first, to align the black level with the input range of the ADC. In the first step an offset of 200 mV is added with the default settings of VBLACK and VOFFSET. This results in the red histogram with a average black level of 1.65V. This means that the spread on the black level falls completely inside the range of the ADC. In a second step, explained in section 2.4.2, the signal will be amplified to use the full range of the ADC.

Figure 6. Offset Regulation



Programmable Gain

The amplification inside the PGA is controlled by three SPI settings:

The PGA gain selection: 16 gain steps are selectable by means of the GAIN_PGA<3:0> register. Selection word 0000 corresponds with gain 1.32 and selection word 1111 corresponds with gain 15.5. *Table 9* gives the 16 gain settings

The unity gain selection of the PGA is done by the UNITY_PGA setting. If this bit is high, the GAIN_PGA settings are ignored.

The SEL_UNI setting can be used to have more gain steps. If this bit is low, the signal is divided by two before entering the PGA. GAIN_PGA and UNITY_PGA settings are applied afterwards. If the SEL_UNI bit is high, there is a unity feed through to the PGA. This allows having a total gain range of 0.5 to 16 in 32 steps.

Table 9. Gain Settings

GAIN_PGA<3.0>	Gain
0000	1.32
0001	1.56
0010	1.85
0011	2.18
0100	2.58
0101	3.05
0110	3.59
0111	4.22
1000	4.9
1001	5.84
1010	6.84
1011	8.02
1100	9.38
1101	11.2
1110	13.12
1111	15.38

The amplification in the PGA is done around a pivoting point, set by Vcal. See *Figure 7* for an illustration of this. The VCAL<7:0> setting is used to apply the Vcal voltage through an on chip DAC

Figure 7. Effect on Histogram of PGA (gain=4); Vcal is the green line.

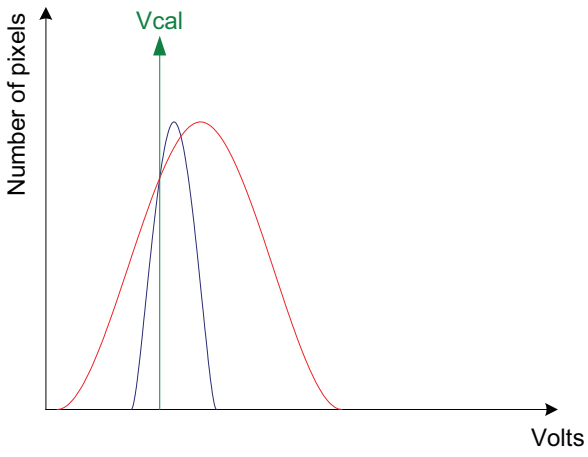
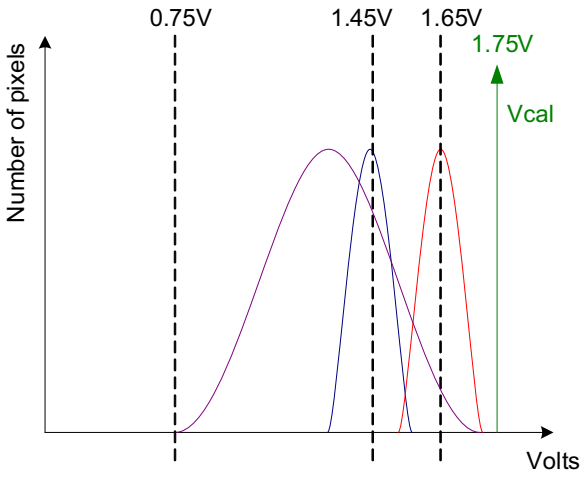


Figure 8 continues on the example of section 2.4.1. The blue histogram is the histogram of the image after the column amplifiers. With offset regulation an offset of 200 mV is added to bring the signal in range of the ADC. The black level of 1.45V is shifted to 1.65V.

The red and blue histograms have a swing of 100 mV. This means the input range of the ADC is not completely used. By

amplifying the signal with a factor 10 by the PGA, the full range of the ADC can be used. In this example Vcal is set at 1.75V (the maximum input range of the ADC) to make sure the spread on the black level is still inside the range of the ADC after amplification. The result after amplification is the purple histogram

Figure 8. Example of PGA operation.



Operation and Signaling

Power Supplies

Every module on chip--column amplifiers, output stages, digital modules, drivers--has its own power supply and ground. Off chip the grounds can be combined, but not all power supplies may be combined. This results in several different power supplies, but this is required to reduce electrical cross-talk and to improve shielding, dynamic range and output swing.

On chip we have the ground lines of every module, which are kept separate to improve shielding and electrical cross-talk between them.

An overview of the supplies is given in *Table 10* and *Table 11*. *Table 11* summarizes the supplies related to the pixel array signals, where *Table 10* summarizes the supplies related with all other modules.

Table 10. Power Supplies

Name	DC Current	Peak Current	Typ.	Max.	Description
V_{DDA}	15.7 mA	50 mA	2.5V		Power supply analog readout module.
V_{DDD}	6.7 mA	50 mA	2.5V	2.5V	Power supply digital modules
V_{ADC}	32.7 mA	100 mA	2.5V		Power supply of ADC circuitry
V_{DDO}	3.5 mA	100 mA	2.5V		Power supply output drivers
GND_D			0V		Ground of the digital module
GND_A			0V		Ground of the analog readout module
GND_{ADC}			0V		Ground of the ADC circuitry
GND_O			0V		Ground of the output drivers

Table 11. Overview of the Power Su[pplies Related to the pixel Signals

Name	DC Current	Peak Current	Min.	Typ.	Max.	Description
V_{PIX}	3 mA	100 mA		2.5V		Power supply pixel array
V_{RES}	1 µA	10 mA	3.0V	3.3V	3.5V	Power supply reset drivers.
V_{RES_DS}	1 µA	10 mA		2.8V		Power supply reset dual slope drivers
V_{RES_TS}	1 µA	10 mA		2.0V		Power supply reset triple slope drivers
V_{MEM_H}	1 µA	1 µA	3.0V	3.3V	3.5V	Power supply for memory element in pixel
$GND_{DRIVERS}$				0V		Ground of the pixel array drivers

The maximum currents mentioned in*Table 10* and *Table 11* are peak currents. All power supplies should be able to deliver these currents except for Vmem_l, which must be able to sink this current.

It is important to notice that no power supply filtering on chip is implemented and that noise on these power supplies can contribute immediately to the noise on the signal. The voltage supplies V_{PIX}, V_{DDA} and V_{ADC} are especially important to be noise free.

Biasing

Table 12 summarizes the biasing signals required to drive this image sensor. For optimization reasons of the biasing of the

column amplifiers with respect to power dissipation, we need several biasing resistors. This optimization results in an increase of signal swing and dynamic range.

Table 12. Overview of Bias Signals

Signal	Comment	Related Module	DC-Level‘
ADC_BIAS	Connect with 10 kOhm to V_{ADC} and decouple with 100n to GND_{ADC}.	ADC	693 mV
PRECHARGE_BIAS	Connect with 68 kOhm to V_{PIX} and decouple with 100 nF to $GND_{DRIVERS}$.	Pixel array precharge	567 mV
BIAS_PGA	Biasing of amplifier stage. Connect with 110 kOhm to V_{DDA} and decouple with 100 nF to GND_A.	PGA	650 mV
BIAS_FAST	Biasing of columns. Connect with 42 kOhm to V_{DDA} and decouple with 100 nF to GND_A.	Column amplifiers	750 mV
BIAS_SLOW	Biasing of columns. Connect with 1.5 MOhm to V_{DDA} and decouple with 100 nF to GND_A.	Column amplifiers	450 mV
BIAS_COL	Biasing of imager core. Connect with 500 kOhm to V_{DDA} and decouple with 100 nF to GND_A.	Column amplifiers	508 mV

Digital Signals

Depending on the operation mode (master or slave), the pixel array of the image sensor requires different digital control signals. The function of each of the signals is shown in *Table 13*:

Table 13. Overview of Digital Signals

Signal Name	I/O	Comments
LINE_VALID	Digital output	Indicates when valid data is at the outputs. Active high
FRAME_VALID	Digital output	Indicates when a valid frame is readout. Active high
INT_TIME_3	Digital IO	In master mode: Output to indicate the triple slope integration time. In slave mode: Input to control the triple slope integration time. Active high
INT_TIME_2	Digital IO	In master mode: Output to indicate the dual slope integration time. In slave mode: Input to control the dual slope integration time. Active high
INT_TIME_1	Digital IO	In master mode: Output to indicate the integration time. In slave mode: Input to control integration time. Active high
RESET_N	Digital input	Sequencer reset. Active low
CLK	Digital input	Readout clock (80 MHz), sine or square clock
SPI_ENABLE	Digital input	Enable of the SPI
SPI_CLK	Digital input	Clock of the SPI. (max. 20 MHz)
SPI_DATA	Digital IO	Data line of the SPI. Bidirectional pin

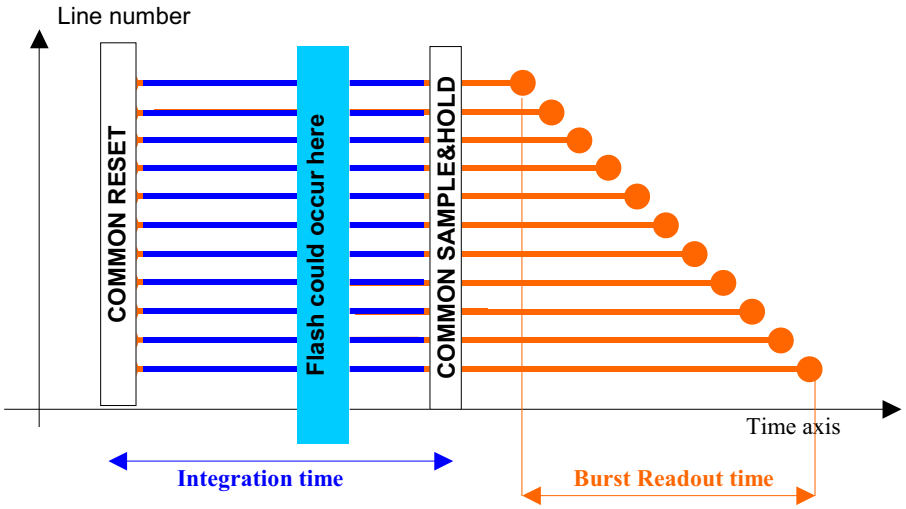
Synchronous Shutter

In a synchronous (snapshot or global) shutter light integration takes place on all pixels in parallel, although subsequent readout is sequential. *Figure 9* shows the integration and read out sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and read out cycle can occur in

Note
4. Each biasing signal determines the operation of a corresponding module in the sense that it controls speed and dissipation.

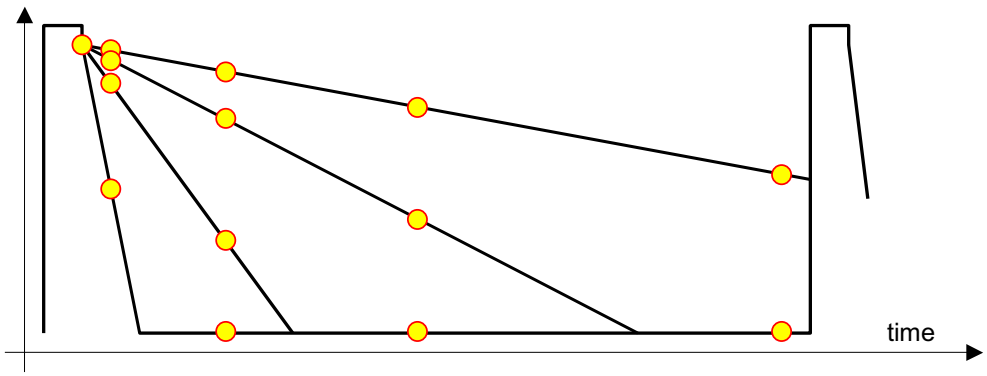
parallel or in sequential mode. (ref. 4. Timing and read out of the image sensor)

Figure 9. Synchronous Shutter Operation



Non-destructive Readout (NDR)

Figure 10. Principle of Non-Destructive Readout



The sensor can also be read out in a non-destructive way. After a pixel is initially reset, it can be read multiple times, without resetting. The initial reset level and all intermediate signals can be recorded. High light levels will saturate the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, one has to use the later or latest samples. Essentially an active pixel array is read multiple times, and reset only once. The external system intelligence takes care of the interpretation of the data. *Table 14* summarizes the advantages and disadvantages of non-destructive readout

Note

5. This mode can be activated by setting the NDR SPI register. The NDR SPI register should only be changed during FOT. The NDR bit should be set high during the first Frame Overhead Time after the pixel array has been reset; the NDR bit should be set low during the last Frame Overhead Time before the pixel array is being reset.

Table 14. Advantages and Disadvantages of Non-Destructive Readout

Advantages	Disadvantages
Low noise - as it is true CDS.	System memory required to record the reset level and the intermediate samples.
High sensitivity - as the conversion capacitance is kept rather low.	Requires multiples readings of each pixel, thus higher data throughput.
High dynamic range - as the results includes signal for short and long integrations times.	Requires system level digital calculations.

Sequencer

The sequencer generates the complete internal timing of the pixel array and the readout. The timing can be controlled by the user through the SPI register settings. The sequencer operates on the same clock as the ADCs. This is a division by 4 of the input clock.

Table 15 shows a list of the internal registers with a short description. In the next section, the registers are explained in more detail.

Table 15. Internal Registers

Address	Bits	Name	Description
0 (0000)	10:0	SEQUENCER	Default <10:0>: 00000101001
	1	mastermode	1: master mode; 0: slave mode
	1	ss	1: ss in y; 0: no subsampling
	2	gran	clock granularity
	1	enable_analog_out	1: enabled; 0: disabled
	1	calib_line	1: line calibration; 0 frame calibration
	1	res2_en	1: enable DS; 0: Disable DS
	1	res3_en	1: enable TS; 0: Disable TS
	1	reverse_x	1: readout in reverse x direction 0: readout in normal x direction
	1	reverse_y	1: readout in reverse y direction 0: readout in normal y direction
	1	Ndr	1: enable non destructive readout 0: disable non destructive readout
1 (0001)	7:0	START_X	Start pointer X readout Default <7:0>: 00000000
2 (0010)	8:0	START_Y	Start pointer Y readout Default <8:0>: 000000000
3 (0011)	7:0	NB_PIX	Number of kernels to read out (4 pixel kernel) Default <7:0>: 10100000
4 (0100)	11:0	RES1_LENGTH	Length of reset pulse (in number of lines) Default <11:0>: 000000000010
5 (0101)	11:0	RES2_TIMER	position of reset DS pulse in number of lines Default <11:0>: 000000000000
6 (0110)	11:0	RES3_TIMER	position of reset TS pulse in number of lines Default <11:0>: 000000000000
7(0111)	11:0	FT_TIMER	position of frame transfer in number of lines Default <11:0>: 000111100001

Table 15. Internal Registers (continued)

Address	Bits	Name	Description
8 (1000)	7:0	VCAL	DAC input for vcal Default <7:0>: 01001010
9 (1001)	7:0	VBLACK	DAC input for vblack Default <7:0>: 01101011
10 (1010)	7:0	VOFFSET	DAC input for voffset Default <7:0>: 01010101
11 (1011)	11:0	ANA_IN_ADC	Activate analog ADC input Default <11:0>: 000011110000
	4	sel_test_path	Selection of analog test path
	4	sel_path	Selection of normal analog path
	4	bypass_mux	Bypass of digital 4 to 1 mux
12 (1100)	11:0	PGA_SETTING	PGA settings Default <11:0>: 111110110000
	4	gain_pga	Gain settings PGA
	1	unity_pga	PGA unity amplification
	1	sel_uni	Preamplification of 0.5 (0: enabled)
	1	enable_analog_in	Activate analog input
	4	enable_adc	Put separate ADCs in standby
	1	sel_calib_fast	Select fast calibration of PGA
13 (1101)	11:0	CALIB_ADC <11:0>	Calibration word of the ADCs Default: calib_adc<11:0>:101011011111 calib_adc<23:12>:011011011011 calib_adc<32:24>:000011011011
14 (1110)	11:0	CALIB_ADC <23:12>	
15 (1111)	8:0	CALIB_ADC <32:24>	

Detailed Description of the Internal Registers

The registers should only be changed during FOT (when frame valid is low).

These registers should only be changed during RESET_N is low:

- Mastermode register
- Granularity register

Sequencer Register <10:0>

The sequencer register is an 11 bit wide register that controls all of the sequencer settings. It contains several "sub-registers".

Mastermode (1 bit)

This bit controls the selection of mastermode/slavemode. The sequencer can operate in 2 modes: master mode and slave mode. In master mode all the internal timing is controlled by the sequencer, based on the SPI settings. In slave mode the integration timing is directly controlled over three pins, the readout timing is still controlled by the sequencer.

1: Master mode (default)

0: Slave mode

Subsampling (1bit)

This bit enables/disables the subsampling mode. Subsampling is only possible in Y direction and follows this pattern:

- Read one, skip one: Y0Y0Y0Y0…

By default, the subsampling mode is disabled.

Clock granularity (2 bits)

The system clock (80 MHz) is divided several times on chip.

The clock, that drives the "snapshot" or synchronous shutter sequencer, can be programmed using the granularity register. The value of this register depends on the speed of your system clock.

11: > 80 MHz

10: 40-80 MHz (default)

01: 20-40 MHz

00: < 20 MHz

Enable analog out (1 bit)

This bit enables/disables the analog output amplifier.

1: enabled

0: disabled (default)

Calib_line (1bit)

This bit sets the calibration method of the PGA. Different calibration modes can be set, at the beginning of the frame and for every subsequent line that is read.

1: Calibration is done every line (default)

0: Calibration is done every frame (less row fixed pattern noise)

Res2_enable (1bit)

This bit enables/disables the dual slope mode of the device.

1: Dual slope is enabled (configured according to the RES2_TIMER register)

0: Dual slope is disabled (RES2_timer register is ignored) - default

Res3_enable (1bit)

This bit enables/disables the triple slope mode of the device.

1: triple slope is enabled (configured according to the RES3_TIMER register)

0: triple slope is disabled (RES3_timer register is ignored) - default

Reverse_X (1bit)

The readout direction in X can be reversed by setting this bit through the SPI.

1: Read direction is reversed (from right to left)

0: normal read direction (from left to right) - default

Reverse_Y (1bit)

The readout direction in Y can be reversed by setting this bit through the SPI.

1: Read direction is reversed (from bottom to top)

0: normal read direction (from top to bottom) - default

Ndr (1 bit)

This bit enables the non destructive readout mode if desired.

1: ndr enables

0: ndr disables (default)

Start_X Register <7:0>

This register sets the start position of the readout in X direction. In this direction there are 80 (from 0 to 79) possible start positions (8 pixels are addressed at the same time in one clock cycle). Keep in mind that if you put Start_X to 0 pixel 0 is being read out. Example:

If you set 23 in the Start_X register readout will only start from pixel 184 (8x23)

Start_Y Register <8:0>

This register sets the start position of the readout in Y direction. In this direction there are 480 (from 0 to 479) possible start positions. This means that the start position in Y direction can be set on a line by line basis.

Nb_pix <7:0>

This register sets the number of pixels to read out. The number of pixels to be read out is expressed as a number of kernels in this register (4 pixels per kernel). This means that there are 160 possible values for the register (from 1 to 160). Example:

If you set 37 in the nb_pix register, 148 (37 x 4) pixels will be read out.

Res1_length <11:0>

This register sets the length of the reset pulse (how long it remains high). This length is expressed as a number of lines (res1_length - 1). The minimum and default value of this register is 2.

The actual time the reset is high can be calculated with the following formula:

Reset high = (Res1_length-1) * (ROT + Nr. Pixels * clock period)

Res2_timer <11:0>

This register defines the position of the additional reset pulse to enable the dual slope capability. This is also defined as a number of lines-1.

The actual time on which the additional reset is given can be calculated with the following formula:

DS high = (Res2_timer-1) * (ROT + Nr. Pixels * clock period)

Res3_timer <11:0>

This register defines the position of the additional reset pulse to enable the triple slope capability. This is also defined as a number of lines - 1.

The actual time on which the additional reset is given can be calculated with the following formula:

TS high = (Res3_timer-1) * (ROT + Nr. Pixels * clock period)

Ft_timer <11:0>

This register sets the position of the frame transfer to the storage node in the pixel. This means that it also defines the end of the integration time. It is also expressed as a the number of lines - 1.

The actual time on which the frame transfer takes place can be calculated with the following formula:

FT time = (ft_timer-1) * (ROT + Nr. Pixels * clock period)

Vcal <7:0>

This register is the input for the on-chip DAC which generates the Vcal supply used by the PGA.

When the register is "00000000" it will set a Vcal of 2.5V. When the register is 11111111 then it will set a Vcal of 0V. This means that the minimum step you can take with the Vcal register is 9.8mV/bit (2.5V/256bits).

For more information, see section 3.4

Vblack <7:0>

This register is the input for the on-chip DAC which generates the Vblack supply used by the PGA. When the register is "00000000" it will set a Vblack of 2.5V. When the register is 11111111 then it will set a Vblack of 0V. This means that the minimum step you can take with the Vblack register is 9.8mV/bit (2.5V/256bits).

For more information, see section 3.4

Voffset <7:0>

This register is the input for the on-chip DAC, which generates the Voffset supply used by the PGA. When the register is "00000000" it will set a Voffset of 2.5V. When the register is 11111111 then it will set a Voffset of 0V. This means that the minimum step you can take with the Voffset register is 9.8 mV/bit (2.5V/256bits).

For more information, see section 3.4

Ana_in_ADC <11:0>

This register sets the different paths that can be used as the ADC input (mainly for testing and debugging). The register consists of several "sub-registers".

Sel_test_path (4 bits)

These bits select the analog test path of the ADC.

0000: No analog test path selected (default)

0001: Path of pixel 1 selected

0010: Path of pixel 2 selected

Sel_path (4 bits)

These bits select the analog path to the ADC.

1111: All paths selected (normal operation) - default

0000: No paths selected (enables ADC to be tested through test paths)

0001: Path of pixel 1 selected

0010: Path of pixel 2 selected

Bypass_mux (4 bits)

These bits enable the possibility to bypass the digital 4 to 1 multiplexer.

0000: no bypass (default)

PGA_SETTING <11:0>

This register defines all parameters to set the PGA. The register consists of different "sub-registers"

Gain_pga (4 bits)

These bits set the gain of the PGA. The following *Table 16* gives an overview of the different gain settings.

Table 16.

GAIN_PGA<3:0>	Gain
0000	1.32
0001	1.56
0010	1.85
0011	2.18
0100	2.58
0101	3.05
0110	3.59
0111	4.22
1000	4.9
1001	5.84
1010	6.84

Table 16. (continued)

GAIN_PGA<3:0>	Gain
1011	8.02
1100	9.38
1101	11.2
1110	13.12
1111	15.38

Unity_pga (1 bit)

This bit sets the PGA in unity amplification.

0: No unity amplification, gain settings apply

1: Unity gain amplification, gain setting are ignored (default)

Sel_uni (1 bit)

This bit selects whether or not the signal gets a 0.5 amplification before the PGA.

0: amplification of 0.5 before PGA

1: Unity feed through (default)

Enable_analog_in (1 bit)

This bit enables/disables an analog input to the PGA.

0: analog input disabled (default)

1: analog input enabled

Enable_adc (4 bits)

These bits can separately enable/disable the different ADCs.

0000: No ADCs enabled

1111: All ADCs enabled (default)

0001: ADC 1 enabled

0010: ADC 2 enabled

Sel_calib_fast (1 bit)

Selects the fast/slow calibration of the ADC

0: slow calibration

1: fast calibration

2ADC Calibration Word <32:0>

The calibration word for the ADCs is distributed over 3 registers (13, 14 and 15). These registers all have their default value and changing this value is not recommended. The default register values are:

calib_adc<11:0>: 101011011111

calib_adc<23:12>: 011011011011

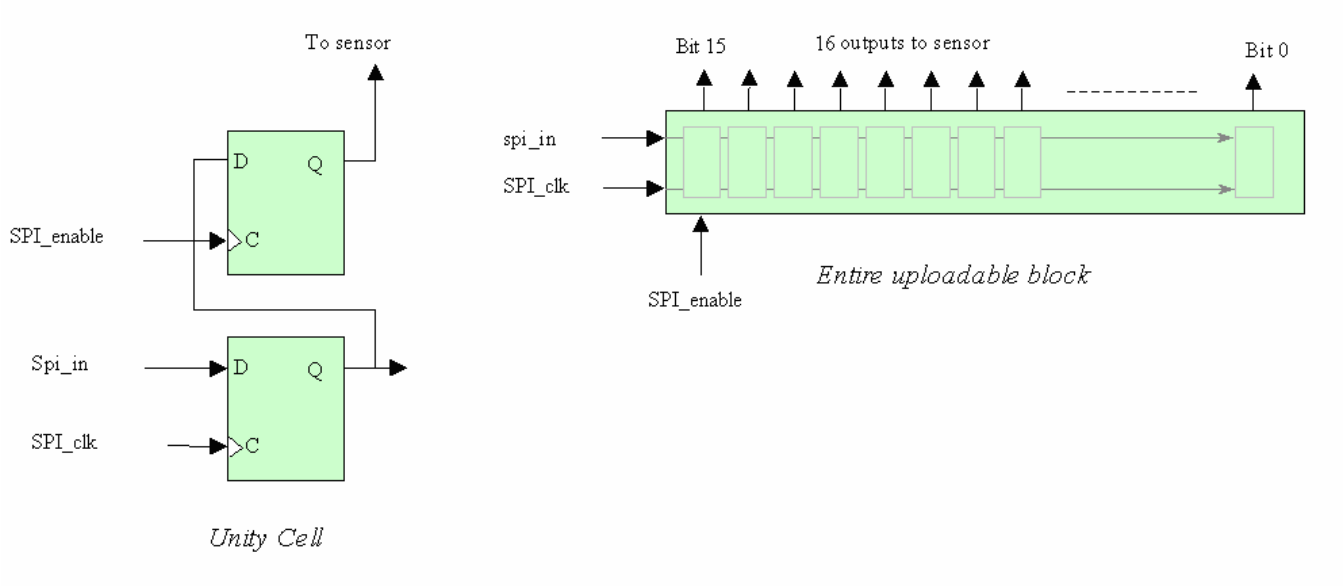
calib_adc<32:24>: 000011011011

Data Interface (SPI)

The serial-3-wire interface (or Serial-to-Parallel Interface) uses a serial input to shift the data in the register buffer. When the complete data word is shifted into the register buffer the data word is loaded into the internal register where it is decoded.

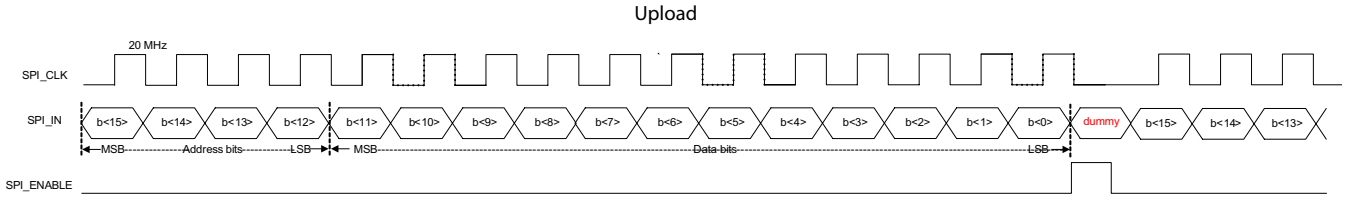
Below is a schematic of what the 16 bit SPI register looks like

Figure 11. Schematic of the SPI



The timing of the SPI register is explained in the timing diagram below

Figure 12. Timing of the SPI.



SPI_IN (15:12): Address bits

SPI_IN (11:0): Data bits

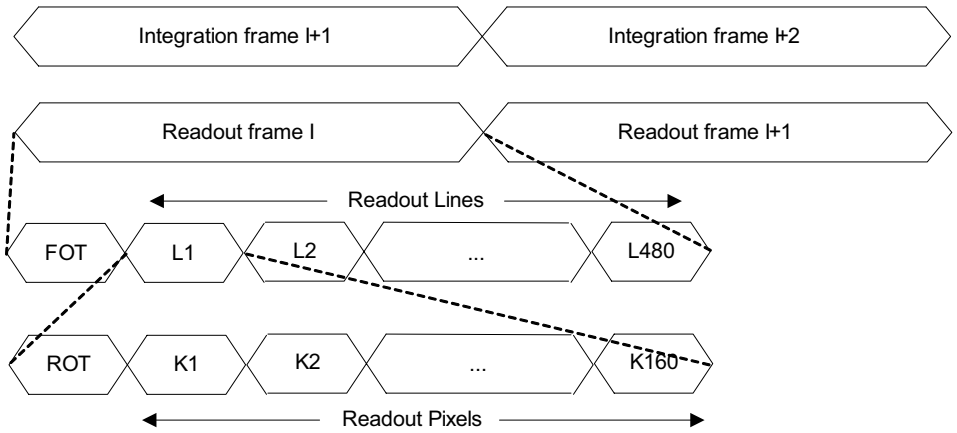
When SPI_ENABLE is asserted the parallel data is loaded into the internal registers of the LUPA300. The frequency of SPI_CLK is 20 MHz or lower. The SPI bits have a default value that allows the sensor to be read out at full resolution without uploading the SPI bits.

Timing and Readout of the Image Sensor

The timing of the sensor consists of 2 parts. The first part is related with the integration time and the control of the pixel. The second part is related with the readout of the image sensor. Integration and readout can be in parallel. In this case the integration time of frame I is ongoing during readout of frame I-1. *Figure 13* shows this parallel timing structure.

The readout of every frame starts with a Frame Overhead Time (FOT) during which the analog value on the pixel diode is transferred to the pixel memory element. After this FOT, the sensor is read out line per line. The readout of every line starts with a Row Overhead Time (ROT) during which the pixel value is put on the column lines. Then the pixels are selected in groups of 4. So in total 160 kernels of 4 pixels are read out. The internal timing is generated by the sequencer. The sequencer can operate in 2 modes: master mode and slave mode. In master mode all the internal timing is controlled by the sequencer, based on the SPI settings. In slave mode the integration timing is directly controlled over three pins, the readout timing is still controlled by the sequencer. The selection between master and slave mode is done by the MASTERMODE register of the SPI. The sequencer is clocked on the core clock; this is the same clock as the ADCs. The core clock is the input clock divided by 4.

Figure 13. Global Readout Timing



Integration Timing

Integration Timing in Mastermode

In mastermode the integration time, the dual slope (DS) integration time and triple slope (TS) integration time are set by the SPI settings. *Figure 14* shows the integration timing and the relationship with the SPI registers. The timing concerning integration is expressed in number of lines read out. The timing is controlled by 4 SPI registers which need to be uploaded with the desired number of lines. This number is then compared with the line counter that keeps track of the number of lines that is read out.

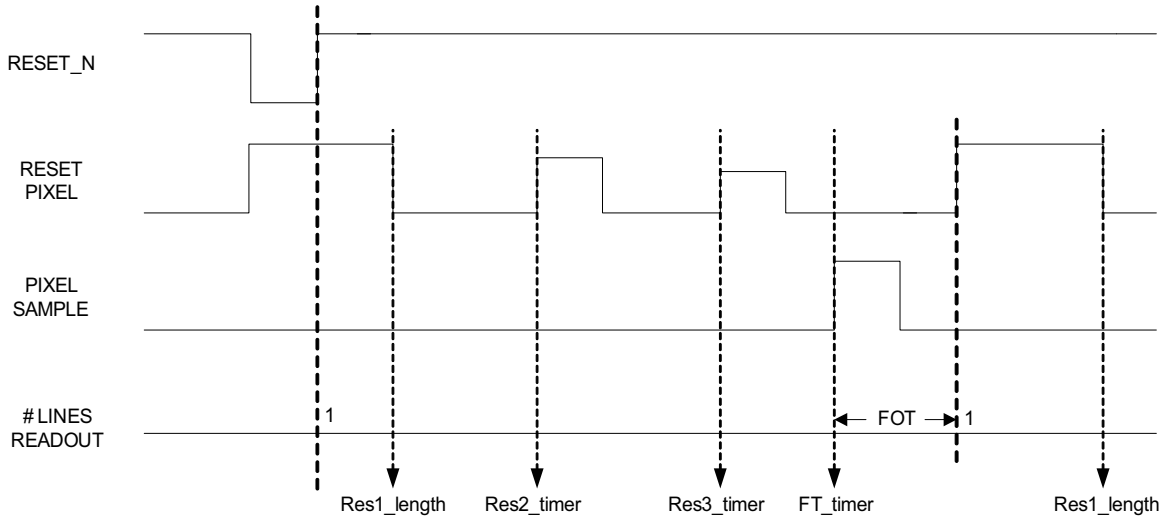
RES1_LENGTH <11:0>: The number of lines read out (minus 1) after which the pixel reset will drop and the integration will start.

RES2_TIMER <11:0>: The number of lines read out (minus 1) after which the dual slope reset pulse will be given. The length of the pulse is given by the formula: 4*(12*(GRAN<1:0>+1)+1) (in clock cycles).

RES3_TIMER < 11:0>: The number of lines read out (minus 1) after which the triple slope reset pulse will be given. The length of the pulse is given by the formula: 4*(12*(GRAN<1:0>+1)+1) (in clock cycles).

FT_TIMER <11:0>: The number of lines read out (minus 1) after which the Frame Transfer (FT) and the FOT will start. The length of the pulse is given by the formula: 4*(12*(GRAN<1:0>+1)+1) (in clock cycles).

Figure 14. Integration Timing in mastermode

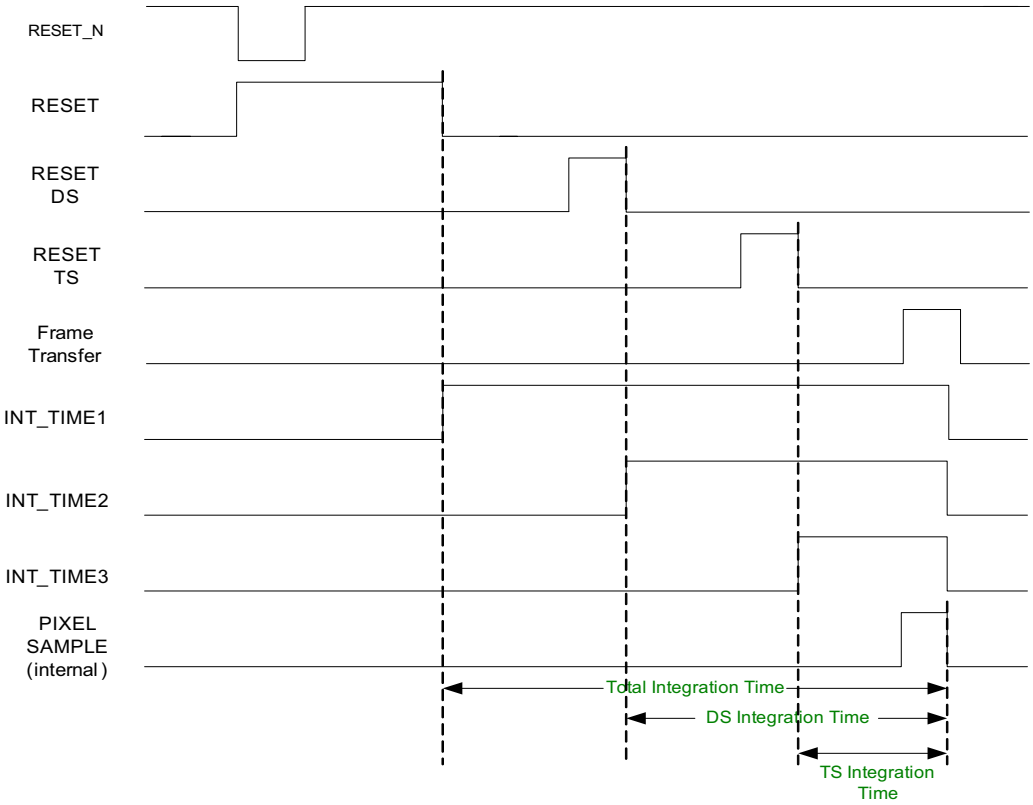


The line counter starts with the value 1 immediately after the rising edge of RESET_N and after the end of the FOT. This means that 4 integration timing registers above need to be upload with the desired number of lines plus one.

In subsampling mode the line counter increases with steps of 2. In this mode the counter starts with the value 2 immediately with the rising edge of RESET_N. This means that for correct operation, the 4 integration timing registers can only be uploaded with an even number of lines if subsampling is enabled.

The length of the integration time, the DS integration time and the TS integration time are indicated by 3 output pins: INT_TIME_1, INT_TIME_2 and INT_TIME_3. These outputs are high during the actual integration time. This is from the falling edge of the corresponding reset pulse to the falling edge of the internal pixel sample. *Figure 15* illustrates this. The internal pixel sample rises at the moment defined by FT_TIMER (see *Figure 14*) and the length of the pulse is 4*(12*(GRAN<1:0>+1)+2).

Figure 15. INT_TIME Timing



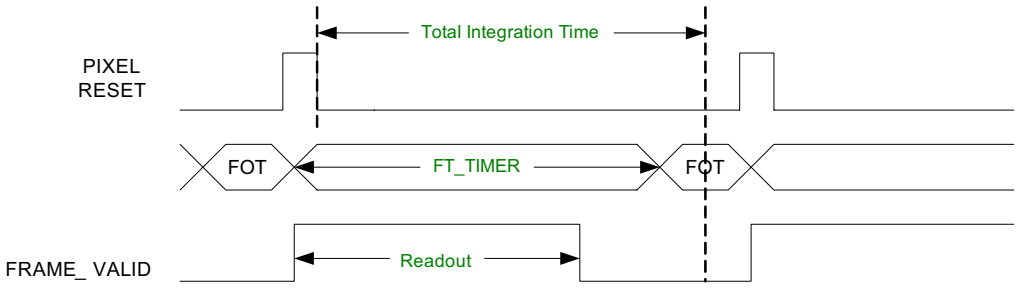
Readout Time Smaller Than or Equal to Integration Time

In this situation the RES_LENGTH register can be uploaded with the smallest possible value, this is the value '2'. In this case the frame rate is determined by the integration time. In the case the readout time is equal to the integration time, the FT_TIMER register is uploaded with a value equal to the window size to readout plus one. In case the readout time is smaller than the integration time the FT_TIMER register will be uploaded with a value bigger than the window size.

Figure 16 shows this principle. While the sensor is being readout the FRAME_VALID signal will go high to indicate the time needed to read out the sensor.

When windowing in Y direction is desired in this mode (longer integration time than read-out time) the following parameters should be set: The integration time is set by the FT_TIMER register. The actual windowing in Y is achieved when the surrounding system discards the lines which are not desired for the selected window.

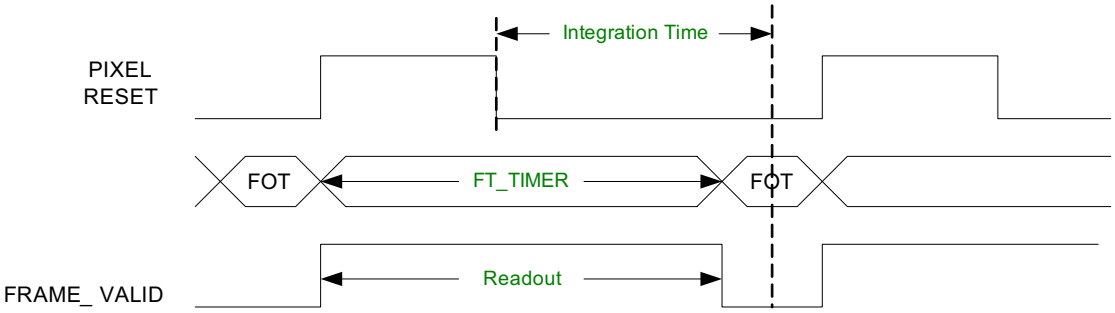
Figure 16. Readout time smaller then Integration time



Readout Time Larger Than Integration Time

In case the readout time is larger than then integration time, the RES_LENGTH register needs to be uploaded with a value larger than two to compensate for the larger readout time. The FT_TIMER register has to be set to the desired window size (in Y). Only the RES_LENGTH register needs to be changed during operation. *Figure 17* shows this example.

Figure 17. Readout time larger then Integration time

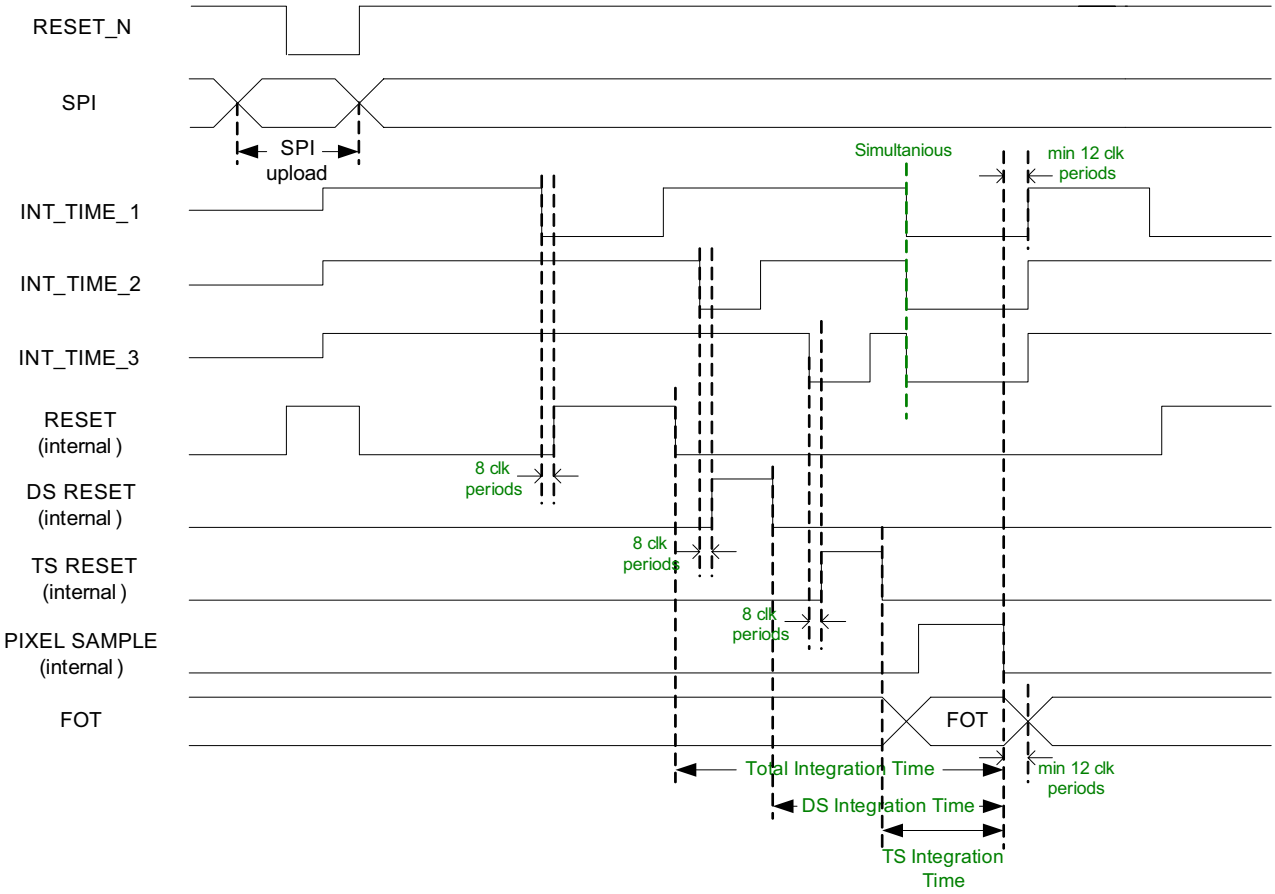


Integration Timing in Slave Mode

In slave mode the registers RES_LENGTH, DS_TIMER, TS_TIMER and FT_TIMER are ignored. The integration timing is now controlled by the pins INT_TIME_1, INT_TIME_2 and INT_TIME_3, which are now active low input pins.

The relationship between the input pins and the integration timing is illustrated in 18. The pixel is reset as soon as IN_TIME_1 is low (active) and INT_TIME_2 and INT_TIME_3 are high. The integration starts when INT_TIME_1 becomes high again and during this integration additional (lower) reset can be given by activating INT_TIME_2 and INT_TIME_3 separately. At the end of the desired integration time the frame transfer starts by making all 3 INT_TIME pins active low simultaneously. There is always a small delay between the applied external signals and the actual internally generated pulses. These delays are also shown in *Figure 18*

Figure 18. Integration Timing in Slave Mode.



In case non-destructive readout is used, the pulses on the input pins still need to be given. By setting the NDR bit to "1" the internal pixel reset pulses are suppressed but the external pulses are still needed to have the correct timing of the frame transfer.

Readout Timing

The sensor is readout row by row. The LINE_VALID signal shows when valid data of a row is at the outputs. FRAME_VALID shows which LINE_VALIDs are valid. LINE_VALIDs when FRAME_VALID is low, must be discarded. *Figure 19* and *Figure 20* illustrate this.

Note: The FRAME_VALID signal will automically go low after 480 LINE_VALID pulses in mastermode

Figure 19. LINE_VALID Timing.

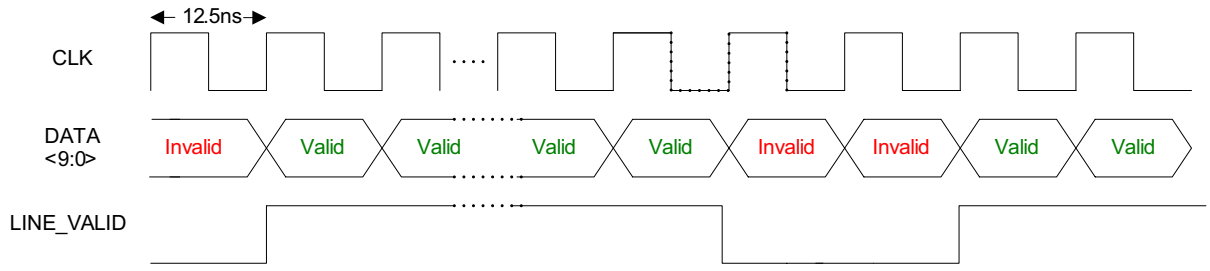
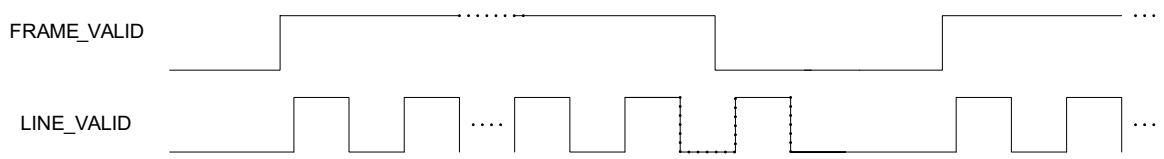


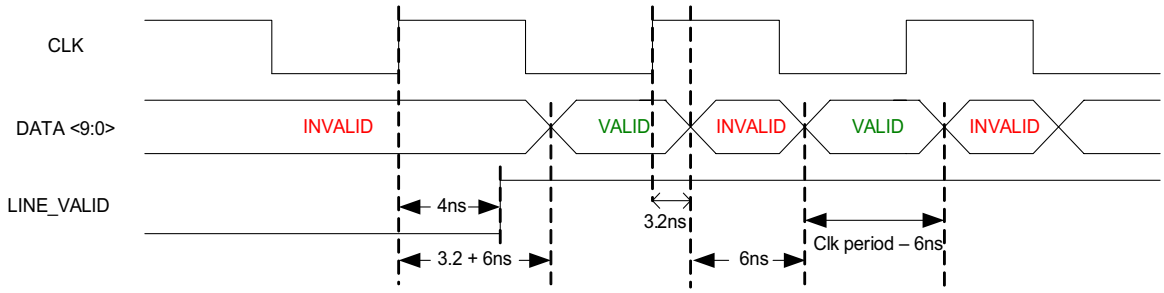
Figure 20. FRAME_VALID Timing



The data at the output of the sensor is clocked on the rising edge of CLK. There is a delay of 3.2 ns between the rising edge of CLK and a change in DATA<9:0>. After this delay DATA<9:0> needs 6 ns to become stable within 10% of VDDD. This means that DATA<9:0> is stable for a time equal to the clock period minus 6 ns. *Figure 21* illustrates this.

Note: In slave mode, line valids that occur beyond the desired image window should be discarded by the user's image data acquisition system

Figure 21. DATA<9.0> Valid Timing



Readout timing in slave mode

The start pointer of the window to readout is still determined by the START_X and START_Y registers (as by readout in master mode). The size of the window in x-direction is also still determined by the NB_OF_PIX register. The length of the window in y-direction is determined by the externally applied integration timing. The sensor cannot know the desired y-size to readout. It will therefore readout all lines starting from START_Y. The readout of lines will continue until the user decides to start the FOT.

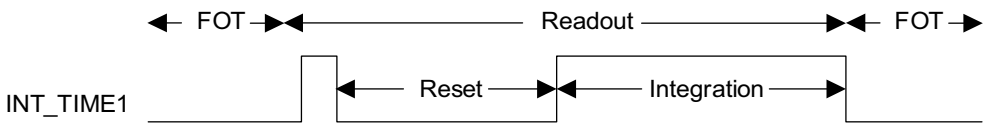
Even when the line pointer wants to address non existing rows (row 481 and higher), the sequencer will continue to run in normal readout mode. This means that FRAME_VALID remains high and LINE_VALID is toggled as if normal lines are readout. The controller of the user should take care of this and ignore the LINE_VALIDs that correspond with non existing lines and LINE_VALIDs that correspond with lines that are not inside the desired readout window.

The length of the FOT and ROT is still controlled by the GRAN register as described in this data sheet.

Readout time longer than integration time

The sensor should be timed according to the formulas and diagram below:

1. INT_TIME_1 should be brought high at time (read_t - int_t) and preferably immediately after the falling edge of LINE_VALID.
2. At time read_t all INT_TIME_x should simultaneous go low to start the FOT. This is immediately after the falling edge of the last LINE_VALID of the desired readout window.

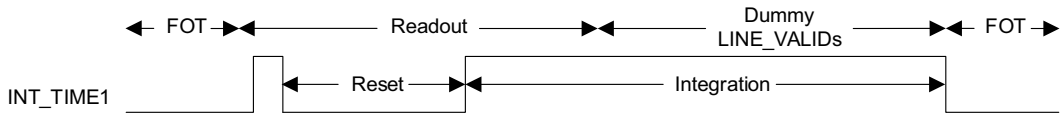


Readout time shorter than integration time

The sensor should be timed according to the formulas and diagram below:

1. INT_TIME_1 should be brought high after a minimum 2 µs reset time and preferably immediately after the falling edge of the first LINE_VALID.
2. At time read_t after the last valid LINE_VALID of the desired window size, all other LINE_VALIDs should be ignored.

3. After the desired integration length all INT_TIME_x should simultaneous go low to start the FOT.

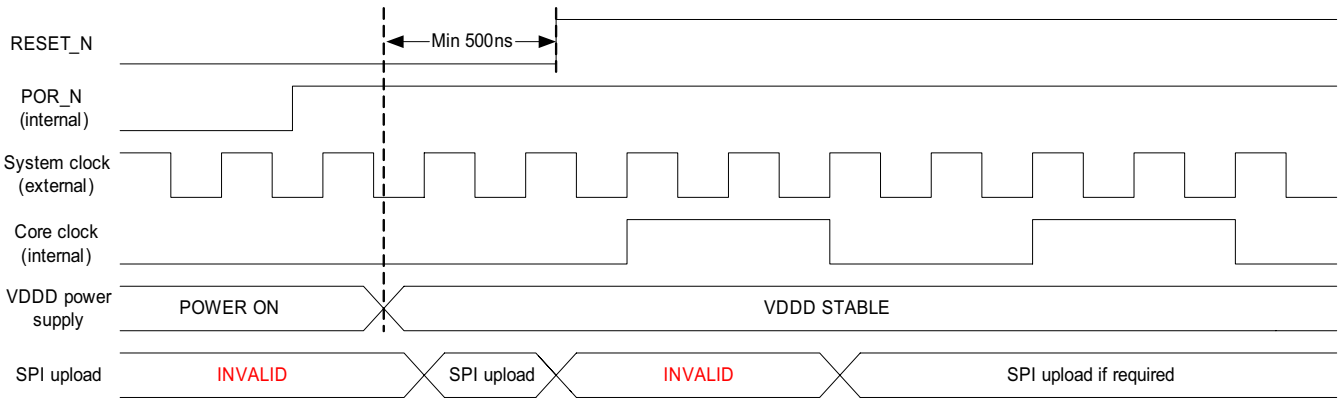


Startup Timing

On start-up VDDD should rise together with or before the other supplies. The rise of VDDD should be limited to 1V/100 µs to avoid the activation of the on chip ESD protection circuitry.

During the rise of VDDD an on chip POR_N signal is generated that resets the SPI registers to its default setting. After VDDD is stable the SPI settings can be uploaded to configure the sensor for future readout and light integration. When powering on the VDDD supply, the RESET_N pin should be kept low to reset the on chip sequencer and addressing logic. The RESET_N pin must remain low until all initial SPI settings are uploaded. RESET_N pin must remain low for at least 500 ns after ALL supplies are stable. The rising edge of RESET_N starts the on chip clock division. The second rising edge of CLK after the rising edge of RESET_N, triggers the rising edge of the core clock. Some SPI settings can be uploaded after the core clock has started. See the chapter about the SPI settings for this.

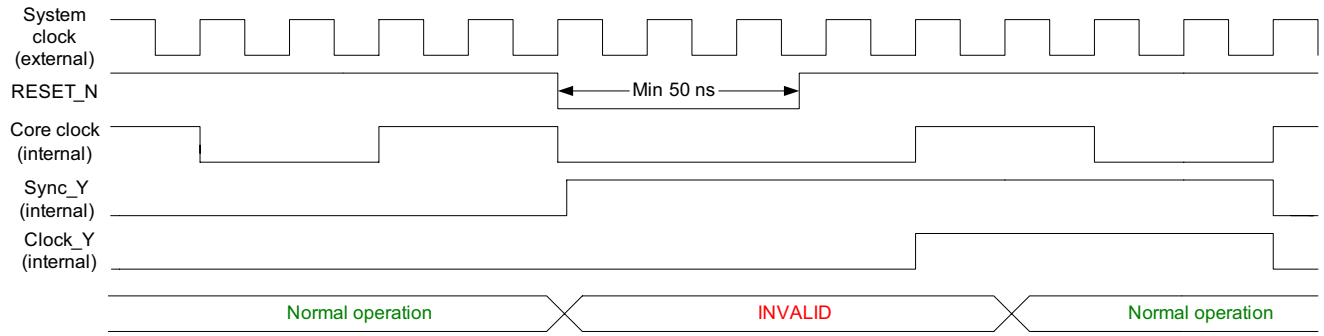
Figure 22. Start-Up Timing



Sequencer Reset Timing

By bringing RESET_N low for at least 50 ns, the on chip sequencer is reset to its initial state. The internal clock division is restarted. The second rising edge of CLK after the rising edge of RESET_N the internal clock is restarted. The SPI settings are not affected by RESET_N. If needed the SPI settings can be changed during a low level of RESET_N.

Figure 23. Sequencer Reset Timing



Pinlist

Table 17. Pinlist

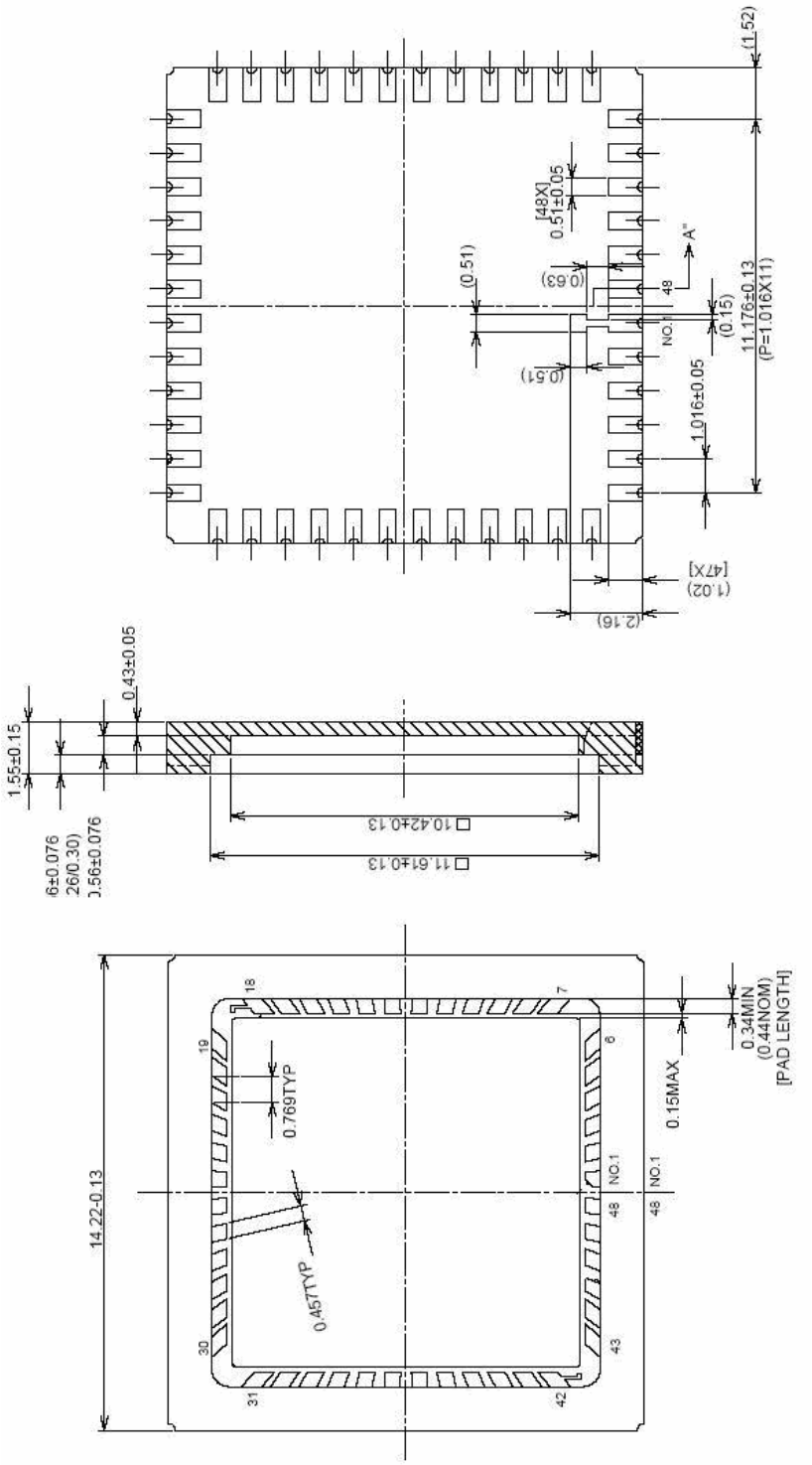
Nr.	Name	Type	Description
1	GND_{ADC}	Ground	Ground supply of the ADCs
2	DATA<5>	Output	Databit<5>
3	DATA<6>	Output	Databit<6>
4	DATA<7>	Output	Databit<7>
5	DATA<8>	Output	Databit<8>
6	DATA<9>	Output	Databit<9> (MSB)
7	GND_D	Ground	Digital ground supply
8	V_{DDD}	Supply	Digital power supply (2.5V)
9	GND_{ADC}	Ground	Ground supply of the ADCs
10	V_{ADC}	Supply	Power supply of the ADCs (2.5V)
11	GND_A	Ground	Ground supply of analog readout circuitry
12	V_{DDA}	Supply	Power supply of analog readout circuitry (2.5V)
13	ADC_BIAS	Biasing	Biasing of ADCs. Connect with 10 kOhm to VADC and decouple with 100n to GND_ADC.
14	BIAS4	Biasing	Biasing of amplifier stage. Connect with 110 kOhm to VDDA and decouple with 100 nF to GNDA.
15	BIAS3	Biasing	Biasing of columns. Connect with 42 kOhm to VDDA and decouple with 100 nF to GNDA.
16	BIAS2	Biasing	Biasing of columns. Connect with 1.5 MOhm to VDDA and decouple with 100 nF to GNDA.
17	BIAS1	Biasing	Biasing of imager core. Connect with 500 kOhm to VDDA and decouple with 100 nF to GNDA.
18	VPIX	Supply	Power supply of pixel array (2.5V)
19	SPI_ENABLE	Digital input	Enable of the SPI
20	SPI_CLK	Digital input	Clock of the SPI. (max. 20 MHz)
21	SPI_DATA	Digital IO	Data line of the SPI. Bidirectional pin
22	VMEM_H	Supply	Supply of vmem_high of pixelarray (3.3V)
23	GND_DRIVERS	Ground	Ground of pixel array drivers
24	VRESET_1	Supply	Reset supply voltage (typical 3.3V)
25	VRESET_2	Supply	Dual slope reset supply voltage. Connect to other supply or ground when dual slope reset is not used.
26	VRESET_3	Supply	Triple slope reset supply voltage. Connect to other supply or ground when triple slope reset is not used.
27	PRECHARGE_BIAS	Bias	Connect with 68 kOhm to VPIX and decouple with 100 nF to GND_DRIVERS.
28	LINE_VALID	Digital output	Indicates when valid data is at the outputs. Active high
29	FRAME_VALID	Digital output	Indicates when valid frame is readout.

Table 17. Pinlist (continued)

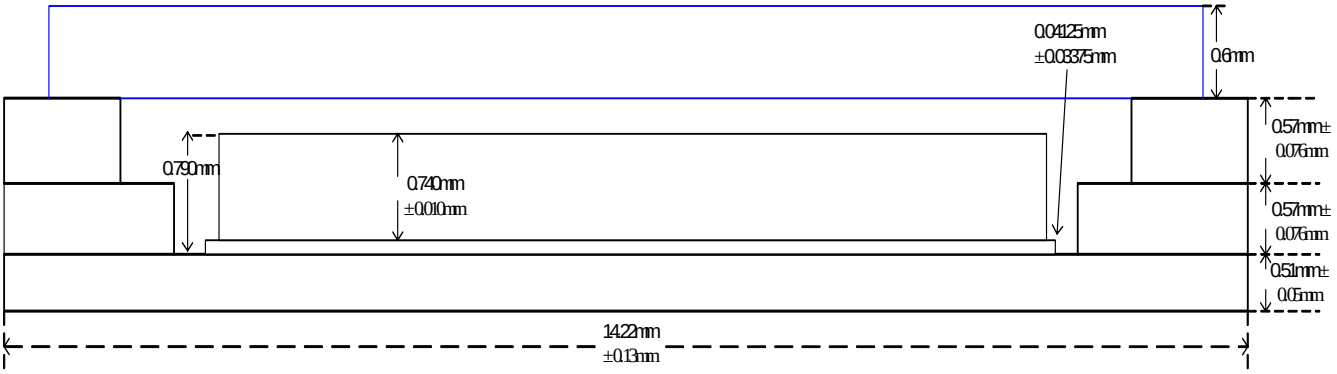
Nr.	Name	Type	Description
30	INT_TIME_3	Digital IO	In master mode: Output to indicate the triple slope integration time. In slave mode: Input to control the triple slope integration time.
31	INT_TIME_2	Digital IO	In master mode: Output to indicate the dual slope integration time. In slave mode: Input to control the dual slope integration time.
32	INT_TIME_1	Digital IO	In master mode: Output to indicate the integration time. In slave mode: Input to control integration time.
33	V_{DDD}	Supply	Digital power supply (2.5V)
34	GND_D	Ground	Digital ground supply
35	V_{DDA}	Supply	Power supply of analog readout circuitry (2.5V)
36	GND_A	Ground	Ground supply of analog readout circuitry
37	RESET_N	Digital input	Sequencer reset, active low
38	CLK	Digital input	Readout clock (80 MHz), sine or square clock
39	V_{ADC}	Supply	Power supply of the ADCs (2.5V)
40	GND_{ADC}	Ground	Ground supply of the ADCs
41	V_{DDO}	Supply	Power supply of the output drivers (2.5V)
42	GND_O	Ground	Ground supply of the output drivers
43	DATA<0>	Output	Databit<0> (LSB)
44	DATA<1>	Output	Databit<1>
45	DATA<2>	Output	Databit<2>
46	DATA<3>	Output	Databit<3>
47	DATA<4>	Output	Databit<4>
48	V_{ADC}	Supply	Power supply of the ADCs (2.5V)

Package Drawing

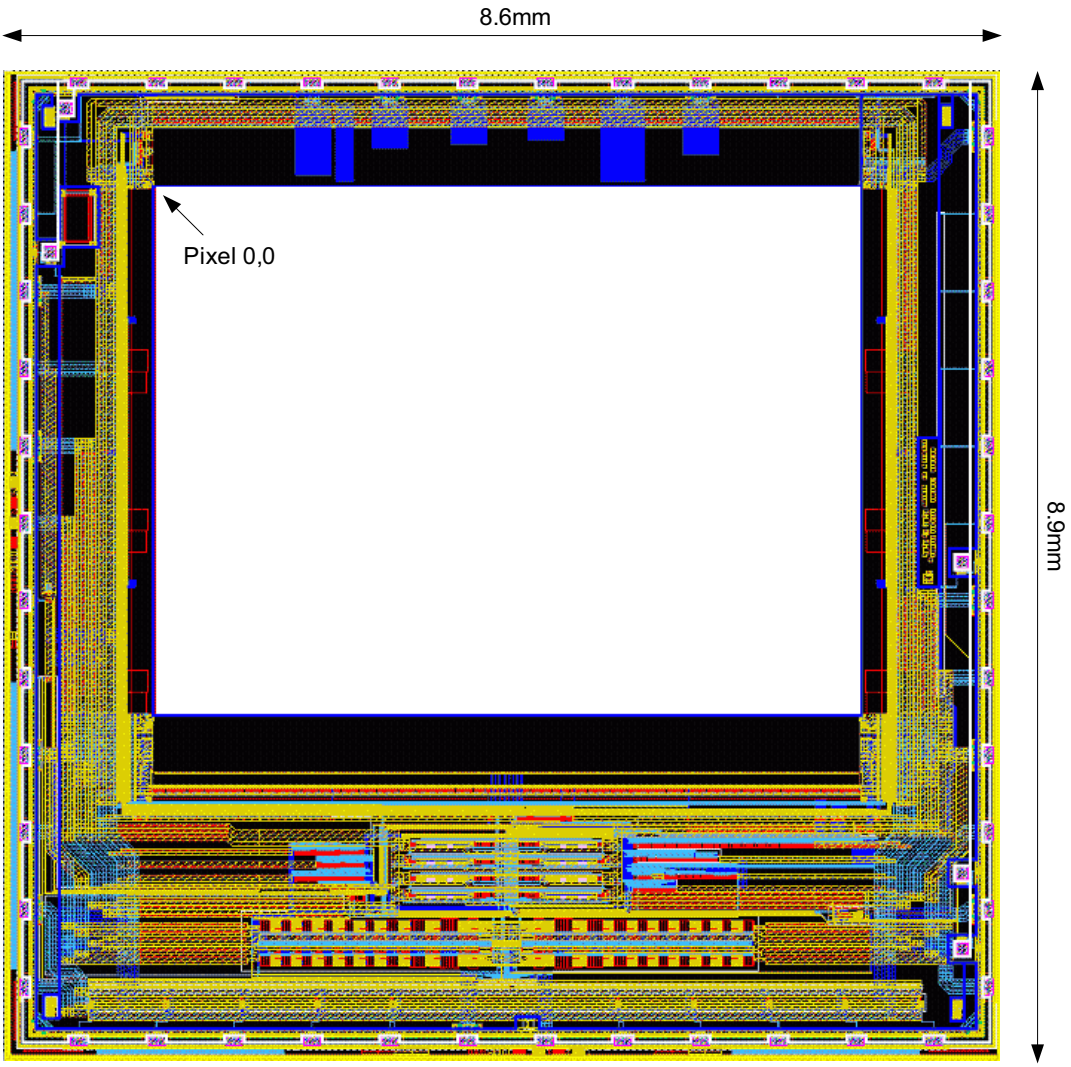
Figure 24. Package drawing



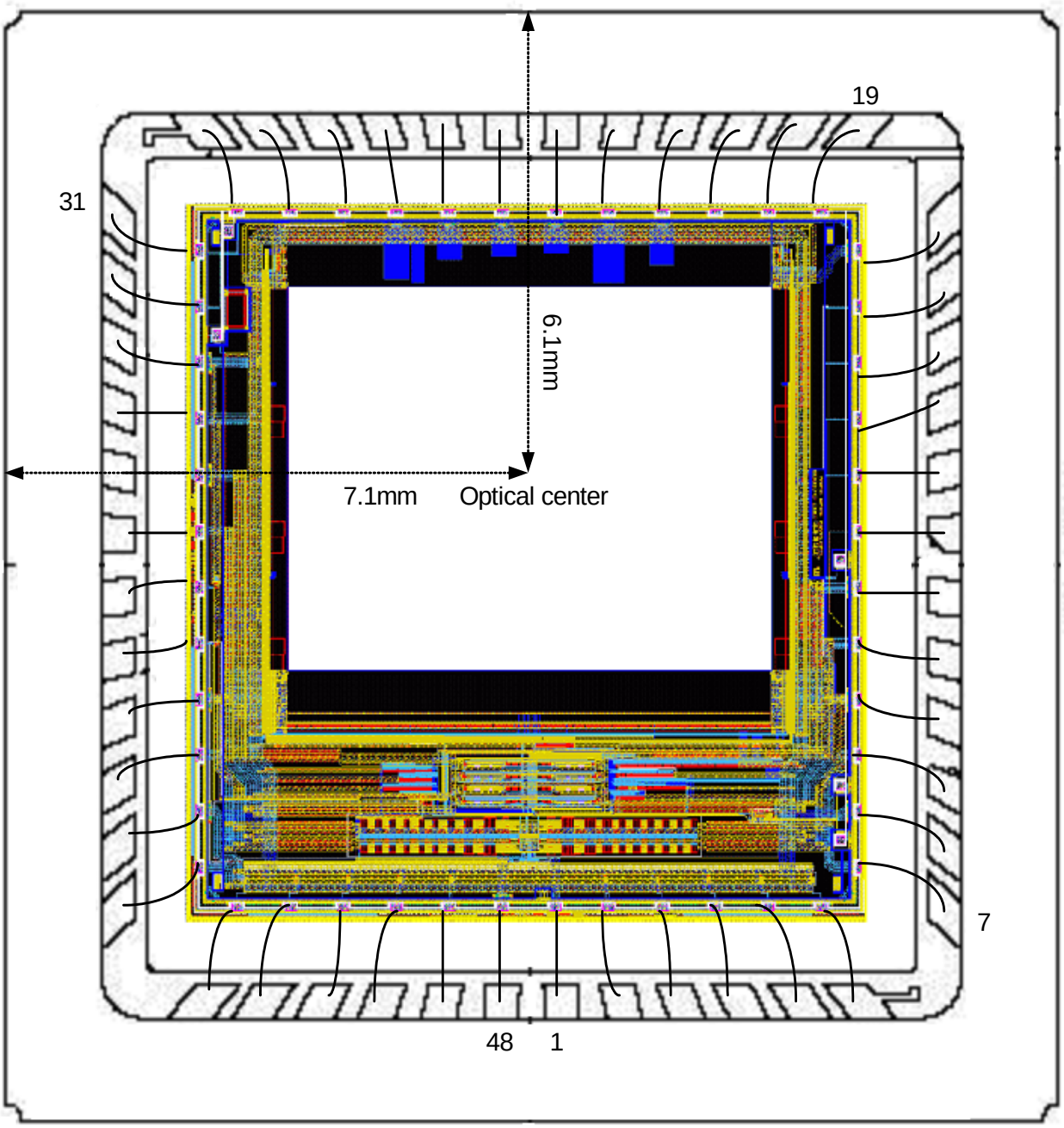
Package with Glass



Die Specifications



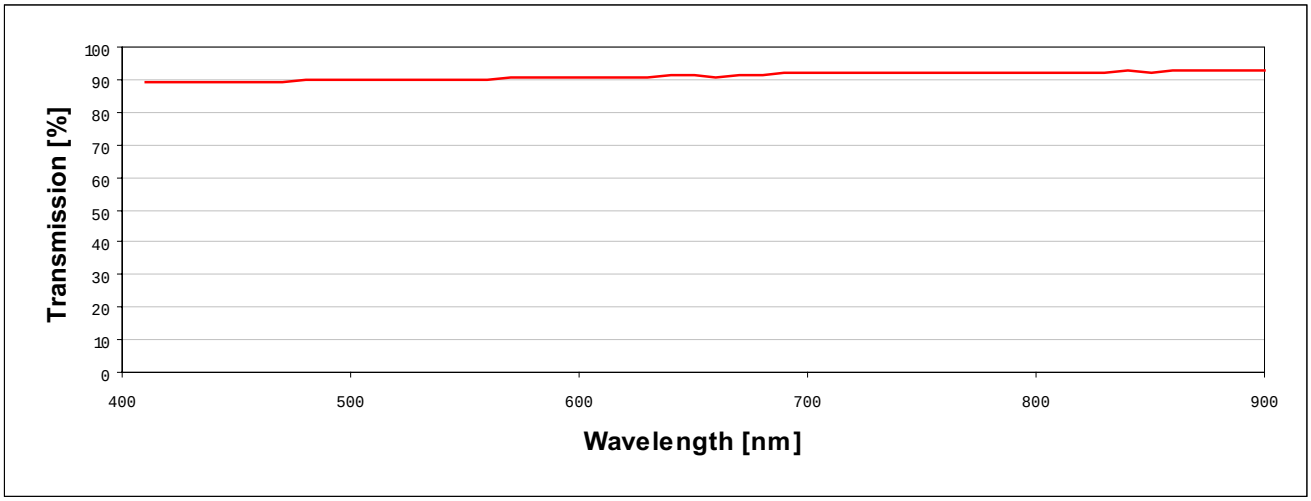
Die in Package



Glass Lid

A D263 glass will be used as protection glass lid on top of the LUPA-300 monochrome and color sensors. *Figure 25* shows the transmission characteristics of the D263 glass.

Figure 25. Transmission characteristics of the D263 glass used as protective cover for the LUPA-1300 sensors

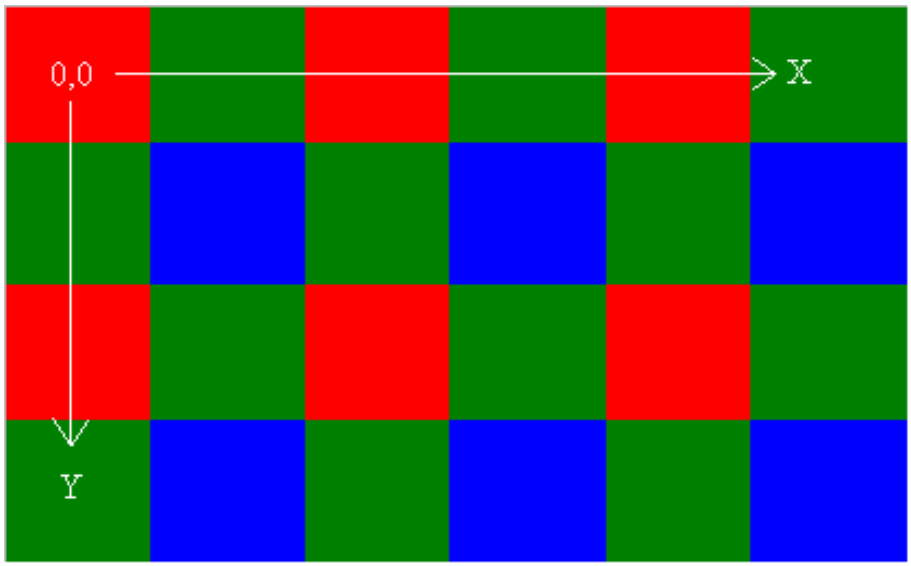


As can be seen in *Figure 25* no infrared attenuating color filter glass is used. This means that it is required for the user to provide this filter in the optical path when color devices are used.

Color Filter

An optional color filter can be processed as well. The LUPA-300 can also be processed with a Bayer RGB color pattern. Pixel (0,0) has a red filter

Figure 26. Color filter arrangement on the pixels.



Handling Precautions

Special care should be given when soldering image sensors with color filter arrays (RGB color filters), onto a circuit board, since color filters are sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. The following recommendations are made to ensure that sensor performance is not compromised during end-users' assembly processes.

Board Assembly:

Device placement onto boards should be done in accordance with strict ESD controls for Class 0, JESD22 Human Body Model, and Class A, JESD22 Machine Model devices. Assembly operators should always wear all designated and approved grounding equipment; grounded wrist straps at ESD protected workstations are recommended including the use of ionized blowers. All tools should be ESD protected.

Manual Soldering:

When a soldering iron is used the following conditions should be observed:

- Use a soldering iron with temperature control at the tip.
- The soldering iron tip temperature should not exceed 350°C.
- The soldering period for each pin should be less than 5 seconds.

Precautions and cleaning:

Avoid spilling solder flux on the cover glass; bare glass and particularly glass with antireflection filters may be adversely affected by the flux. Avoid mechanical or particulate damage to the cover glass.

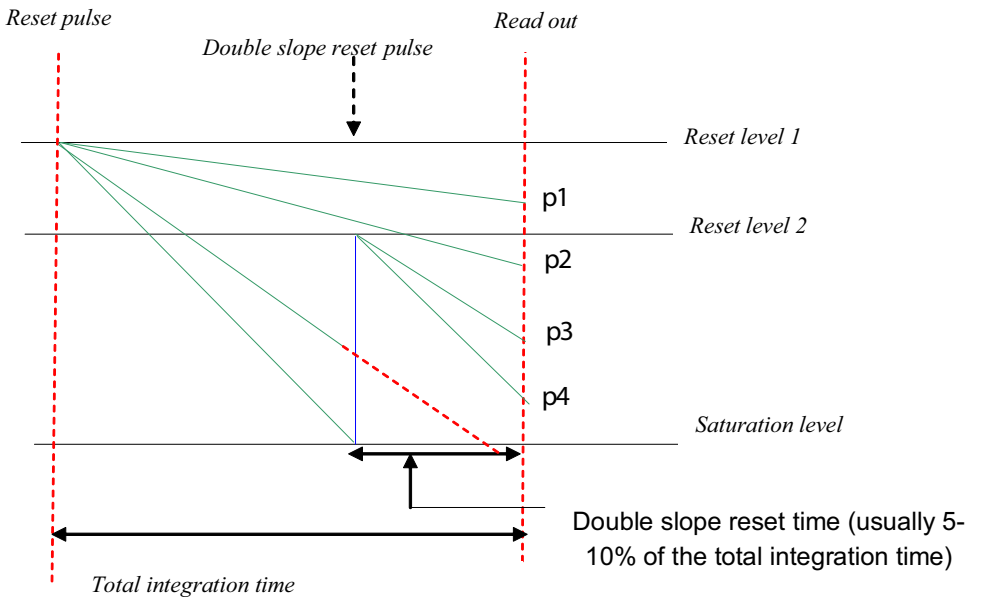
It is recommended that isopropyl alcohol (IPA) be used as a solvent for cleaning the image sensor glass lid. When using other solvents, it should be confirmed beforehand whether the solvent will dissolve the package and/or the glass lid or not.

APPENDIX A: Frequently Asked Questions

Q: How does the dual (multiple) slope extended dynamic range mode work?

A:

Figure 27. Dual Slope Diagram



The green lines are the analog signal on the photodiode, which decrease as a result of exposure. The slope is determined by the amount of light at each pixel (the more light the steeper the slope). When the pixels reach the saturation level the analog signal will not change despite further exposure. As you can see, without any double slope pulse pixels p3 and p4 will reach saturation before the sample moment of the analog values--no signal will be acquired without double slope. When double slope is enabled a second reset pulse will be given (blue line) at a certain time before the end of the integration time. This double slope reset pulse resets the analog signal of the pixels BELOW this level to the reset level. After the reset the analog signal starts to decrease with the same slope as before the double slope reset pulse. If the double slope reset pulse is placed at the end of the integration time (90% for instance) the analog signal that would have reach the saturation levels aren't saturated anymore (this increases the optical dynamic range) at read out. It's important to notice that pixel signals above the double slope reset level will not be influenced by this double slope reset pulse (p1 and p2). If desired, additional reset pulses can be given at lower levels to achieve multiple slope.

Document History Page

Document Title: LUPA-300 CMOS Image Sensor Document Number: 001-00371				
REV.	**ECN.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	386743	See ECN	FPW	Initial Cypress release
*A	391272	See ECN	FPW	Added spectral and photo voltaic response curve. Updated specifications according to the characterization measurements
*B	422288	See ECN	FPW	Removed note about nb_pix in X because the problem was solved. Removed the 68 pin JLCC pinlist. Changed footer in some pages
*C	497126	See ECN	QGS	Converted to Frame file
*D	645720	See ECN	FPW	Updated ordering information