CY74FCT16501T
CY74FCT162501T
CY74FCT162H501T

18-Bit Registered Transceiver

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-E speed at 3.8 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6 mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16501T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162501T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

CY74FCT162H501T Features:

- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

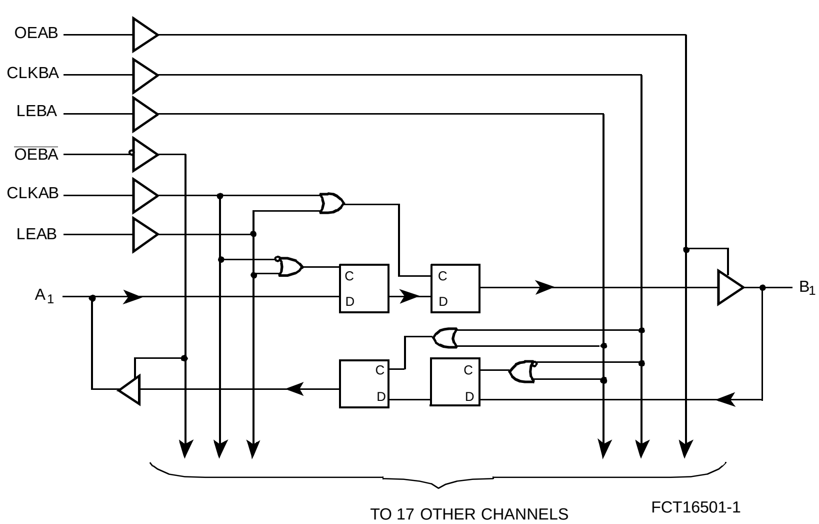
These 18-bit universal bus transceivers can be operated in transparent, latched or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock inputs (CLKAB and CLKBA). For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

The CY74FCT16501T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

THE CY74FCT162501T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162501T is ideal for driving transmission lines.

The CY74FCT162H501T is a 24-mA balanced output part, that has “bus hold” on the data inputs. The device retains the input’s last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

Functional Block Diagram



Pin Configuration

SSOP/TSSOP
Top View

OEAB	1	56	GND
LEAB	2	55	CLKAB
A_1	3	54	B_1
GND	4	53	GND
A_2	5	52	B_2
A_3	6	51	B_3
V_{CC}	7	50	V_{CC}
A_4	8	49	B_4
A_5	9	48	B_5
A_6	10	47	B_6
GND	11	46	GND
A_7	12	45	B_7
A_8	13	44	B_8
A_9	14	43	B_9
A_{10}	15	42	B_{10}
A_{11}	16	41	B_{11}
A_{12}	17	40	B_{12}
GND	18	39	GND
A_{13}	19	38	B_{13}
A_{14}	20	37	B_{14}
A_{15}	21	36	B_{15}
V_{CC}	22	35	V_{CC}
A_{16}	23	34	B_{16}
A_{17}	24	33	B_{17}
GND	25	32	GND
A_{18}	26	31	B_{18}
$\overline{\text{OEBA}}$	27	30	CLKBA
LEBA	28	29	GND

FCT16501-2

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Pin Description

Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs[1]
B	B-to-A Data Inputs or A-to-B Three-State Outputs[1]

Function Table[2, 3]

Inputs				Outputs
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B[4]
H	L	H	X	B[5]

Maximum Ratings[6, 7]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–55°C to +125°C

Ambient Temperature with
Power Applied ....–55°C to +125°C

DC Input Voltage.. –0.5V to +7.0V

DC Output Voltage... –0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin)...........................–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.. >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	–40°C to +85°C	5V ± 10%

Notes:

1. On the 74FCT162H501T these pins have bus hold.
2. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance
   ↑ = LOW-to-HIGH Transition
4. Output level before the indicated steady-state input conditions were established.
5. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
6. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
7. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Conditions		Min.	Typ.[8]	Max.	Unit
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_H	Input Hysteresis[9]					100		mV
V_{IK}	Input Clamp Diode Voltage		V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_{IH}	Input HIGH Current	Standard	V_{CC}=Max., V_I=V_{CC}				±1	μA
		Bus Hold					±100	
I_{IL}	Input LOW Current	Standard	V_{CC}=Max., V_I=GND				±1	μA
		Bus Hold					±100	μA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[10]		V_{CC}=Min.,	V_I=2.0V	–50			μA
				V_I=0.8V	+50			μA
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[10]		V_{CC}=Max., V_I=1.5V				TBD	mA
I_{OZH}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=2.7V				±1	μA
I_{OZL}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=0.5V				±1	μA
I_{OS}	Short Circuit Current[11]		V_{CC}=Max., V_{OUT}=GND		–80	–140	–200	mA
I_O	Output Drive Current[11]		V_{CC}=Max., V_{OUT}=2.5V		–50		–180	mA
I_{OFF}	Power-Off Disable		V_{CC}=0V, V_{OUT}≤4.5V[12]				±1	μA

Output Drive Characteristics for CY74FCT16501T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=–15 mA	2.4	3.5		
		V_{CC}=Min., I_{OH}=–32 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162501T, CY74FCT162H501T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
I_{ODL}	Output LOW Current[11]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[11]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Notes:

8. Typical values are at V_{CC}= 5.0V, T_A= +25°C ambient.
9. This parameter is guaranteed but not tested.
10. Pins with bus hold are described in Pin Description.
11. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
12. Tested at +25°C.

Capacitance[9] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[8]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Sym.	Parameter	Test Conditions[13]		Min.	Typ.[8]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V V_{IN}≥V_{CC}–0.2V	—	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current TTL inputs HIGH	V_{CC}= Max., V_{IN} = 3.4V[14]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[15]	V_{CC}=Max., Outputs Open OEAB=$\overline{OEBA}$=V_{CC} or GND One Input Toggling, 50% Duty Cycle	V_{IN}=V_{CC} or V_{IN}=GND	—	75	120	μA/MHz
I_C	Total Power Supply Current[16]	V_{CC}=Max., Outputs Open f_0 =10MHz (CLKAB) 50% Duty Cycle OEAB=$\overline{OEBA}$=V_{CC} LEAB = GND, One Bit Toggling f_1 = 5MHz, 50% Duty Cycle	V_{IN}=V_{CC} or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	
		V_{CC}=Max., Outputs Open f_0 = 10MHz (CLKAB) 50% Duty Cycle OEAB=$\overline{OEBA}$=V_{CC} LEAB=GND Eighteen Bits Toggling f_1=2.5MHz, 50% Duty Cycle	V_{IN}=V_{CC} or V_{IN}=GND	—	3.8	6.5[17]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.5	20.8[17]	

Notes:

13. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
14. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
15. This parameter is not directly testable, but is derived for use in Total Power Supply.
16. I_C= $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
17. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range[18]

Parameter	Description		CY74FCT16501AT CY74FCT162501AT CY74FCT162H501AT		CY74FCT16501CT CY74FCT162501CT CY74FCT162H501CT		CY74FCT16501ET CY74FCT162501ET CY74FCT162H501ET		Unit	Fig. No.[19]
			Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	CLKAB or CLKBA frequency[20]		—	150	—	150	—	150	MHz	—
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A		1.5	5.1	1.5	4.6	1.5	3.8	ns	1,3
t_{PLH} t_{PHL}	Propagation Delay LEBA to A, LEAB to B		1.5	5.6	1.5	5.3	1.5	4.2	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay CLKBA to A, CLKAB to B		1.5	5.6	1.5	5.3	1.5	4.2	ns	1,5
t_{PZH} t_{PZL}	Output Enable Time $\overline{\text{OEBA}}$ to A, OEAB to B		1.5	6.0	1.5	5.6	1.5	4.8	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{\text{OEBA}}$ to A, OEAB to B		1.5	5.6	1.5	5.2	1.5	5.2	ns	1,7,8
t_{SU}	Set-Up Time, HIGH or LOW A to CLKAB, B to CLKBA		3.0	—	3.0	—	2.4	—	ns	4
t_H	Hold Time HIGH or LOW A to CLKAB, B to CLKBA		0	—	0	—	0	—	ns	4
t_{SU}	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock LOW	3.0	—	3.0	—	2.0	—	ns	4
		Clock HIGH	1.5	—	1.5	—	1.5	—	ns	4
t_H	Hold Time, HIGH or LOW, A to LEAB, B to LEBA		1.5	—	1.5	—	0.5	—	ns	4
t_W	LEAB or LEBA Pulse Width HIGH[20]		3.0	—	3.0	—	3.0	—	ns	5
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[20]		3.0	—	3.0	—	3.0	—	ns	5
$t_{SK(O)}$	Output Skew[21]		—	0.5	—	0.5	—	0.5	ns	—

Notes:
18. Minimum limits are guaranteed, but not tested, on propagation delays.
19. See "Parameter Measurement Information" in the General Information section.
20. This parameter is guaranteed but not tested.
21. Skew between any two outputs of the same package switching in the same direction. This parameter guaranteed by design.

Ordering Information CY74FCT16501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT16501ETPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16501ETPVC	O56	56-Lead (300-Mil) SSOP	
4.6	CY74FCT16501CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16501CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT16501ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16501ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT162501ETPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162501ETPVC	O56	56-Lead (300-Mil) SSOP	
4.6	CY74FCT162501CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162501CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162501ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162501ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT162H501ETPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H501ETPVC	O56	56-Lead (300-Mil) SSOP	
4.6	CY74FCT162H501CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H501CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162H501ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H501ATPVC	O56	56-Lead (300-Mil) SSOP	

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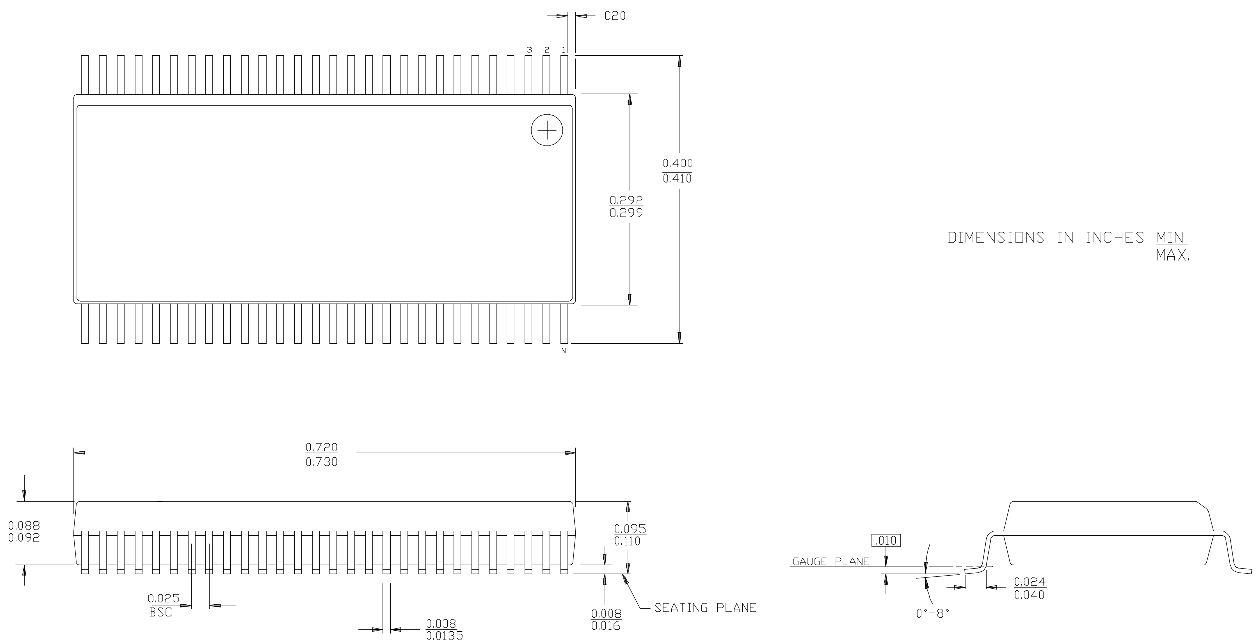
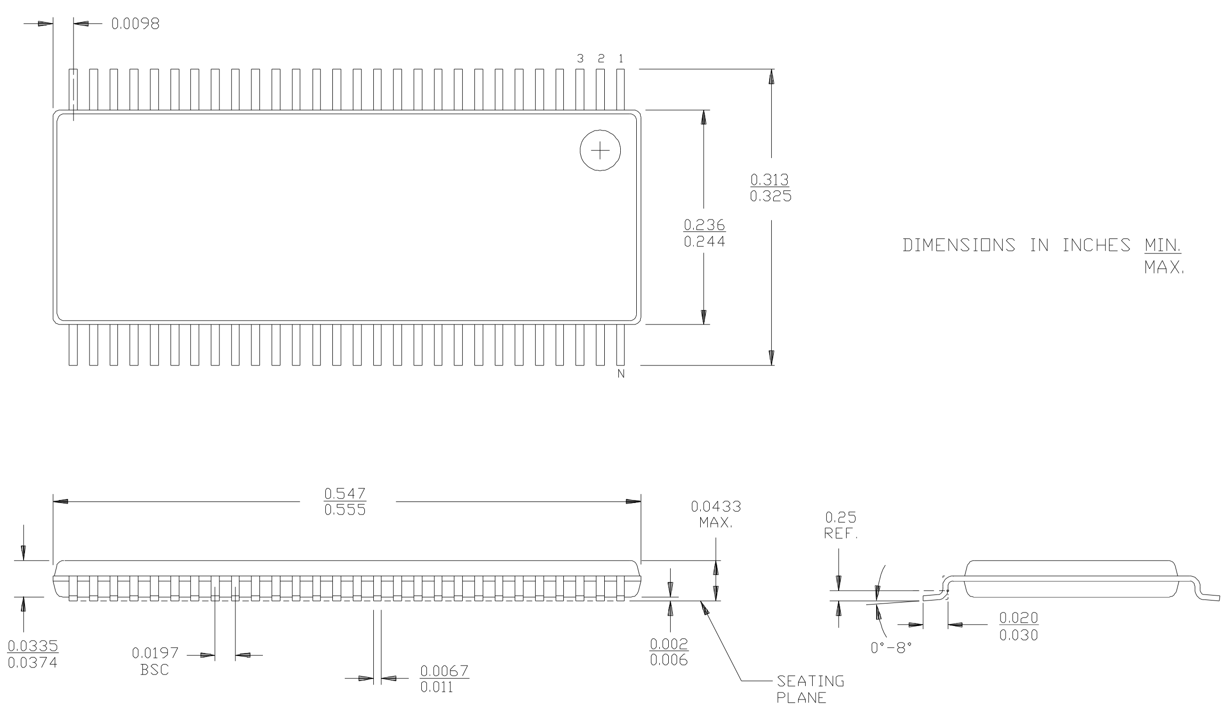
Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



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