128K x 8 Static RAM

Features

- 4.5V 5.5V operation
- CMOS for optimum speed/power
- Low active power (70 ns, LL version)
 - -330 mW (max.) (60 mA)
- Low standby power (70 ns, LL version)
 - 110 μW (max.) (20 μA)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE₁, CE₂, and OE options

Functional Description

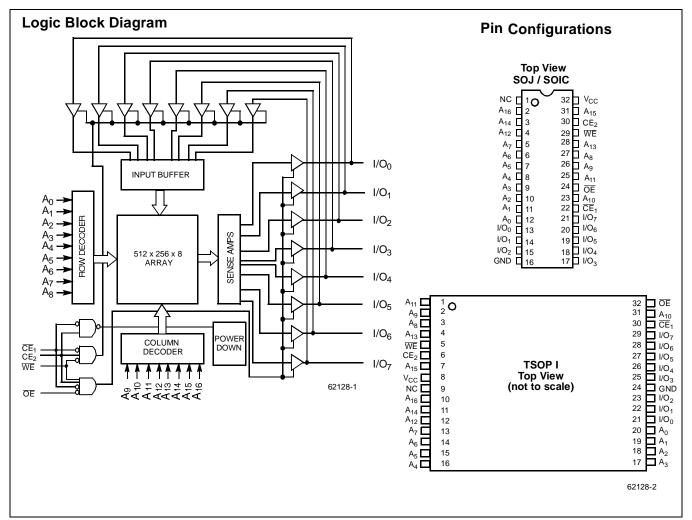
The CY62128 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), an active LOW output enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75%

Writing to the device is accomplished by taking chip enable one (\overline{CE}_1) and write enable (\overline{WE}) inputs LOW and chip enable two (CE₂) input HIGH. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins $(A_0 \text{ through } A_{16})$.

Reading from the device is accomplished by taking chip enable one $(\overline{\text{CE}}_1)$ and output enable $(\overline{\text{OE}})$ LOW while forcing write enable $(\overline{\text{WE}})$ and chip enable two $(\overline{\text{CE}}_2)$ HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (CE1 HIGH or CE₂ LOW), the outputs are disabled (OE HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

The CY62128 is available in a standard 400-mil-wide SOJ, 525-mil wide (450-mil-wide body width) SOIC and 32-pin TSOP type I.





Selection Guide

			CY62128-55	CY62128-70
Maximum Access Time (ns)			55	70
Maximum Operating Current	Commercial		115 mA	110 mA
		L	70 mA	60 mA
		LL	70 mA	60 mA
Maximum CMOS Standby Current	Commercial		10 mA	10 mA
		L	100 μΑ	100 μΑ
		LL	20 μΑ	20 μΑ

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.) Storage Temperature-65°C to +150°C Ambient Temperature with Power Applied......–55°C to +125°C Supply Voltage on V_{CC} to Relative $GND^{[1]}$ -0.5V to +7.0VDC Voltage Applied to Outputs in High Z State $^{[1]}$ -0.5V to V CC +0.5V DC Input Voltage^[1].....-0.5V to V_{CC} +0.5V

Current into Outputs (LOW)	20 mA
Static Discharge Voltage(per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature ^[2]	v _{cc}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

					6212	28–55	6212	28–70	
Parameter	Description	Test Conditions				Max.	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	$V_{CC} = Min., I_{OH} = -1.0 \text{ mA}$			2.4		2.4		V
V _{OL}	Output LOW Voltage	$V_{CC} = Min., I_{OL} = 2.1mA$				0.4		0.4	V
V _{IH}	Input HIGH Voltage	00 01				V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage[1]				-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$			-1	+1	-1	+1	μΑ
I _{OZ}	Output Leakage Current	$GND \le V_1 \le V_{CC}$, Output Dis	sabled		-5	+5	-5	+5	μΑ
Ios	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND				-300		-300	mA
I _{CC}	V _{CC} Operating	$V_{CC} = Max.$ $I_{OUT} = 0 \text{ mÅ},$ $f = f_{MAX} = 1/t_{RC}$	Com'l			115 11	110	mA	
	Supply Current			L	70		60	mA	
				LL		70		60	mA
I _{SB1}	Automatic CE	Max. V_{CC} , $\overline{CE}_1 \ge V_{IH}$	Com'l			25		25	mA
	Power-Down Current —TTL Inputs	or $CE_2 \le V_{IL}$, $V_{IN} \ge V_{IH}$ or		L		10		10	mA
		$V_{IN} \le V_{IL}$, $f = f_{MAX}$		LL		2		2	mA
I _{SB2}	Automatic CE	Max. V _{CC} ,	Com'l			10		10	mA
	Power-Down Current —CMOS Inputs	$\overline{CE}_1 \ge \overline{V}_{CC} - 0.3V$, or $CE_2 \le 0.3V$,		L		100		100	μΑ
	— CiviO3 inputs	$V_{IN} \ge V_{CC} - 0.3V$, or $V_{IN} \le 0.3V$, f=0		LL		20		20	μΑ

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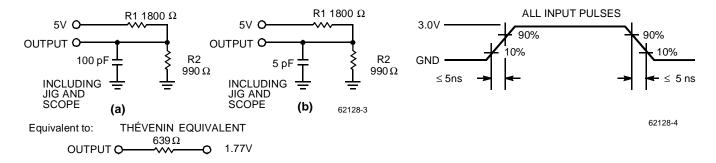
- $V_{\rm IL}$ (min.) = -2.0V for pulse durations of less than 20 ns. $T_{\rm A}$ is the "instant on" case temperature. See the last page of this specification for Group A subgroup testing information. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.



Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	$T_A = 25^{\circ}C, f = 1 \text{ MHz},$	9	pF
C _{OUT}	Output Capacitance	$V_{CC} = 5.0V$	9	pF

AC Test Loads and Waveforms



Switching Characteristics [3,6] Over the Operating Range

			28-55	6212	62128–70	
Parameter	Description	Min.	Max.	Min.	Max.	Unit
READ CYCLE		•	•	•	•	•
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		5		ns
t _{ACE}	CE ₁ LOW to Data Valid, CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	OE LOW to Data Valid		20		35	ns
t _{LZOE}	OE LOW to Low Z	0		0		ns
t _{HZOE}	OE HIGH to High Z ^[7, 8]		20		25	ns
t _{LZCE}	$\overline{\text{CE}}_1$ LOW to Low Z, CE_2 HIGH to Low Z ^[8]	5		5		ns
t _{HZCE}	$\overline{\text{CE}}_1$ HIGH to High Z, CE ₂ LOW to High Z ^[7, 8]		20		25	ns
t _{PU}	CE₁ LOW to Power-Up, CE₂ HIGH to Power-Up	0		0		ns
t _{PD}	CE₁ HIGH to Power-Down, CE₂ LOW to Power-Down		55		70	ns
WRITE CYCLE	<u>-</u> [9]	•	•	•	•	•
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	CE₁ LOW to Write End, CE₂ HIGH to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	WE Pulse Width	45		50		ns
t _{SD}	Data Set-Up to Write End	45		55		ns

Shaded areas contain advance information

Notes:

- Tested initially and after any design or process changes that may affect these parameters.

 Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified 5. 6. I_{OL}/I_{OH} and 100pF load capacitance.
- 7. $t_{HZOE}, t_{HZCE}, \text{and } t_{HZWE} \text{ are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured <math>\pm 500 \, \text{mV}$ from steady-state voltage.}

At any given temperature and voltage condition, t_{HZCE} is less than t_{LZOE} , t_{HZOE} is less than t_{LZOE} , and t_{HZNE} is less than t_{LZNE} for any given device. The internal write time of the memory is defined by the overlap of \overline{CE}_1 LUW, \overline{CE}_2 HIGH, and \overline{WE} LOW. \overline{CE}_1 and \overline{WE} must be LOW and \overline{CE}_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates



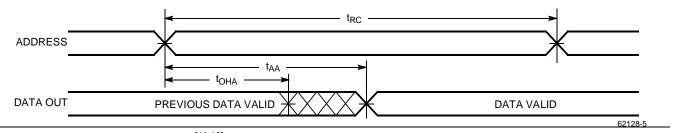
Switching Characteristics^[3,6] Over the Operating Range (continued)

		62128–55		6212		
Parameter	Description	Min.	Max.	Min.	Max.	Unit
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	WE HIGH to Low Z ^[8]	5		5		ns
t _{HZWE}	WE LOW to High Z ^[7,8]		20		25	ns

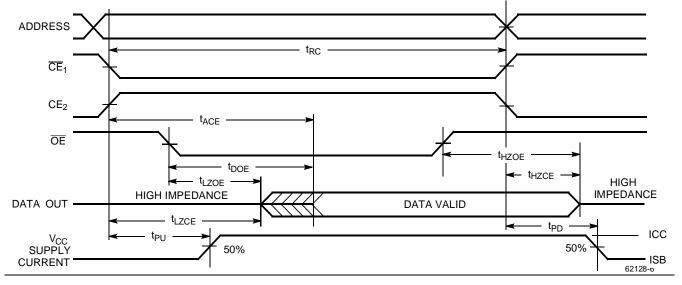
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Switching Waveforms

Read Cycle No.1^[10,11]



Read Cycle No. 2 (OE Controlled)[11,12]



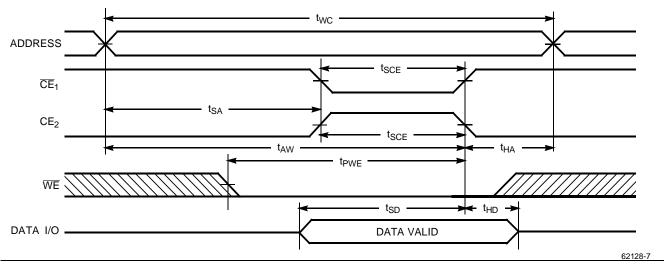
Notes:

- Device is continuously selected. OE, CE₁ = V_{IL}, CE₂ = V_{IH}.
 WE is HIGH for read cycle.
 Address valid prior to or coincident with CE₁ transition LOW and CE₂ transition HIGH.

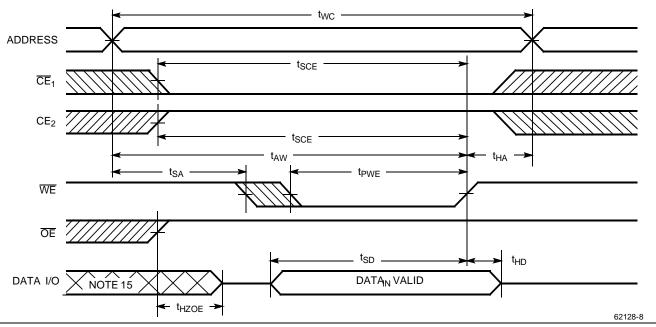


Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}_1$ or CE_2 Controlled) $^{[13,14]}$



Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write) $^{[13,14]}$

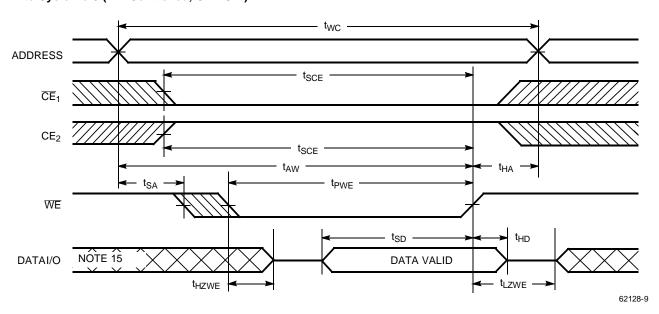


- 13. Data I/O is high impedance if OE = V_{IH}.
 14. If CE₁ goes HIGH or CE₂ goes LOW simultaneously with WE going HIGH, the output remains in a high-impedance state.
 15. During this period the I/Os are in the output state and input signals should not be applied.



Switching Waveforms (continued)

Write Cycle No.3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[13,14]



Truth Table

CE ₁	CE ₂	ΟE	WE	I/O ₀ – I/O ₇	Mode	Power
Н	Х	Х	Х	High Z	Power-Down	Standby (I _{SB})
Х	L	Х	Х	High Z	Power-Down	Standby (I _{SB})
L	Н	L	Н	Data Out	Read	Active (I _{CC})
L	Н	Х	L	Data In	Write	Active (I _{CC})
L	Н	Н	Н	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128-55VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY62128-55SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128-55ZC	Z32	32-Lead TSOP Typel	
70	CY62128-70VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY62128-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128-70ZC	Z32	32-Lead TSOP Type I	
	CY62128L-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128L-70ZC	Z32	32-Lead TSOP Type I	
	CY62128LL-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128LL-70ZC	Z32	32-Lead TSOP Type I	

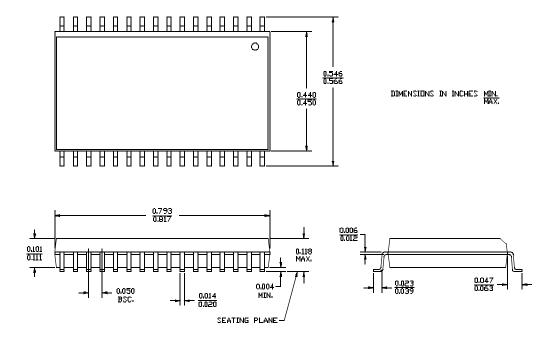
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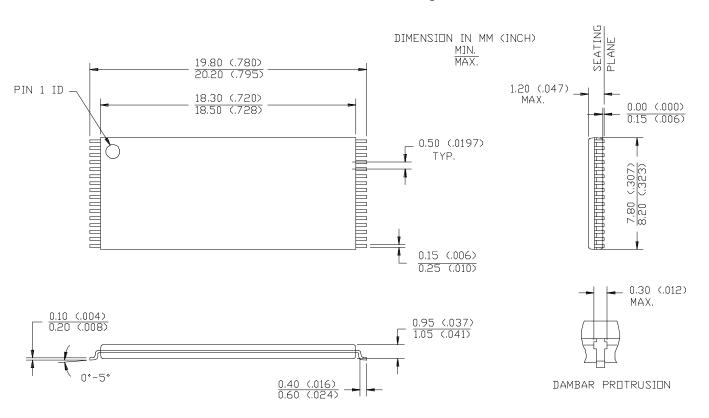


Package Diagrams

32-Lead (450 Mil) Molded SOIC S34



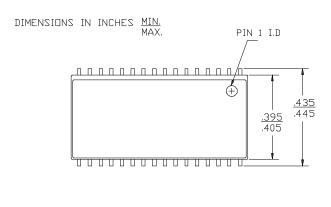
32-Lead Thin Small Outline Package Z32

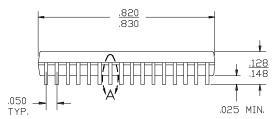


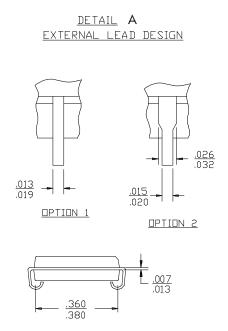


Package Diagrams (continued)

32-Lead (400-Mil) Molded SOJ V33







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