CY2305, CY2309

Low Cost 3.3-V Zero Delay Buffer

Features

- Not recommended for new designs. The CY2305C and CY2309C are form, fit, function compatible devices with improved specifications.
- 10 MHz to 100/133 MHz operating range, compatible with CPU and PCI bus frequencies
- Zero input-output propagation delay
- 60-ps typical cycle-to-cycle jitter (high drive)
- Multiple low skew outputs
  - 85 ps typical output-to-output skew
  - One input drives five outputs (CY2305)
  - One input drives nine outputs, grouped as 4 + 4 + 1 (CY2309)
- Compatible with Pentium-based systems
- Test Mode to bypass phase-locked loop (PLL) (CY2309)
- Packages:
  - 8-pin, 150-mil SOIC package (CY2305)
  - 16-pin 150-mil SOIC or 4.4-mm TSSOP (CY2309)
- 3.3-V operation
- Commercial and industrial temperature ranges

Functional Description

The CY2309 is a low-cost 3.3-V zero delay buffer designed to distribute high speed clocks and is available in a 16-pin SOIC or TSSOP package. The CY2305 is an 8-pin version of the CY2309. It accepts one reference input, and drives out five low skew clocks. The -1H versions of each device operate at up to 100-/133 MHz frequencies, and have higher drive than the -1 devices. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

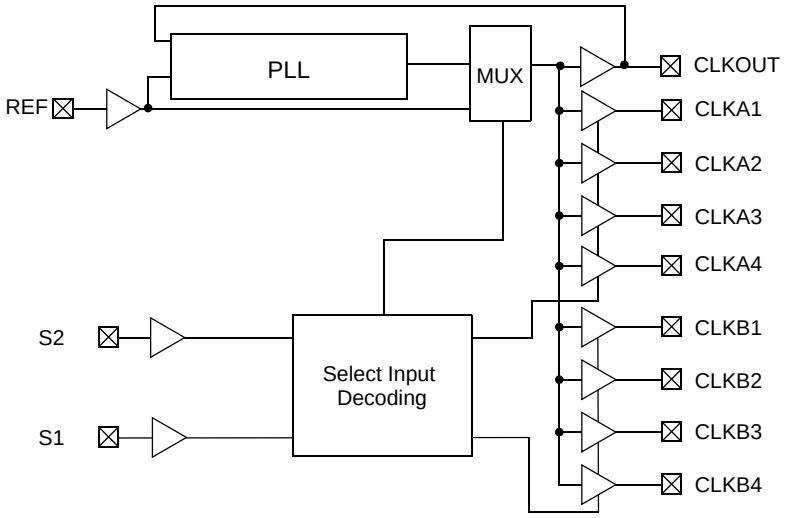
The CY2309 has two banks of four outputs each, which can be controlled by the select inputs as shown in "Select Input Decoding for CY2309" on page 4. If all output clocks are not required, BankB can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The CY2305 and CY2309 PLLs enter a power-down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 25.0 µA current draw for these parts. The CY2309 PLL shuts down in one additional case as shown in "Select Input Decoding for CY2309" on page 4.

Multiple CY2305 and CY2309 devices can accept the same input clock and distribute it. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

The CY2305/CY2309 is available in two or three different configurations, as shown in "Ordering Information for CY2305" on page 13. The CY2305-1/CY2309-1 is the base part. The CY2305-1H/ CY2309-1H is the high-drive version of the -1, and its rise and fall times are much faster than the -1.

Logic Block Diagram



Contents

Pinouts

Figure 1. Pin Diagram - CY2305

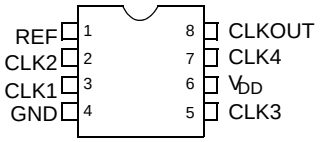


Table 1. Pin Description for CY2305

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5-V tolerant input
2	CLK2[2]	Buffered clock output
3	CLK1[2]	Buffered clock output
4	GND	Ground
5	CLK3[2]	Buffered clock output
6	V_{DD}	3.3-V supply
7	CLK4[2]	Buffered clock output
8	CLKOUT[2]	Buffered clock output, internal feedback on this pin

Figure 2. Pin Diagram - CY2309

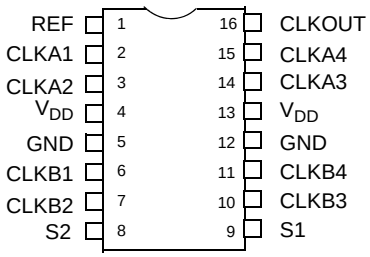


Table 2. Pin Description for CY2309

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5-V tolerant input
2	CLKA1[2]	Buffered clock output, Bank A
3	CLKA2[2]	Buffered clock output, Bank A
4	V_{DD}	3.3-V supply
5	GND	Ground
6	CLKB1[2]	Buffered clock output, Bank B
7	CLKB2[2]	Buffered clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	CLKB3[2]	Buffered clock output, Bank B
11	CLKB4[2]	Buffered clock output, Bank B
12	GND	Ground

Notes
1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.

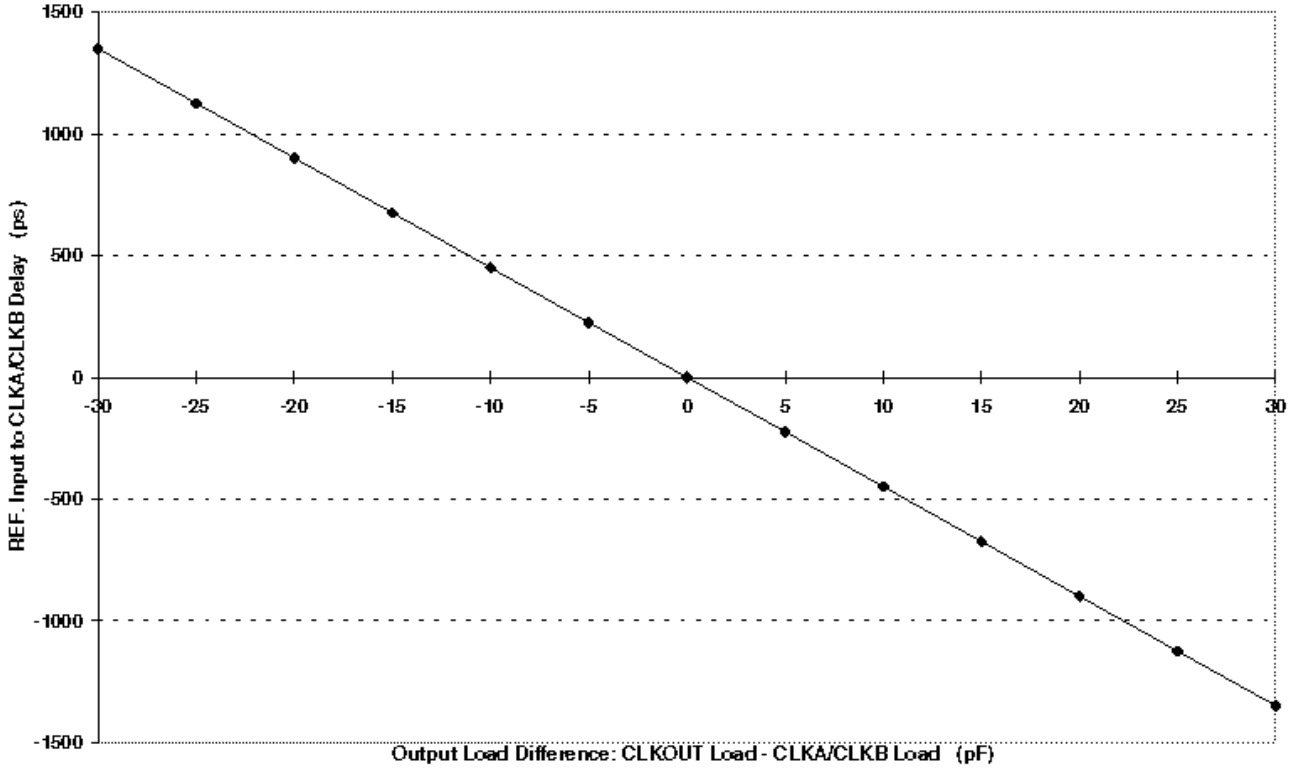
Table 2. Pin Description for CY2309

Pin	Signal	Description
13	V_{DD}	3.3-V supply
14	CLKA3[4]	Buffered clock output, Bank A
15	CLKA4[4]	Buffered clock output, Bank A
16	CLKOUT[4]	Buffered output, internal feedback on this pin

Select Input Decoding for CY2309

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT[5]	Output Source	PLL Shutdown
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Figure 3. REF. Input to CLKA/CLKB Delay vs. Loading Difference between CLKOUT and CLKA/CLKB Pins



Zero Delay and Skew Control

All outputs must be uniformly loaded to achieve zero delay between the input and output. Because the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay. If input to output delay adjustments are required, use Figure 3 to calculate loading differences between the CLKOUT pin and other outputs.

For zero output-output skew, be sure to load all outputs equally. For further information, refer to the application note titled "CY2305 and CY2309 as PCI and SDRAM Buffers."

Notes
4. Weak pull down on all outputs
5. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Absolute Maximum Conditions

Supply voltage to ground potential .....–0.5 V to +7.0 V
DC input voltage (Except REF) .....–0.5 V to V_{DD} + 0.5 V
DC input voltage REF.....–0.5 V to 7 V
Storage temperature ..... –65°C to +150°C
Junction temperature..... 150°C
Static discharge voltage
(per MIL-STD-883, Method 3015) .....> 2,000 V

Operating Conditions for CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	0	70	°C
C_L	Load capacitance, below 100 MHz	–	30	pF
C_L	Load capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage[6]		–	0.8	V
V_{IH}	Input HIGH voltage[6]		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50.0	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	100.0	µA
V_{OL}	Output LOW voltage[7]	I_{OL} = 8 mA (–1) I_{OH} = 12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH voltage[7]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power-down supply current	REF = 0 MHz	–	12.0	µA
I_{DD}	Supply current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{SS}	–	32.0	mA

Switching Characteristics for CY2305SC-1 and CY2309SC-1 Commercial Temperature Devices

Parameter[9]	Name	Test Conditions	Min	Typ.	Max	Unit
t1	Output frequency	30-pF load 10-pF load	10 10	–	100 133.33	MHz MHz
t_{DC}	Duty cycle[7] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise time[7]	Measured between 0.8 V and 2.0 V	–	–	2.50	ns
t_4	Fall time[7]	Measured between 0.8 V and 2.0 V	–	–	2.50	ns
t_5	Output-to-output skew[7]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge[7]	Measured at V_{DD}/2	–	0	±350	ps

Notes
6. REF input has a threshold voltage of V_{DD}/2.
7. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics for CY2305SC-1 and CY2309SC-1 Commercial Temperature Devices

Parameter[9]	Name	Test Conditions	Min	Typ.	Max	Unit
t_{6B}	Delay, REF rising edge to CLKOUT rising edge[8]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device-to-device skew[8]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_J	Cycle-to-cycle jitter[8]	Measured at 66.67 MHz, loaded outputs	–	70	200	ps
t_{LOCK}	PLL lock time[8]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Switching Characteristics for CY2305SC-1H and CY2309SC-1H Commercial Temperature Devices

Parameter[9]	Name	Description	Min	Typ.	Max	Unit
t_1	Output frequency	30 pF load 10 pF load	10 10	–	100 133.33	MHz MHz
t_{DC}	Duty cycle[8] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t_{DC}	Duty cycle[8] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} < 50 MHz	45.0	50.0	55.0	%
t_3	Rise time[8]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_4	Fall time[8]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_5	Output-to-output skew[8]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge[8]	Measured at $V_{DD}/2$	–	–	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge[8]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device-to-device skew[8]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_8	Output slew rate[8]	Measured between 0.8 V and 2.0 V using Test Circuit #2	1	–		V/ns
t_J	Cycle-to-cycle jitter[8]	Measured at 66.67 MHz, loaded outputs	–	60	200	ps
t_{LOCK}	PLL lock time[8]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Operating Conditions for CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	–40	85	°C
C_L	Load capacitance, below 100 MHz	–	30	pF
C_L	Load capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input capacitance	–	7	pF

Notes
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.
9. All parameters specified with loaded outputs.

Electrical Characteristics for CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage[10]		–	0.8	V
V_{IH}	Input HIGH voltage[10]		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50.0	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	100.0	µA
V_{OL}	Output LOW voltage[11]	I_{OL} = 8 mA (–1) I_{OH} =12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH voltage[11]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power-down supply current	REF = 0 MHz	–	25.0	µA
I_{DD}	Supply current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{SS}	–	35.0	mA

Switching Characteristics for CY2305SI-1 and CY2309SI-1 Industrial Temperature Devices

Parameter[12]	Name	Test Conditions	Min	Typ	Max	Unit
t1	Output frequency	30 pF load 10 pF load	10 10	–	100 133.33	MHz MHz
t_{DC}	Duty cycle[11] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise time[11]	Measured between 0.8 V and 2.0 V	–	–	2.50	ns
t_4	Fall time[11]	Measured between 0.8 V and 2.0 V	–	–	2.50	ns
t_5	Output-to-output skew[11]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge[11]	Measured at V_{DD}/2	–	–	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge[11]	Measured at V_{DD}/2. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device-to-device skew[11]	Measured at V_{DD}/2 on the CLKOUT pins of devices	–	–	700	ps
t_J	Cycle-to-cycle jitter[11]	Measured at 66.67 MHz, loaded outputs	–	70	200	ps
t_{LOCK}	PLL lock time[11]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Notes
10. REF input has a threshold voltage of V_{DD}/2.
11. Parameter is guaranteed by design and characterization. Not 100% tested in production.
12. All parameters specified with loaded outputs

Switching Characteristics for CY2305SI-1H and CY2309SI-1H Industrial Temperature Devices

Parameter[13]	Name	Description	Min	Typ	Max	Unit
t_1	Output frequency	30 pF load 10 pF load	10 10	–	100 133.33	MHz MHz
t_{DC}	Duty cycle[14] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t_{DC}	Duty cycle[14] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} < 50 MHz	45.0	50.0	55.0	%
t_3	Rise time[14]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_4	Fall time[14]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_5	Output-to output skew[14]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge[14]	Measured at $V_{DD}/2$	–	–	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge[14]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device-to-device skew[14]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_8	Output slew rate[14]	Measured between 0.8 V and 2.0 V using Test Circuit #2	1	–	–	V/ns
t_J	Cycle-to-cycle jitter[14]	Measured at 66.67 MHz, loaded outputs	–	60	200	ps
t_{LOCK}	PLL lock time[14]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Switching Waveforms

Figure 4. Duty Cycle Timing

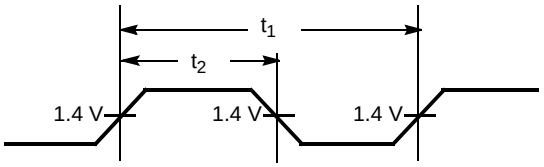


Figure 5. All Outputs Rise/Fall Time

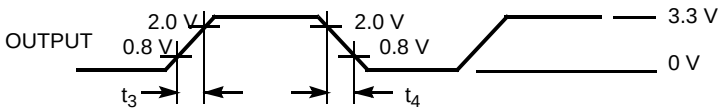
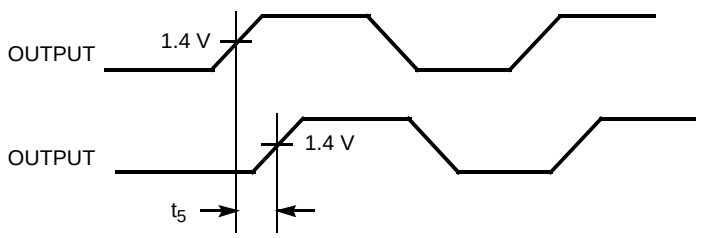


Figure 6. Output-Output Skew



Notes
13. All parameters specified with loaded outputs.
14. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

Figure 7. Input-Output Propagation Delay

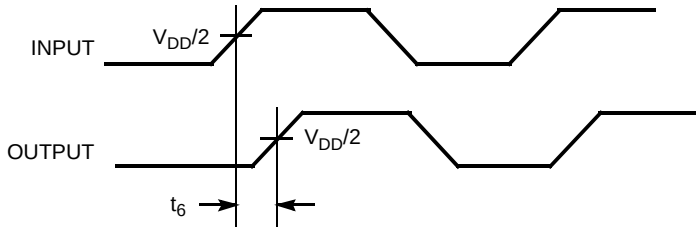
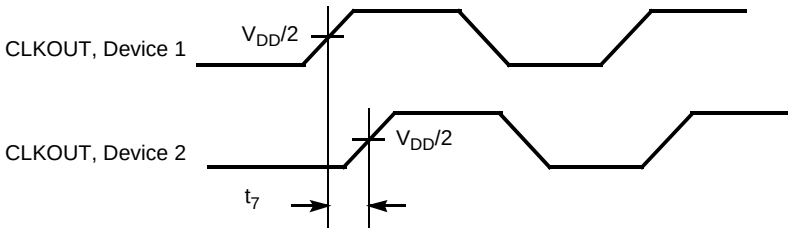
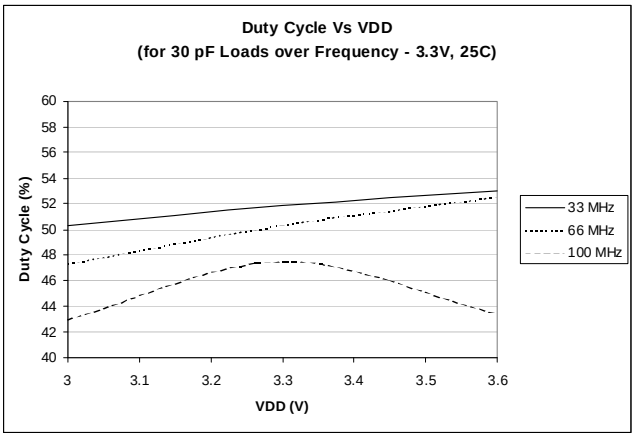
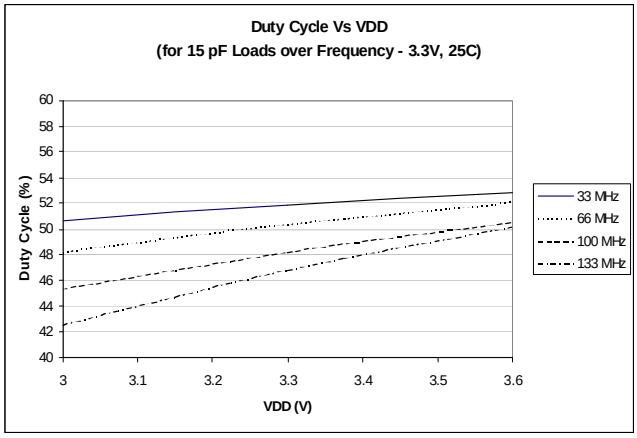


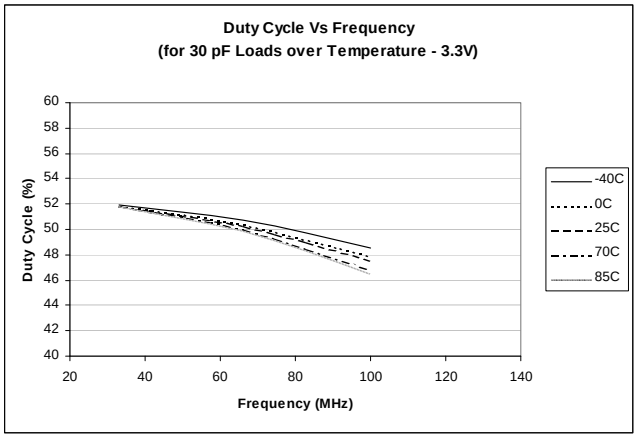
Figure 8. Device-Device Skew

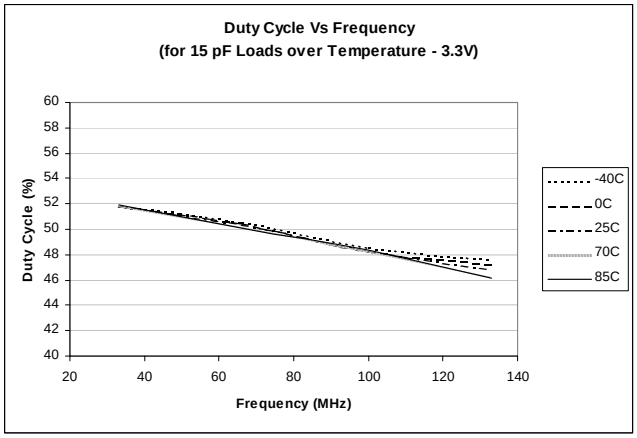


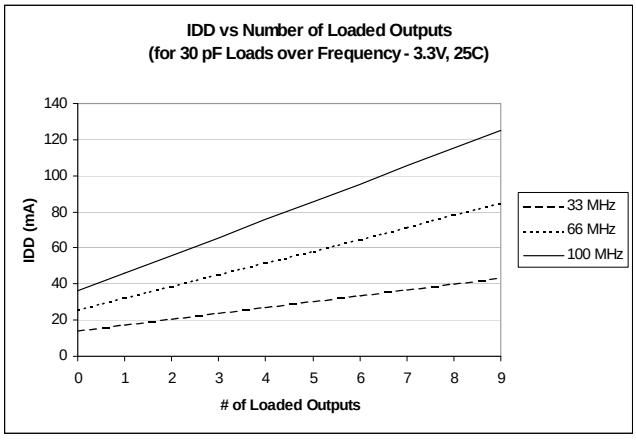
Typical Duty Cycle[15] and I_{DD} Trends[16] for CY2305-1 and CY2309-1

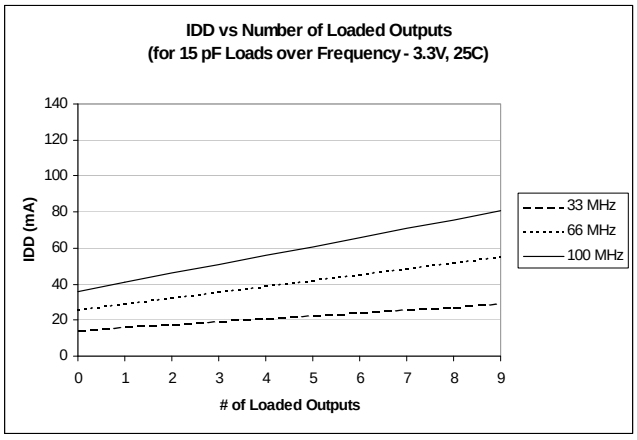








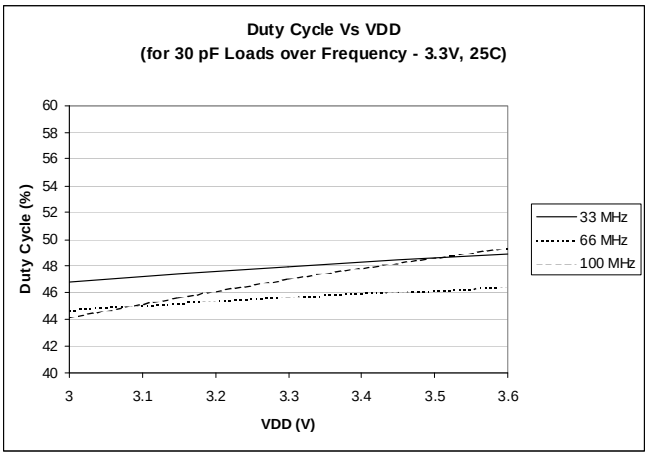


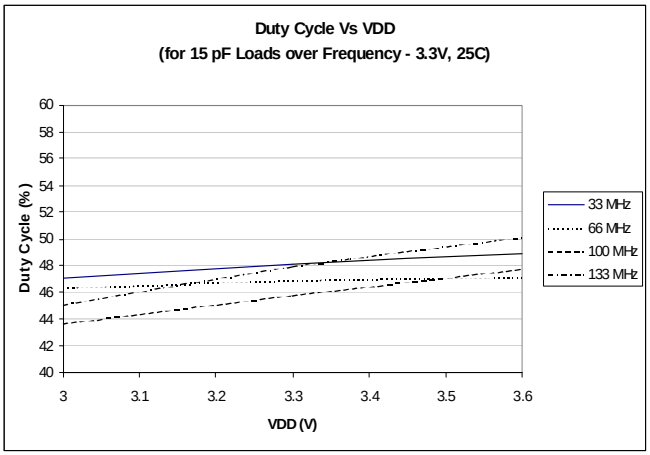


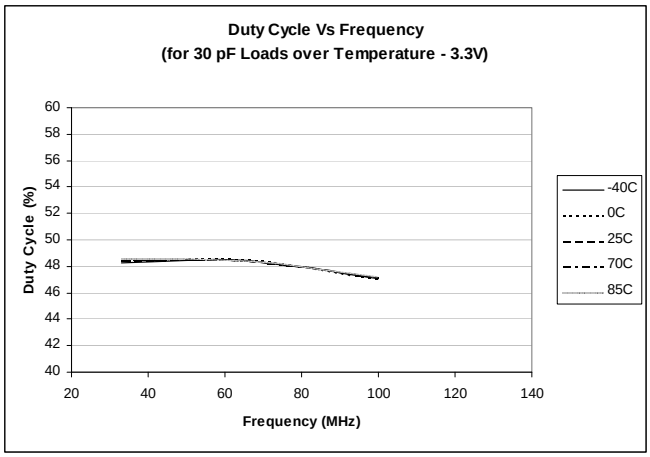
Notes

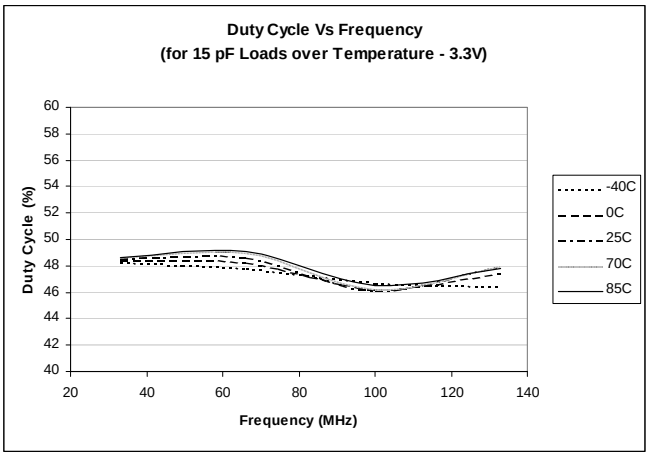
15. Duty cycle is taken from typical chip measured at 1.4 V.
16. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current. (n = # of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = frequency (Hz)).

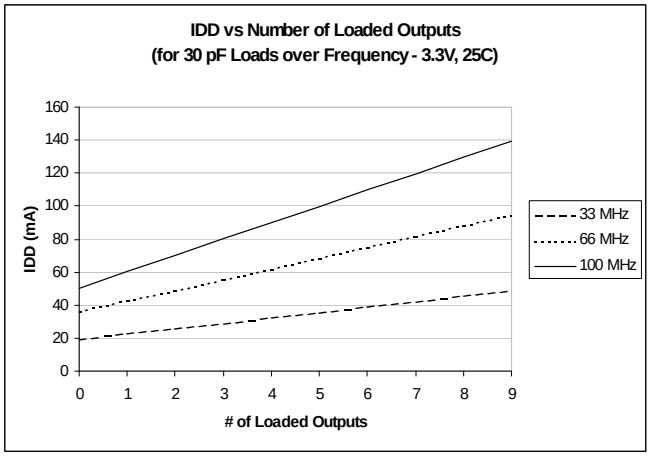
Typical Duty Cycle[17] and IDD Trends[18] for CY2305-1H and CY2309-1H

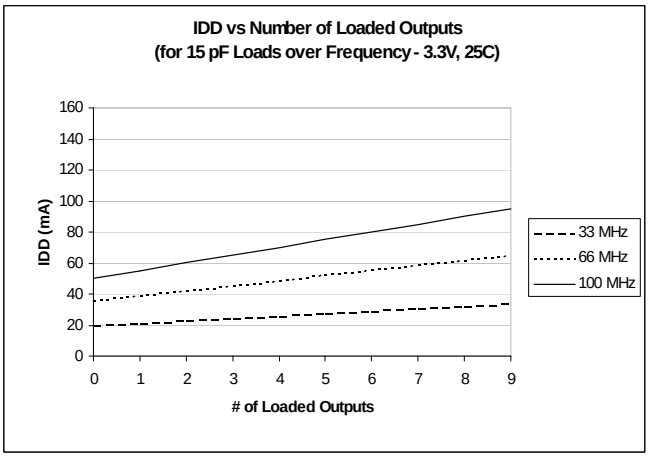










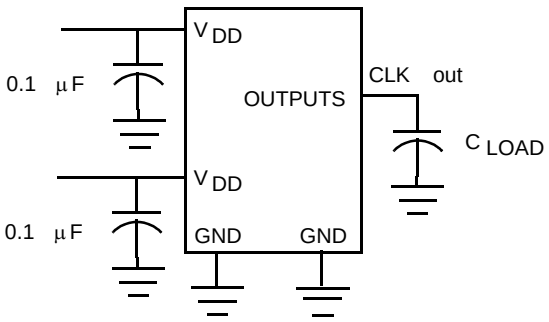


Notes

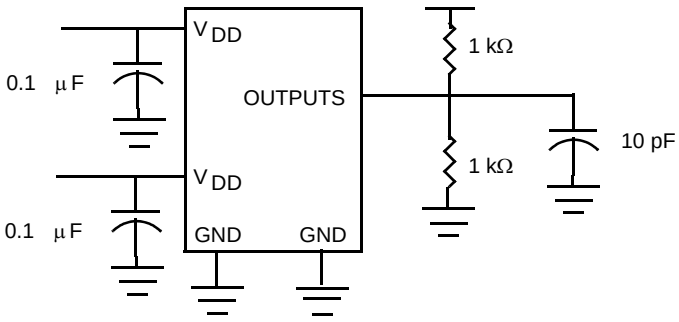
17. Duty cycle is taken from typical chip measured at 1.4 V.
18. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current. (n = # of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = frequency (Hz)).

Test Circuits

Test Circuit # 1



Test Circuit # 2



For parameter t_8 (output slew rate) on -1H devices

Ordering Information for CY2305

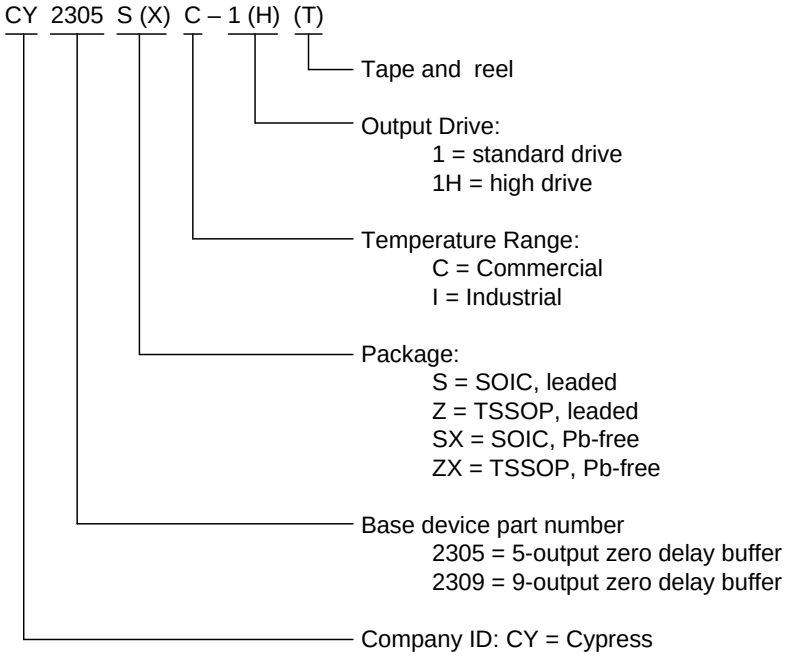
Ordering Code	Package Type	Operating Range
CY2305SC-1[19]	8-pin 150-mil SOIC	Commercial
CY2305SC-1T[19]	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY2305SC-1H[19]	8-pin 150-mil SOIC	Commercial
CY2305SC-1HT[19]	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY2305SI-1H[19]	8-pin 150-mil SOIC	Industrial
CY2305SI-1HT[19]	8-pin 150-mil SOIC – Tape and Reel	Industrial
Pb-free		
CY2305SXC-1[19]	8-pin 150-mil SOIC	Commercial
CY2305SXC-1T[19]	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY2305SXI-1[19]	8-pin 150-mil SOIC	Industrial
CY2305SXI-1T[19]	8-pin 150-mil SOIC – Tape and Reel	Industrial
CY2305SXC-1H[19]	8-pin 150-mil SOIC	Commercial
CY2305SXC-1HT[19]	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY2305SXI-1H[19]	8-pin 150-mil SOIC	Industrial
CY2305SXI-1HT[19]	8-pin 150-mil SOIC – Tape and Reel	Industrial

Ordering Information for CY2309

Ordering Code	Package Type	Operating Range
CY2309SC-1[19]	16-pin 150-mil SOIC	Commercial
CY2309SC-1T[19]	16-pin 150-mil SOIC – Tape and Reel	Commercial
CY2309SC-1H[19]	16-pin 150-mil SOIC	Commercial
CY2309SC-1HT[19]	16-pin 150-mil SOIC – Tape and Reel	Commercial
CY2309ZC-1H[19]	16-pin 4.4-mm TSSOP	Commercial
CY2309ZC-1HT[19]	16-pin 4.4-mm TSSOP – Tape and Reel	Commercial
Pb-free		
CY2309SXC-1[19]	16-pin 150-mil SOIC	Commercial
CY2309SXC-1T[19]	16-pin 150-mil SOIC – Tape and Reel	Commercial
CY2309SXI-1[19]	16-pin 150-mil SOIC	Industrial
CY2309SXI-1T[19]	16-pin 150-mil SOIC – Tape and Reel	Industrial
CY2309SXC-1H[19]	16-pin 150-mil SOIC	Commercial
CY2309SXC-1HT[19]	16-pin 150-mil SOIC – Tape and Reel	Commercial
CY2309SXI-1H[19]	16-pin 150-mil SOIC	Industrial
CY2309SXI-1HT[19]	16-pin 150-mil SOIC – Tape and Reel	Industrial
CY2309ZXC-1H[19]	16-pin 4.4-mm TSSOP	Commercial
CY2309ZXC-1HT[19]	16-pin 4.4-mm TSSOP – Tape and Reel	Commercial
CY2309ZXI-1H[19]	16-pin 4.4-mm TSSOP	Industrial
CY2309ZXI-1HT[19]	16-pin 4.4-mm TSSOP – Tape and Reel	Industrial

Note
19. Not recommended for new designs.

Ordering Code Definitions



Package Drawing and Dimensions

Figure 9. 8-Pin (150-Mil) SOIC S8

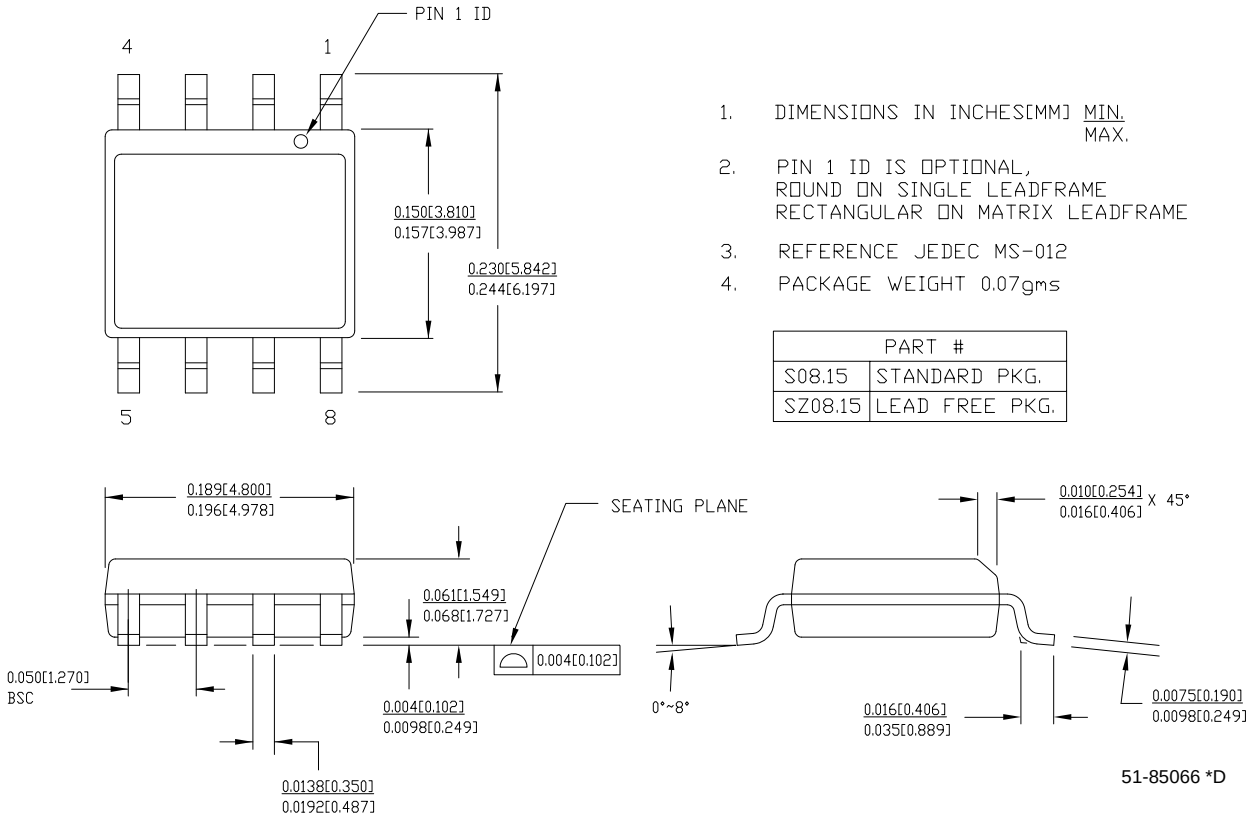


Figure 10. 16-Pin (150-Mil) SOIC S16

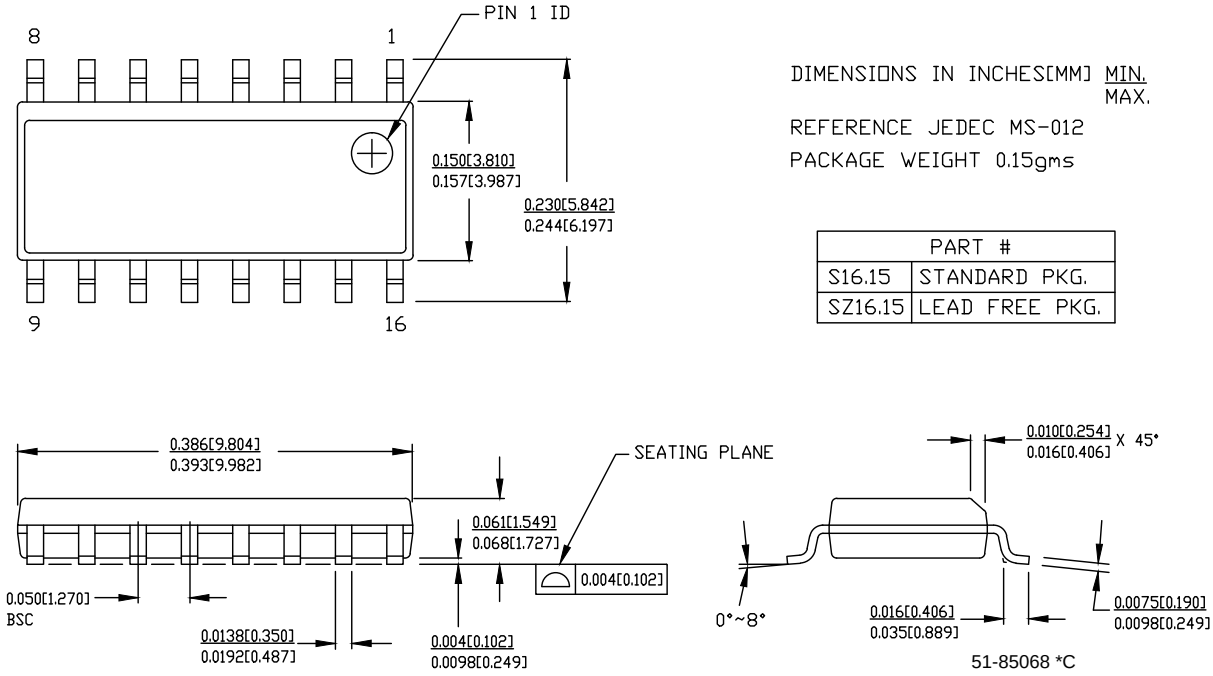
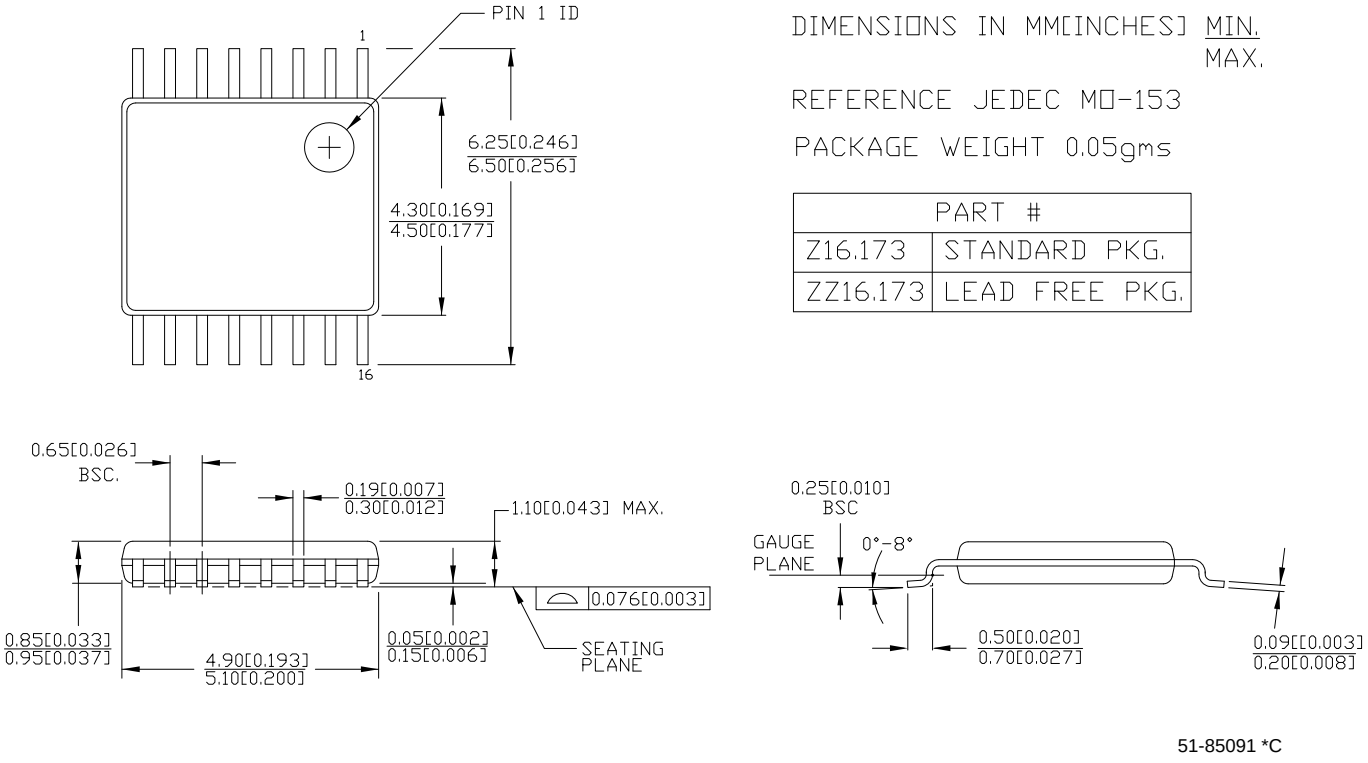


Figure 11. 16-Pin TSSOP 4.40 MM Body Z16.173



Acronyms

Acronym	Description
PCI	Personal computer interconnect
PLL	Phase locked loop
SDRAM	Synchronous dynamic random access memory
SOIC	Small outline integrated circuit
TSSOP	Thin small outline package
ZDB	Zero delay buffer

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	micro amperes
mA	milli amperes
ms	milli seconds
MHz	Mega Hertz
ns	nano seconds
pF	pico Farad
ps	pico seconds
V	Volts

Document History Page

Document Title: CY2305/CY2309 Low Cost 3.3-V Zero Delay Buffer Document Number: 38-07140				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110249	SZV	10/19/01	Change from Spec number: 38-00530 to 38-07140
*A	111117	CKN	03/01/02	Added t6B row to the Switching Characteristics Table; also added the letter “A” to the t6A row Corrected the table title from CY2305SC-IH and CY2309SC-IH to CY2305SI-IH and CY2309SI-IH
*B	117625	HWT	10/21/02	Added eight-pin TSSOP packages (CY2305ZC-1 and CY2305ZC-1T) to the ordering information table. Added the Tape and Reel option to all the existing packages: CY2305SC-1T, CY2305SI-1T, CY2305SC-1HT, CY2305SI-1HT, CY2305ZC-1T, CY2309SC-1T, CY2309SI-1T, CY2309SC-1HT, CY2309SI-1HT, CY2309ZC-1HT, CY2309ZI-1HT
*C	121828	RBI	12/14/02	Power up requirements added to Operating Conditions information
*D	131503	RGL	12/12/03	Added Lead-free for all the devices in the ordering information table
*E	214083	RGL	See ECN	Added a Lead-free with the new coding for all SOIC devices in the ordering information table
*F	291099	RGL	See ECN	Added TSSOP Lead-free devices
*G	390582	RGL	See ECN	Added typical values for jitter
*H	2542461	AESA	07/23/08	Updated template. Added Note “Not recommended for new designs.” Added part number CY2305ESXC-1, CY2305ESXC-1T, CY2305ESXI-1, CY2305ESXI-1T, CY2305ESXC-1H, CY2305ESXC-1HT, CY2305ESXI-1H, CY2305ESXI-1HT, CY2309ESXC-1, CY2309ESXC-1T, CY2309ESXI-1, CY2309ESXI-1T, CY2309ESXC-1H, CY2309ESXC-1HT, CY2309ESXI-1H, CY2309ESXI-1HT, CY2309EZXC-1H, CY2309EZXC-1HT, CY2309EZXI-1H, and CY2309EZXI-1HT in ordering information table. Removed part number CY2305SZC-1, CY2305SZC-1T, CY2305SZI-1, CY2305SZI-1T, CY2305SZC-1H, CY2305SZC-1HT, CY2305SZI-1H, CY2305SZI-1HT, CY2309SZC-1, CY2309SZC-1T, CY2309SZI-1, CY2309SZI-1T, CY2309SZC-1H, CY2309SZC-1HT, CY2309SZI-1H, CY2309SZI-1HT, CY2309ZZC-1H, CY2309ZZC-1HT, CY2309ZI-1H, CY2309ZI-1HT, CY2309ZZI-1H, and CY2309ZZI-1HT in Ordering Information table. Changed Lead-Free to Pb-Free.
*I	2565153	AESA	09/18/08	Removed part number CY2305ESXC-1, CY2305ESXC-1T, CY2305ESXI-1, CY2305ESXI-1T, CY2305ESXC-1H, CY2305ESXC-1HT, CY2305ESXI-1H, CY2305ESXI-1HT, CY2309ESXC-1, CY2309ESXC-1T, CY2309ESXI-1, CY2309ESXI-1T, CY2309ESXC-1H, CY2309ESXC-1HT, CY2309ESXI-1H, CY2309ESXI-1HT, CY2309EZXC-1H, CY2309EZXC-1HT, CY2309EZXI-1H, and CY2309EZXI-1HT in ordering information table. Removed note references to note 10 in Pb-Free sections of ordering information table. Changed IDD (PD mode) from 12.0 to 25.0 μA for commercial temperature devices Deleted Duty Cycle parameters for F_{out} < 50 MHz commercial and industrial devices.
*J	2673353	KVM/PYRS	03/13/09	Reverted IDD (PD mode) and Duty Cycle parameters back to the values in revision *H: Changed IDD (PD mode) from 25 to 12 μA for commercial devices. Added Duty Cycle parameters for F_{out} < 50 MHz for commercial and industrial devices.

Document Title: CY2305/CY2309 Low Cost 3.3-V Zero Delay Buffer Document Number: 38-07140				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*K	2904641	KVM	04/05/10	Removed parts CY2305SI-1,CY2305SI-1T,CY2309SI-1,CY2309SI-1H,CY2309SI-1HT,CY2309SI-1T from Ordering Information. Updated Package Diagram
*L	3047136	KVM	10/04/2010	Added table of contents, ordering code definition, Acronyms and Units tables. Updated 16-pin TSSOP package diagram.
*M	3146330	CXQ	01/18/2011	Added “Not recommended for new designs” statement to Features on page 1. Added ‘not recommended for new designs’ footnote to all parts in the ordering information table.

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