**CY22313**

# Two-PLL Clock Generator with Direct Rambus™ (Lite) Support

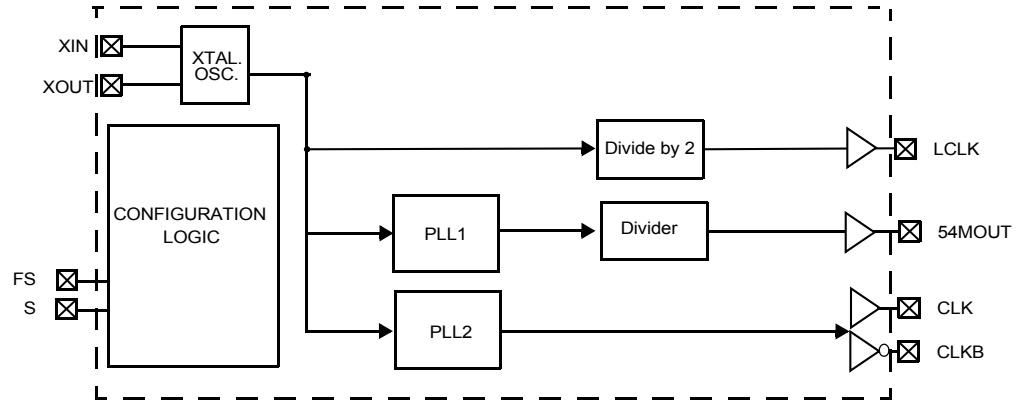
## Features

- Two integrated phase-locked loops (PLLs)
- Ultra-accurate PLLs
- Direct Rambus™ clock support
- Two input selects
- 3.45V core; 3.45V, 2.5V, 1.8V, and 1.675V outputs
- 24-pin TSSOP package

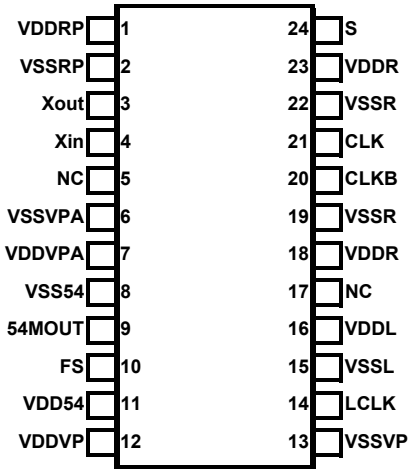
## Benefits

- High-performance PLL tailored for multimedia applications
- Frequency tolerance within 1 PPM on all frequencies
- One pair of differential output drivers, identical specification to CY2212
- Selectable 54.0-/53.946-MHz output and 294.912-/393.216-MHz Rambus® output
- Supports output voltage requirements
- Industry-standard packaging saves on board space

## Block Diagram




## Pin Configuration




## Frequency Select Tables

| FS | 54MOUT | Unit | PPM |
|---|---|---|---|
| 0 | 54 | MHz | 0 |
| 1 | 53.94605395 | MHz | –1 |

| S | CLK, CLKB | Unit | PPM |
|---|---|---|---|
| 0 | 294.912 | MHz | 0 |
| 1 | 393.216 | MHz | 0 |

| LCLK | Unit | PPM |
|---|---|---|
| 9.216 | MHz | 0 |

## Pin Definitions

| Name | Pin Numbers | Pin Description |
|---|---|---|
| $V_{DDRP}$ | 1 | **Power for DRCG PLL** |
| $V_{SSRP}$ | 2 | **Ground for DRCG PLL** |
| $X_{out}$ | 3 | **Crystal Output** |
| $X_{in}$ | 4 | **Crystal Input** |
| NC | 5 | **Do Not Connect, Leave Floating** |
| $V_{SSVPA}$ | 6 | **Analog Ground For Video PLL** |
| $V_{DDVPA}$ | 7 | **Analog Power for Video PLL** |
| $V_{SS54}$ | 8 | **Ground for 54MOUT** |
| 54MOUT | 9 | **54-MHz/53.94605395-MHz Output** |
| FS | 10 | **Frequency Select Pin for 54MOUT** (internal pull-down resistor) |
| $V_{DD54}$ | 11 | **Power for 54MOUT** |
| $V_{DDVP}$ | 12 | **Power for Video PLL** |
| $V_{SSVP}$ | 13 | **Ground for Video PLL** |
| LCLK | 14 | **LCLK Output** |
| $V_{SSL}$ | 15 | **Ground for LCLK** |
| $V_{DDL}$ | 16 | **Power for LCLK** |
| NC | 17 | **Do Not Connect**, Leave Floating |
| $V_{DDR}$ | 18 | **Power for DRCG CLK/CLKB** |
| $V_{SSR}$ | 19 | **Ground for DRCG CLK/CLKB** |
| CLKB | 20 | **Output Clock to Rambus** (complement) |
| CLK | 21 | **Output Clock to Rambus** |
| $V_{SSR}$ | 22 | **Ground for DRCG CLK/CLKB** |
| $V_{DDR}$ | 23 | **Power for DRCG CLK/CLKB** |
| S | 24 | **Frequency Select Pin for DRCG CLK/CLKB** (internal pull-up resistor) |

## Absolute Maximum Conditions

(Above which the useful life may be impaired. For user guidelines; not tested.)

Supply Voltage ..... –0.5V to +4.0V

DC Input Voltage ..... –0.5V to + ($V_{DD}$ + 0.5V)

Storage Temperature ..... –65°C to +125°C

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... 2000V

Latch-up (per JEDEC 17) ..... ≥ ±200 mA

## Recommended Operating Conditions[1]

| Parameter | Description | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DDRP}$, $V_{DDVPA}$, $V_{DDVP}$, $V_{DDR}$ | Supply Voltage for PLL's, Crystal Oscillator, and 3.45V Outputs | 3.15 | 3.45 | 3.6 | V |
| $V_{DD54}$ (2.5V) | Supply Voltage for 2.5V Outputs | 2.25 | 2.5 | 2.75 | V |
| $V_{DD54}$ (1.675V) | Supply Voltage for 1.675V Outputs | 1.6 | 1.675 | 1.75 | V |
| $V_{DDL}$ | Supply Voltage for 1.8V Outputs | 1.6 | 1.8 | 2.0 | V |
| $t_{PU}$ | Power-up time for all $V_{DDS}$ to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | | 500 | ms |
| $T_A$ | Operating Temperature, Ambient | 0 | | +85 | °C |
| $C_{LOAD\_54MOUT}$ | Max. Load Capacitance, CMOS Output | | | 15 | pF |
| $f_{REF}$ | External Reference Crystal | | 18.432 | | MHz |

## Electrical Specifications

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{OH}$[2] | Output High Current, 2.5V outputs[3] | $V_{OH} = V_{DD} – 0.5$, $V_{DD}$ = 2.5V | 8 | 16 | | mA |
| | Output High Current, 1.8V outputs[3] | $V_{OH} = V_{DD} – 0.5$, $V_{DD}$ = 1.8V | 6 | 12 | | mA |
| | Output High Current, 1.675V outputs[3] | $V_{OH} = V_{DD} – 0.5$, $V_{DD}$ = 1.675V | 5 | 10 | | mA |
| $I_{OL}$[2] | Output Low Current, 2.5V outputs[3] | $V_{OL}$ = 0.5V, $V_{DD}$ = 2.5V | 8 | 16 | | mA |
| | Output Low Current, 1.8V outputs[3] | $V_{OL}$ = 0.5V, $V_{DD}$ = 1.8V | 6 | 12 | | mA |
| | Output Low Current, 1.675V outputs[3] | $V_{OL}$ = 0.5V, $V_{DD}$ = 1.675V | 5 | 10 | | mA |
| $C_{XTAL}$ | Crystal Load Capacitance[3] | Total effective load of internal load caps | | 11[4] | | pF |
| $C_{LOAD\_IN}$ | Input Pin Capacitance[3] | Except crystal pins | | 7 | | pF |
| $V_{IH}$ | HIGH-Level Input Voltage | CMOS levels,% of $V_{DDRP}/V_{DDVPA}/V_{DDVP}$ | 70% | | | $V_{DD}$ |
| $V_{IL}$ | LOW-Level Input Voltage | CMOS levels,% of $V_{DDRP}/V_{DDVPA}/V_{DDVP}$ | | | 30% | $V_{DD}$ |
| $R_{I\_FS}$ | FS Input Resistor | Pull-down resistor on FS | 60 | 150 | 225 | kΩ |
| $R_{I\_S}$ | S Input Resistor | Pull-up resistor on S | 10 | | 100 | kΩ |
| $I_{DD}$ | Total Power Supply Current | Sum of all supply currents | | | 125 | mA |

## Direct Rambus Electrical Specifications[3]

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CM}$ | Differential output common-mode voltage | 1.35 | | 1.75 | V |
| $V_X$ | Differential output crossing-point voltage[5] | 1.25 | | 1.85 | V |
| $V_{COS}$ | Output Voltage swing (p-p single-ended)[6] | 0.4 | | 0.7 | V |
| $V_{COH}$ | Output high voltage | | | 2.1 | V |
| $V_{COL}$ | Output low voltage | 1.0 | | | V |
| $r_{OUT}$ | Output dynamic resistance (at pins)[7] | 12 | | 50 | Ω |

**Notes:**

1. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
2. LCLK and 54MOUT outputs only.
3. Guaranteed by design, not 100% tested.
4. Identical Crystal Load Capacitance as CY2212ZC-2. Use the same crystal and $X_{IN}$ / $X_{OUT}$ board layout as implemented with the original crystal-driven CY2212ZC-2.
5. Differential output crossing point voltages shown in *Figure 1*.
6. $V_{COS} = V_{OH} – V_{OL}$.
7. $r_{OUT} = \Delta V_O / \Delta I_O$. This is defined at the output pins, not at the measurement point of *Figure 9*.

## Switching Characteristics[3]

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{PPM}$ | Frequency Error | Part to Part, does not include PCB variation[8] | | ±5 | ±10 | PPM |
| | | Over commercial temperature range[9] | | ±2 | ±5 | PPM |
| DC | Output Duty Cycle | Duty cycle for all outputs, measured at $V_{DD}/2$ | 45 | 50 | 55 | % |
| $t_{3\_54,\ 2.5}$ | 54MOUT Rising Edge Slew Rate | 20% to 80% of $V_{DD54}$, $V_{DD54}$ = 2.5V | 0.75 | 1.2 | 4.0 | V/ns |
| $t_{3\_54,\ 1.675}$ | 54MOUT Rising Edge Slew Rate | 20% to 80% of $V_{DD54}$, $V_{DD54}$ = 1.675V | 0.35 | 0.5 | 2.5 | V/ns |
| $t_{4\_54,\ 2.5}$ | 54MOUT Falling Edge Slew Rate | 80% to 20% of $V_{DD54}$, $V_{DD54}$ = 2.5V | 0.75 | 1.2 | 4.0 | V/ns |
| $t_{4\_54,\ 1.675}$ | 54MOUT Falling Edge Slew Rate | 80% to 20% of $V_{DD54}$, $V_{DD54}$ = 1.675V | 0.35 | 0.5 | 2.5 | V/ns |
| $t_{CR}$, $t_{CF}$ | CLK/CLKB Rise and Fall Times | 20% to 80% of output voltage | 160 | | 400 | ps |
| $t_{CR-CF}$ | CLK/CLKB Rise and Fall Difference[10] | 20% to 80% of output voltage | | | 100 | ps |
| $t_5$ | Lock Time[11] | PLL lock time from power-up | | 1.0 | 3.0 | ms |

## Phase Noise Specifications

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Phase Noise | 54 MHz at 10-kHz offset | | –95 | | dBc |
| | Phase Noise | 53.946 MHz at 10-kHz offset | | –92 | | dBc |

## Jitter Specifications[3]

| Parameter | Description | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{6\_LCLK}$ | LCLK Jitter[12] | Cycle-Cycle Jitter – 9.216 MHz | | 250 | ps |
| $t_{6\_54,\ 2.5}$ | 54MOUT Jitter[12] | Cycle-Cycle Jitter – 54 MHz, $V_{DD}$ = 2.5V | | 150 | ps |
| | | Cycle-Cycle Jitter – 53.946 MHz, $V_{DD}$ = 2.5V | | 150 | ps |
| $t_{6\_54,\ 1.675}$ | | Cycle-Cycle Jitter – 54 MHz, $V_{DD}$ = 1.675V | | 250 | ps |
| | | Cycle-Cycle Jitter – 53.946 MHz, $V_{DD}$ = 1.675V | | 250 | ps |
| $t_{7\_LCLK}$ | LCLK 1000 Cycle Jitter[13] | 1000 Cycle Jitter – 9.216 MHz | | 250 | ps |
| $t_{7\_54}$ | 54MOUT 1000 Cycle Jitter[13] | 1000 Cycle Jitter – 54 MHz, | | 400 | ps |
| | | 1000 Cycle Jitter – 53.946 MHz, | | 400 | ps |
| $t_8$ | CLK/CLKB 1–6 Cycle Jitter[14] | Cycle-Cycle Jitter, 1–6 Cycles, 400 MHz | | 50 | ps |
| | | Cycle-Cycle Jitter, 1–6 Cycles, 300 MHz | | 70 | ps |
| $t_9$ | CLK/CLKB Long-term Jitter[15] | Long-term Jitter, 400 MHz | | 300 | ps |
| | | Long-term Jitter, 300 MHz | | 400 | ps |
| $t_{10}$ | CLK/CLKB Duty Cycle Error[16] | Cycle-Cycle Duty Cycle Error, 400 MHz | | 50 | ps |
| | | Cycle-Cycle Duty Cycle Error, 300 MHz | | 70 | ps |

**Notes:**

8. Tested across three lots on same board, PCB boards can vary more than ± 5 PPM.
9. Crystal should not be heated for this test, only IC.
10. Measured on same pin of a single device.
11. Lock Time shown in *Figure 2*.
12. LCLK and 54MOUT Cycle-Cycle Jitter shown in *Figure 3*.
13. LCLK and 54MOUT 1000 Cycle Jitter shown in *Figure 4*.
14. CLK/CLKB 1-6 Cycle Jitter specification is absolute value of worst case deviation, and is shown in *Figure 5* and *Figure 6*.
15. CLK/CLKB Long Term Jitter shown in *Figure 7*.
16. CLK/CLKB Duty Cycle Error shown in *Figure 8*.

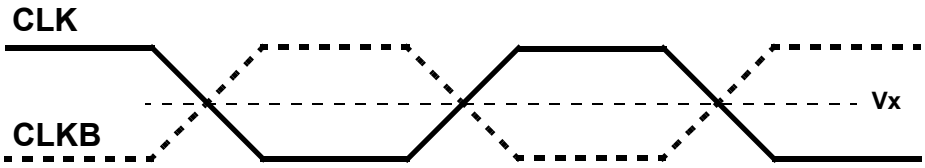



**Figure 1. Direct Rambus Crossing Point Voltage**

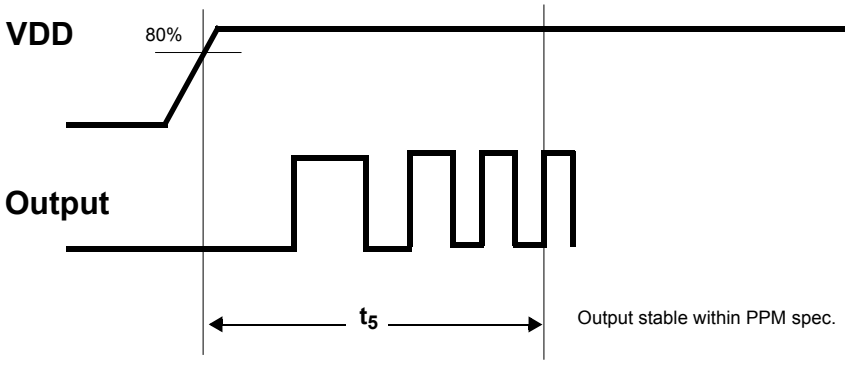
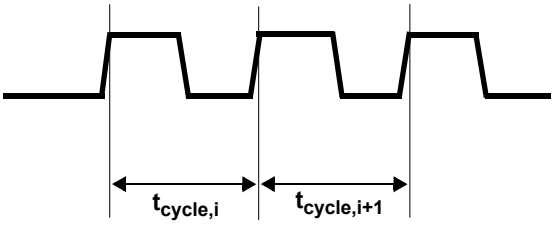
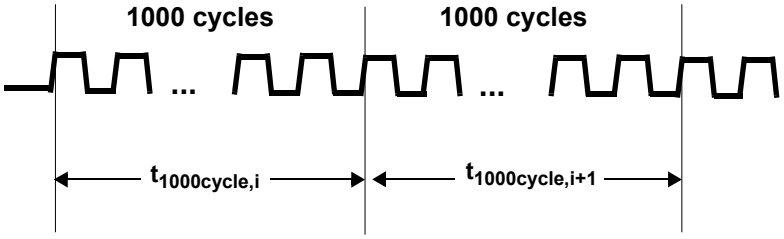



**Figure 2. PLL Lock Time**



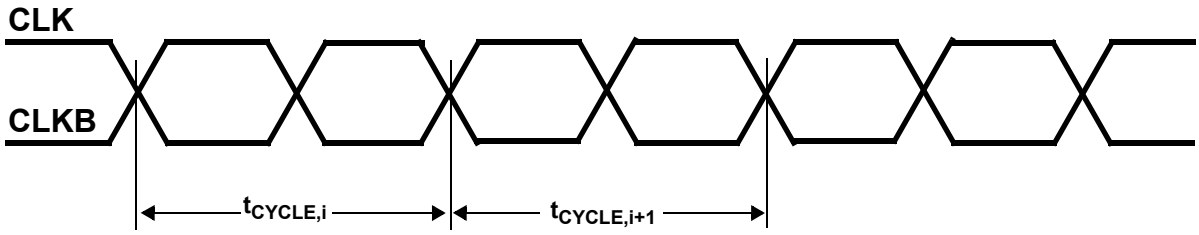

$$t_6 = t_{cycle,i} - t_{cycle,i+1}$$

**Figure 3. 54MOUT, LCLK Cycle-to-Cycle Jitter**



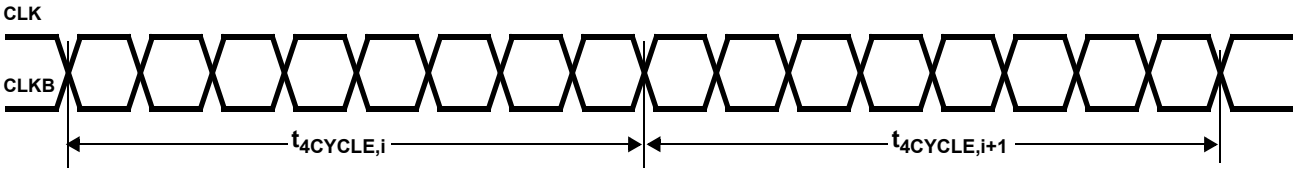

$$t_7 = t_{1000cycle,i} - t_{1000cycle,i+1}$$

**Figure 4. 54MOUT, LCLK 1000 Cycle Jitter**



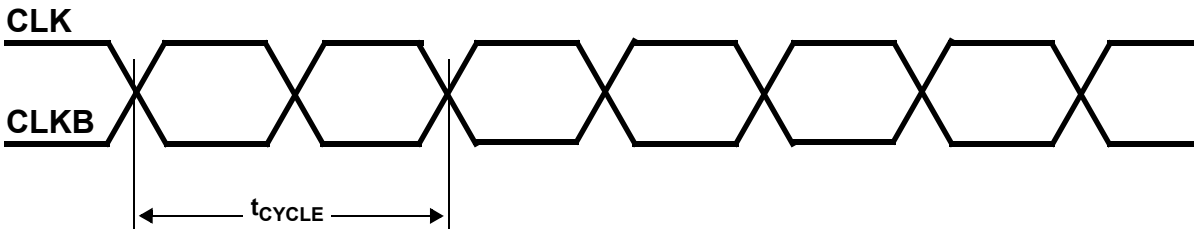

$t_8 = t_{CYLCE,i} - t_{CYCLE,i+1}$ over 10000 consecutive cycles

**Figure 5. CLK, CLKB Cycle-to-Cycle Jitter**



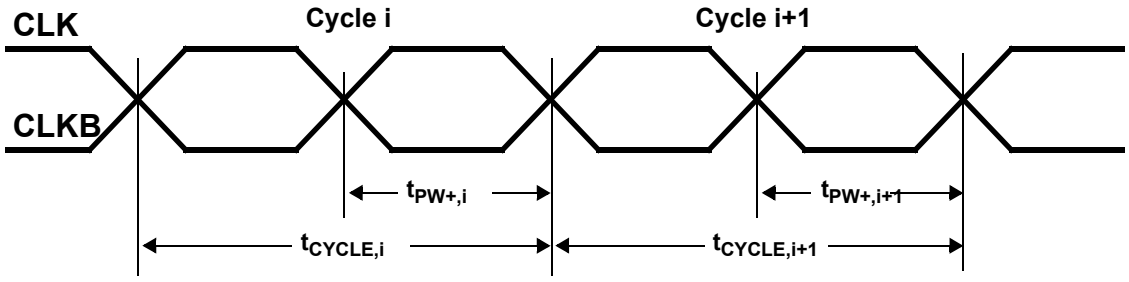

$t_8 = t_{4CYCLE,i} - t_{4CYCLE,i+1}$ over 10000 consecutive cycles

**Figure 6. CLK, CLKB 4-Cycle-to-Cycle Jitter**




$t_9 = t_{CYCLE,max} - t_{CYCLE,min}$ over 10000 cycles

**Figure 7. CLK, CLKB Long-term Jitter**




$t_{10} = t_{PW+,i} - t_{PW+,i+1}$

**Figure 8. CLK, CLKB Duty Cycle Error**

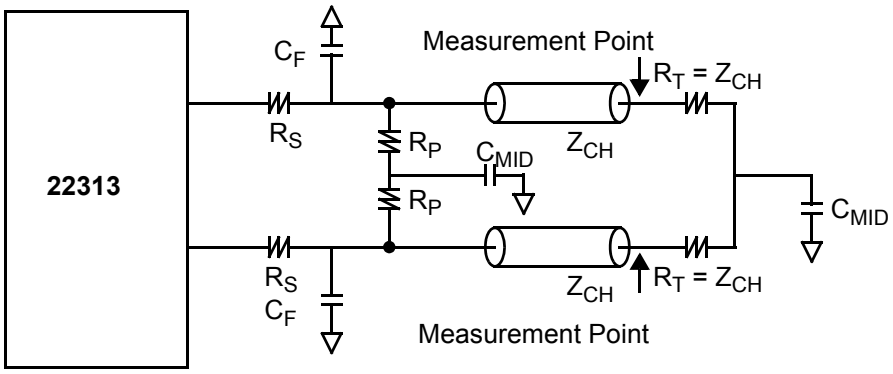



**Figure 9. Direct Rambus Test Circuit**

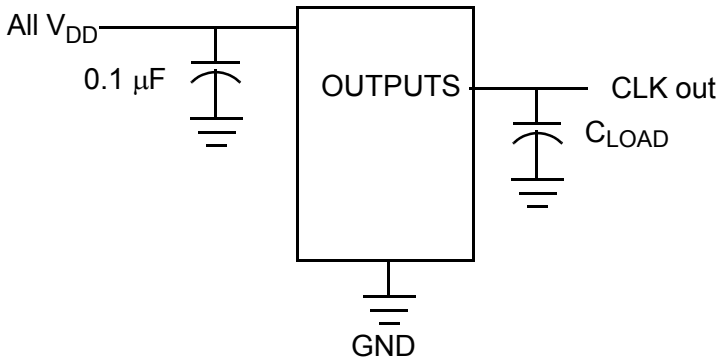



**Figure 10. LCLK, 54MOUT Output Test Circuits**

**Table 1. Direct Rambus Test Circuit Component Values**

| Parameter | Description | Value | Tolerance | Unit |
|---|---|---|---|---|
| $R_S$ | Series Resistor | 68 | ±5% | Ω |
| $R_P$ | Parallel Resistor | 39 | ±5% | Ω |
| $C_F$ | Edge-Rate Filter Capacitor[17] | 15 | ±10% | pF |
| $C_{MID}$ | AC Ground Capacitor | 0.01 | ±20% | µF |

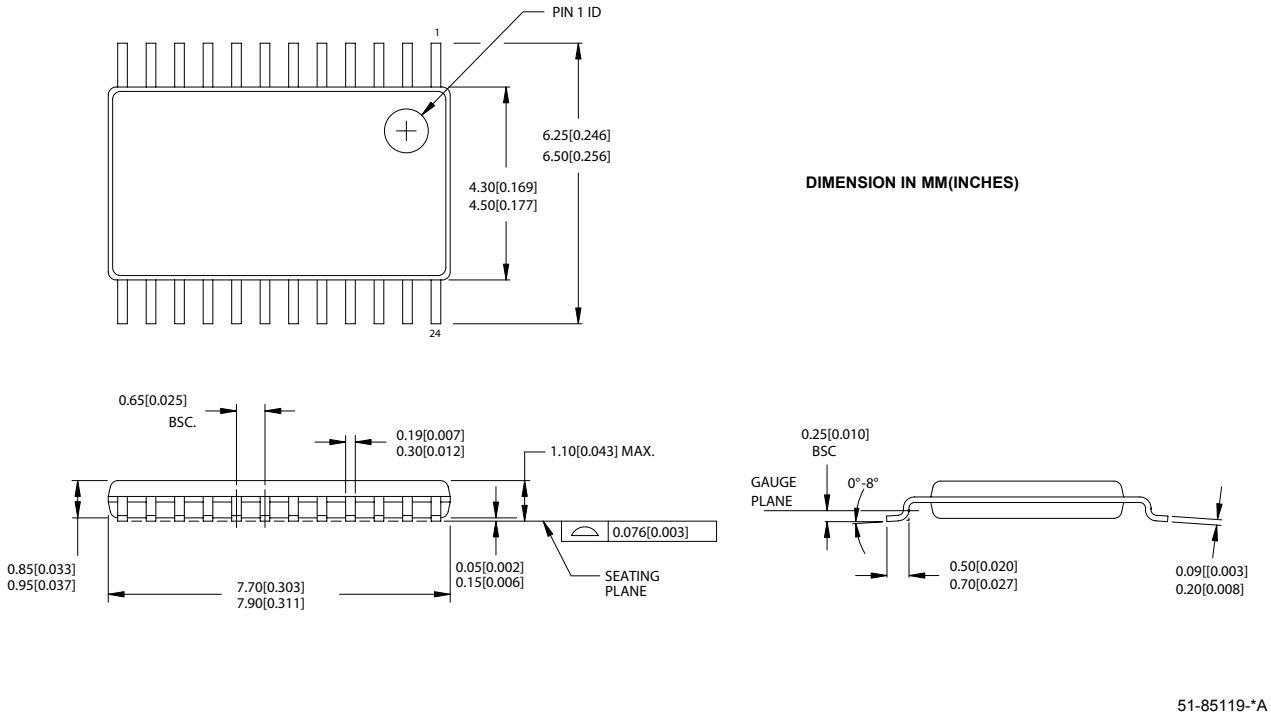
## Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range | Operating Voltages |
|---|---|---|---|---|
| CY22313ZC | Z24 | 24-lead TSSOP | Commercial ($T_A$ = 0°C to 85°C) | 3.45V |
| CY22313ZCT | Z24 | 24-lead TSSOP – Tape and Reel | Commercial ($T_A$ = 0°C to 85°C) | 3.45V |
| **Lead Free** | | | | |
| CY22313ZXC | Z24 | 24-lead TSSOP | Commercial ($T_A$ = 0°C to 85°C) | 3.45 |
| CY22313ZXCT | Z24 | 24-lead TSSOP – Tape and Reel | Commercial ($T_A$ = 0°C to 85°C) | 3.45 |

**Notes:**
17. CF is OPTIONAL filter capacitor for adjusting edge rates and EMI. No filter capacitors are used for characterization and test data.

## Package Drawing and Dimensions

**24-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z24**

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## Document History Page

| Document Title: CY22313 Two-PLL Clock Generator with Direct Rambus™ (Lite) Support<br>Document Number: 38-07434 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 117092 | 07/02/02 | CKN | New Data Sheet |
| *A | 121365 | 11/15/02 | CKN | Reordered Pin Description table<br>Changed all 3.3V references to 3.45V<br>Changed RI_FS min. spec to 60 KOhms<br>Changed note 4<br>Inserted max. spec for Edge Rates<br>Reduced min. spec for Edge Rates on 1.8V and 1.675V outputs<br>Inserted phase noise specifications<br>Created separate specs for Jitter, depending on output voltage<br>Correctly specified CF in *Table 1* |
| *B | 121773 | 02/17/03 | CKN | Added $t_{PU}$ row to the Recommended Operating Conditions table |
| *C | 125454 | 05/19/03 | CKN | Updated Switching Characteristics table<br>Added CY22313LF ordering information and corresponding note |
| *D | 127393 | 06/12/03 | RGL | Removed “PRELIMINARY”<br>Rephrased Note 18 to provide clarity on marking |
| *E | 239051 | See ECN | RGL | Corrected the Lead Free Coding in the Ordering Information table |