

High-Frequency SPDT Antenna Switch**Description**

The CXG1016N is a high power antenna switch MMIC. This IC is designed using the Sony's GaAs J-FET process and operates at a single positive power supply

Features

- Single positive power supply operation
- Low insertion loss 0.45 dB (Typ.) at 1.5 GHz
- Isolation 20 dB (Typ.) at 1.5 GHz
- High power switching

P1 dB (Typ.)	33 dBm	at 1.5 GHz
		$V_{CTL(H)}=3.0\text{ V}$
	37 dBm	at 1.5 GHz
		$V_{CTL(H)}=4.0\text{ V}$

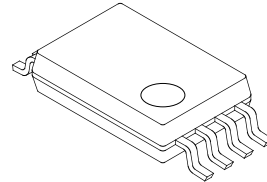
Applications

Antenna switch for digital cellular telephones

Structure

GaAs J-FET MMIC

8 pin SSOP (Plastic)

**Absolute Maximum Ratings (Ta=25 °C)**

- | | | | |
|-------------------------|-----------|-------------|----|
| • Control voltage | V_{ctl} | 7 | V |
| • Operating temperature | T_{opr} | -35 to +85 | °C |
| • Storage temperature | T_{stg} | -65 to +150 | °C |

Operating Condition

- | | | | |
|-------------------|--|-----|---|
| • Control voltage | | 0/4 | V |
|-------------------|--|-----|---|

Electrical Characteristics

$V_{CTL(L)}=0\text{ V}$, $V_{CTL(H)}=4\text{ V}$, $P_{IN}=32\text{ dBm}$, $R_{EF}=75\text{ k}\Omega$

($T_a=25\text{ }^\circ\text{C}$)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL1	f=1.0 GHz		0.4	0.7	dB
Isolation	ISO1		20	23		dB
Insertion Loss	IL1.5	f=1.5 GHz		0.45	0.75	dB
Isolation	ISO1.5		17	20		dB
Insertion Loss	IL2	f=2.0 GHz		0.5	0.8	dB
Isolation	ISO2		14	17		dB
VSWR	VSWR				1.5	
Switching Time	TSW			100		ns

$V_{CTL(L)}=0\text{ V}$, f=2 GHz

($T_a=25\text{ }^\circ\text{C}$)

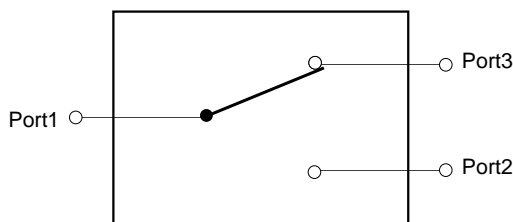
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
1 dB Compression Point	P1 dB (3)	$V_{CTL(H)}=3\text{ V}$	31	33		dBm
1 dB Compression Point	P1 dB (4)	$V_{CTL(H)}=4\text{ V}$	35	37		dBm

$V_{CTL(L)}=0\text{ V}$, $R_{RF}=75\text{ k}\Omega$

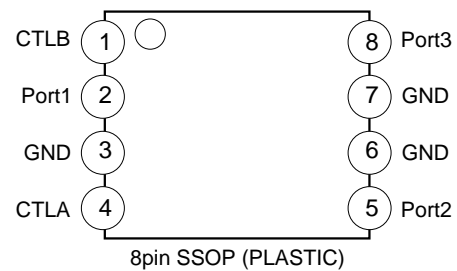
($T_a=25\text{ }^\circ\text{C}$)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Control Current	$I_{CTL(1)}$	$V_{CTL(H)}=3\text{ V}$		120	170	μA
Control Current	$I_{CTL(2)}$	$V_{CTL(H)}=4\text{ V}$		170	220	μA
Control Current	$I_{CTL(3)}$	$V_{CTL(H)}=5\text{ V}$		250	300	μA

Block Diagram

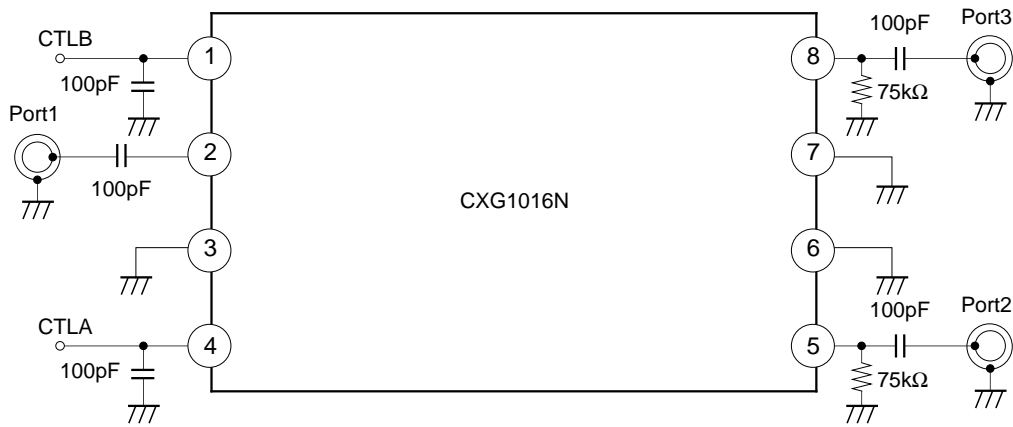


Package Outline/Pin Configuration

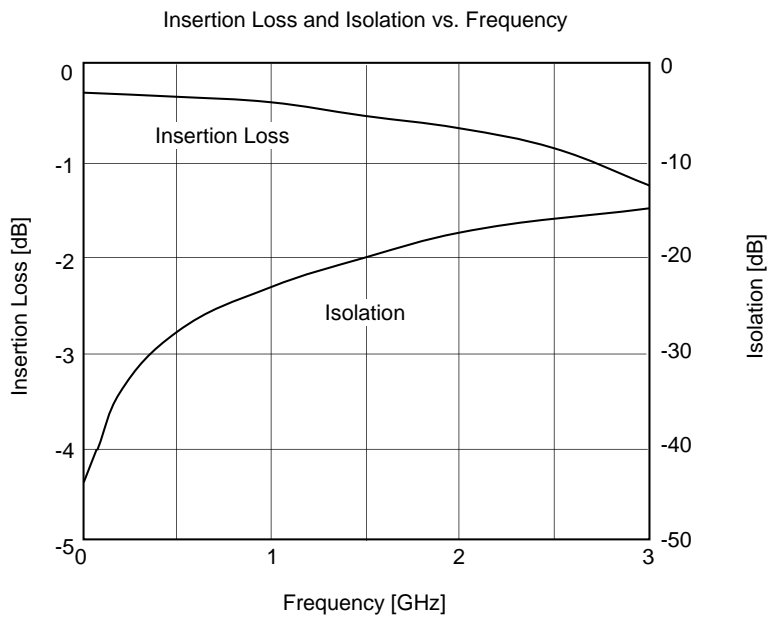
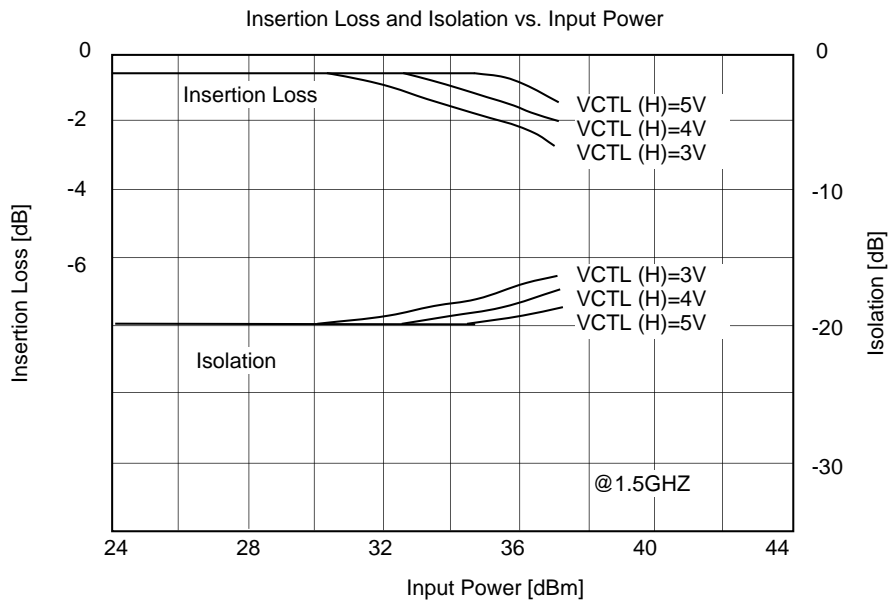


V_{CTLA}	V_{CTLB}	
High	Low	Port1-Port2 ON Port1-Port3 OFF
Low	High	Port1-Port2 OFF Port1-Port3 ON

Recommended Circuit

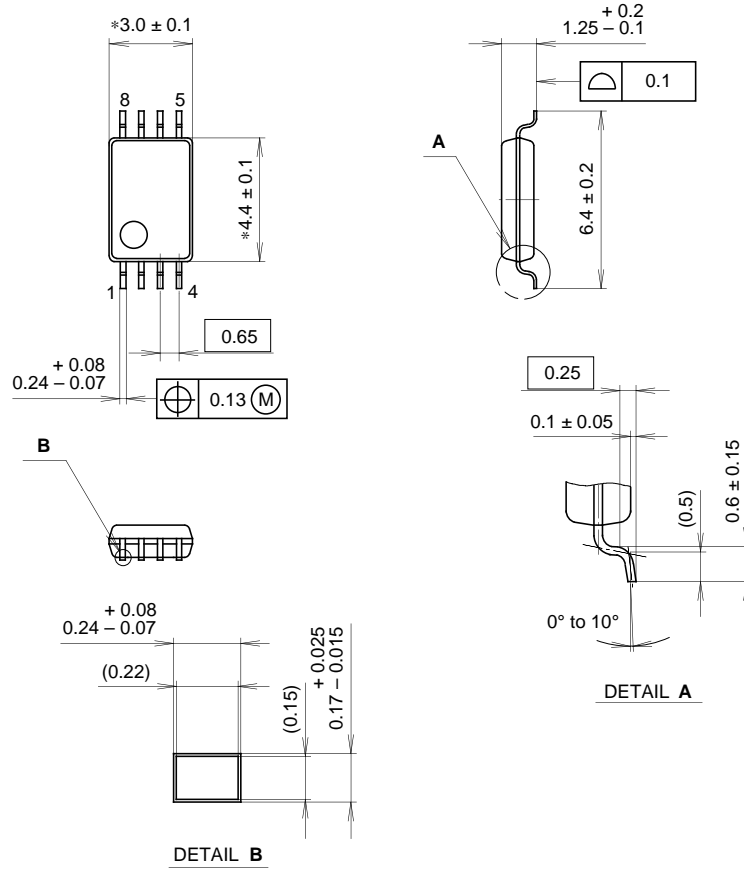


Example of Representative Characteristics (Ta=25 °C)



Package Outline Unit : mm

8PIN SSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-8P-L01
EIAJ CODE	SSOP008-P-0044
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.04g