SONY

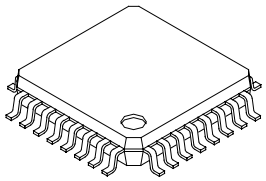
CXB1563Q

2R IC for Optical Fiber Communication Receiver

Description

The CXB1563Q achieves the 2R optical-fiber communication receiver functions (Reshaping and Regenerating) on a single chip. This IC is also equipped with the signal interruption alarm output function, which is used to discriminate the existence of data input.

32 pin QFP (Plastic)



Features

- Auto-offset canceler circuit
- Signal interruption alarm output
- 2-level switching function of identification maximum voltage amplitude for alarm block
- Single 5V power supply

Applications

- SONET/SDH : 622.08Mb/s
- Fiber channel : 531.25Mb/s

Absolute Maximum Ratings

• Supply voltage	$V_{CC} - V_{EE}$	–0.3 to +7.0	V
• Storage temperature	Tstg	–65 to +150	°C
• Input voltage difference : I $V_D - V_{\overline{D}}$ I	Vdif	0.0 to +2.5	V
• SW input voltage	Vi	V_{EE} to V_{CC}	V
• Output current (Continuous)	I_O	0 to 50	mA
(Surge current)		0 to 100	mA

Recommended Operating Conditions

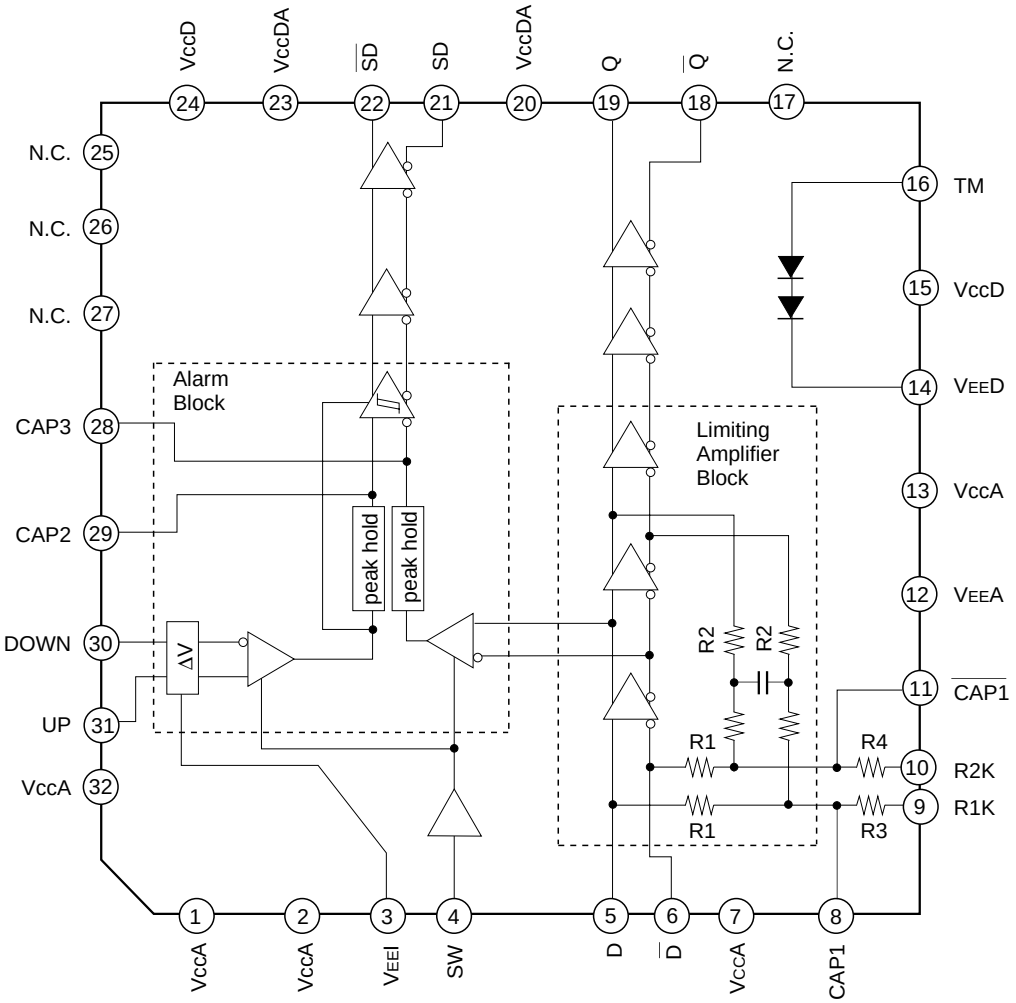
• Supply voltage	$V_{CC} - V_{EE}$	5.0±0.5	V
• Termination voltage (for data/alarm)	$V_{CC} - V_{T1}$	1.8 to 2.2	V
• Termination voltage (for alarm 2)	V_{T2}	V_{EE}	V
• Termination resistance (for data/alarm)	R_{T1}	45 to 55	Ω
• Termination resistance (for alarm 2)	R_{T2}	460 to 560	Ω
• Operating temperature	Ta	–40 to +85	°C

Structure

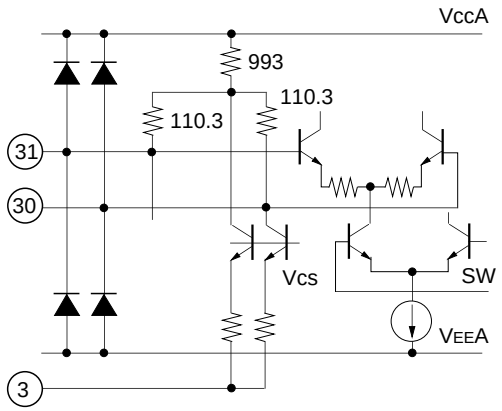
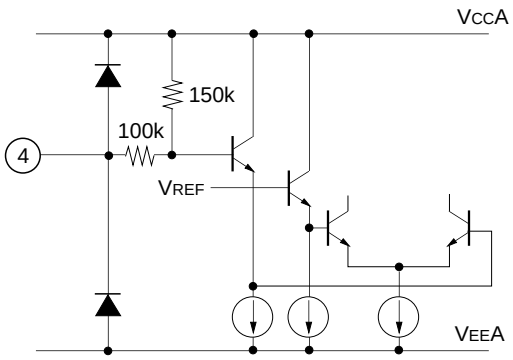
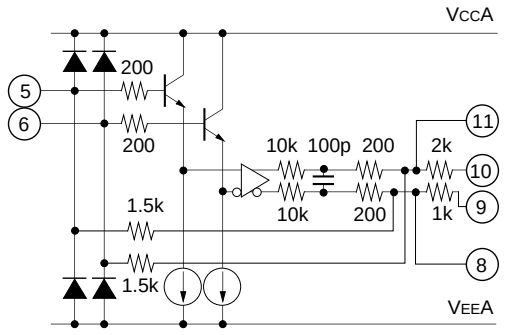
Bipolar silicon monolithic IC

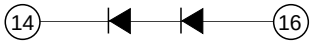
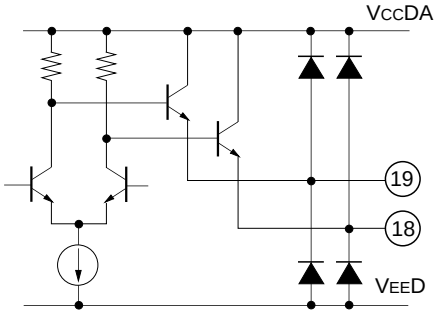
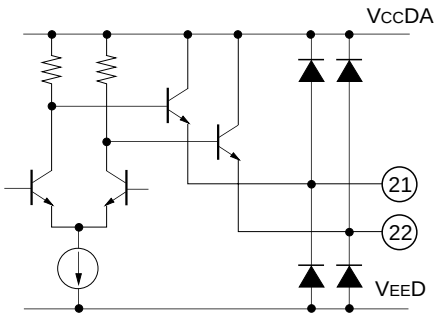
E95710B1Z-PS

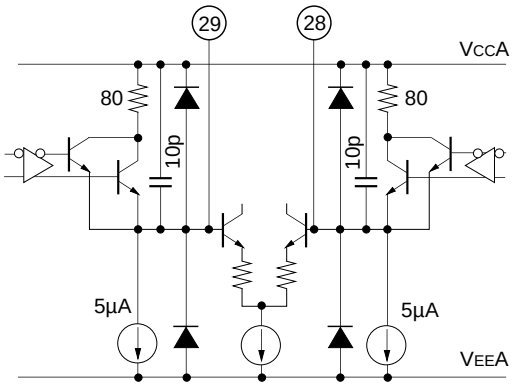
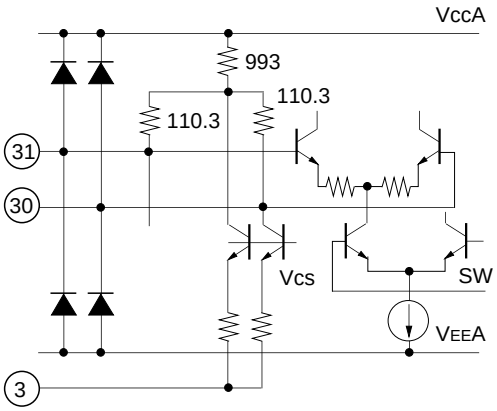
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Typical pin voltage (V) DC	Typical pin voltage (V) AC	Equivalent circuit	Description
1,2	$V_{CC}A$	0V			Positive power supply for analog block.
3	$V_{EE}I$	–5V			Generates the default voltage between UP and DOWN. The voltage (8.0mV for input conversion) can be generated between UP and DOWN (Pins 30 and 31) as alarm setting level by connecting this pin to $V_{EE}A$.
4	SW	0V (OPEN) or –5V			Switches the identification maximum voltage amplitude. High voltage when open; the identification maximum voltage amplitude becomes 50mVp-p. Low voltage when connecting this pin to V_{EE}; the amplitude becomes 20mVp-p.
5	D	–1.3V	–0.9V to –1.7V		Limiting amplifier block input. Be sure to make this input with AC coupled.
6	$\overline{D}$	–1.3V	–0.9V to –1.7V		
7	$V_{CC}A$	0V			Positive power supply for analog block.
8	CAP1	–1.8V			Pins 8 and 11 connect a capacitor which determines the cut-off frequency for feedback block, and 1kΩ is connected between Pins 8 and 9; 2kΩ between Pins 10 and 11. A resistor which is to be inserted in parallel with a capacitor can be selected 5 ways by external wiring, and DC feedback can be varied.
9	R1K				
10	R2K				
11	$\overline{CAP1}$	–1.8V			

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
12	$V_{EE}A$	–5V			Negative power supply for analog block.
13	$V_{CC}A$	0V			Positive power supply for analog block.
14	$V_{EE}D$	–5V			Negative power supply for digital block.
15	$V_{CC}D$	0V			Positive power supply for digital block.
16	TM	–3.4V			Chip temperature monitor.
17	N.C				No connected.
18	$\overline{Q}$		–0.9V to –1.7V		Data signal output. Terminate this pin in 50Ω at V_{TT} = –2V.
19	Q		–0.9V to –1.7V		
20	$V_{CC}DA$	0V			Positive power supply for output buffer.
21	SD		–0.9V to –1.7V		Alarm signal output. Terminate this pin in 50Ω at V_{TT} = –2V.
22	$\overline{SD}$		–0.9V to –1.7V		
23	VccDA	0V			Positive power supply for digital block.
24	VccD	0V			Positive power supply for digital block.
25	N.C				No connected.
26	N.C				
27	N.C				

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
28	CAP3	–1.8V			Connects a peak hold circuit capacitor for alarm block. 470pF should be connected to VccA each. CAP2 pin → Peak hold capacitor connection for alarm level setting block. CAP3 pin → Peak hold capacitor connection for limiting amplifier signal.
29	CAP2	–1.8V			
30	DOWN	–0.84V (for VEEI = –5V)			Connects a resistor for alarm level setting. Default voltage can be generated without an external resistor by shorting the VEEI pin to VEEA.
31	UP	–0.8V (for VEEI = –5V)			
32	VccA	0V			Positive power supply for analog block.

Electrical Characteristics

• DC characteristics

(V_{CC} = GND, V_{EE} = –5V±10%, Ta = –40 to +85°C, V_{CC} = V_{CC}D, V_{CC}DA, V_{CC}A V_{EE} = V_{EE}D, V_{EE}A)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply	I_{EE}	R_{T1} = 50Ω, V_{T1} = –2V termination	–50	–37	–28	mA
Q/$\overline{Q}$ SD/$\overline{SD}$ High output voltage	V_{OH}	R_{T1} = 50Ω, V_{T1} = –2V termination, Ta = 0 to 85°C	–1025		–880	mV
Q/$\overline{Q}$ SD/$\overline{SD}$ Low output voltage	V_{OL}		–1810		–1620	
SD/$\overline{SD}$ High output voltage 2	V_{OHb}	R_{T2} = 510Ω, V_{EE} termination, Ta = 0 to 85°C	–1075		–830	
SD/$\overline{SD}$ Low output voltage 2	V_{OLb}		–1860		–1570	
SW High input voltage	V_{IH}		–1900		0	
SW Low input voltage	V_{IL}		V_{EE}		–2500	
SW High input current	I_{IH}				2	µA
SW Low input current	I_{IL}		–60			
D/$\overline{D}$ input resistance	Rin		1125	1500	1875	Ω
Internal resistance 1 for alarm level setting	Ra1	Refer to Fig. 3.	745	993	1241	
Internal resistance 2 for alarm level setting	Ra2A, B	Refer to Fig. 3.	82.7	110.3	137.9	
Pare ratio of internal resistance 2 for alarm level setting	δRa2	Ra2A/Ra2B	0.97		1.03	
Resistance between CAP1 and R1K	R3		745	993	1241	Ω
Resistance between $\overline{CAP1}$ and R2K	R4		1489	1986	2482	

• **AC characteristics**

(V_{CC} = GND, V_{EE} = –5V±10%, Ta = –40 to +85°C, V_{CC} = V_{CC}D, V_{CC}DA, V_{CC}A V_{EE} = V_{EE}D, V_{EE}A)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum input voltage amplitude	Vmax	Single-ended input	1600			mVp-p
Amplifier gain (in Limiting Amplifier)	Gv		40			dB
Identification maximum voltage amplitude of alarm level	VminA1	SW pad: Low, single-ended input	20			mVp-p
	VminA2	SW pad: Open High, single-ended input	50			
Hysteresis width	ΔP		4	6	7	dB
SD response assert time	Tas	Low → High*1	0		100	µs
SD response deassert time	Tdas	High → Low*2	2.3		100	
SD response assert time for alarm level default	Tasd	Low → High*3	0		100	
SD response deassert time for alarm level default	Tdasd	High → Low*4	2.3		100	
Alarm setting level for default	Vdef	UP/DOWN pins; Open, connect V_{EE}I to V_{EE}.	6.6	8.0	9.3	mV
Propagation delay time	T_{PD}	D to Q	0.4	1.0	1.6	ns
Q/$\overline{Q}$ rise time	Tr_Q	R_{T1} = 50Ω, V_{T1} = –2V termination, V_{EE} = –5V, Ta = 0 to 85°C 20% to 80%	250		450	ps
Q/$\overline{Q}$ fall time	Tf_Q		250		450	
SD/$\overline{SD}$ rise time	Tr_SD		0.45		1.6	ns
SD/$\overline{SD}$ fall time	Tf_SD		0.45		1.6	

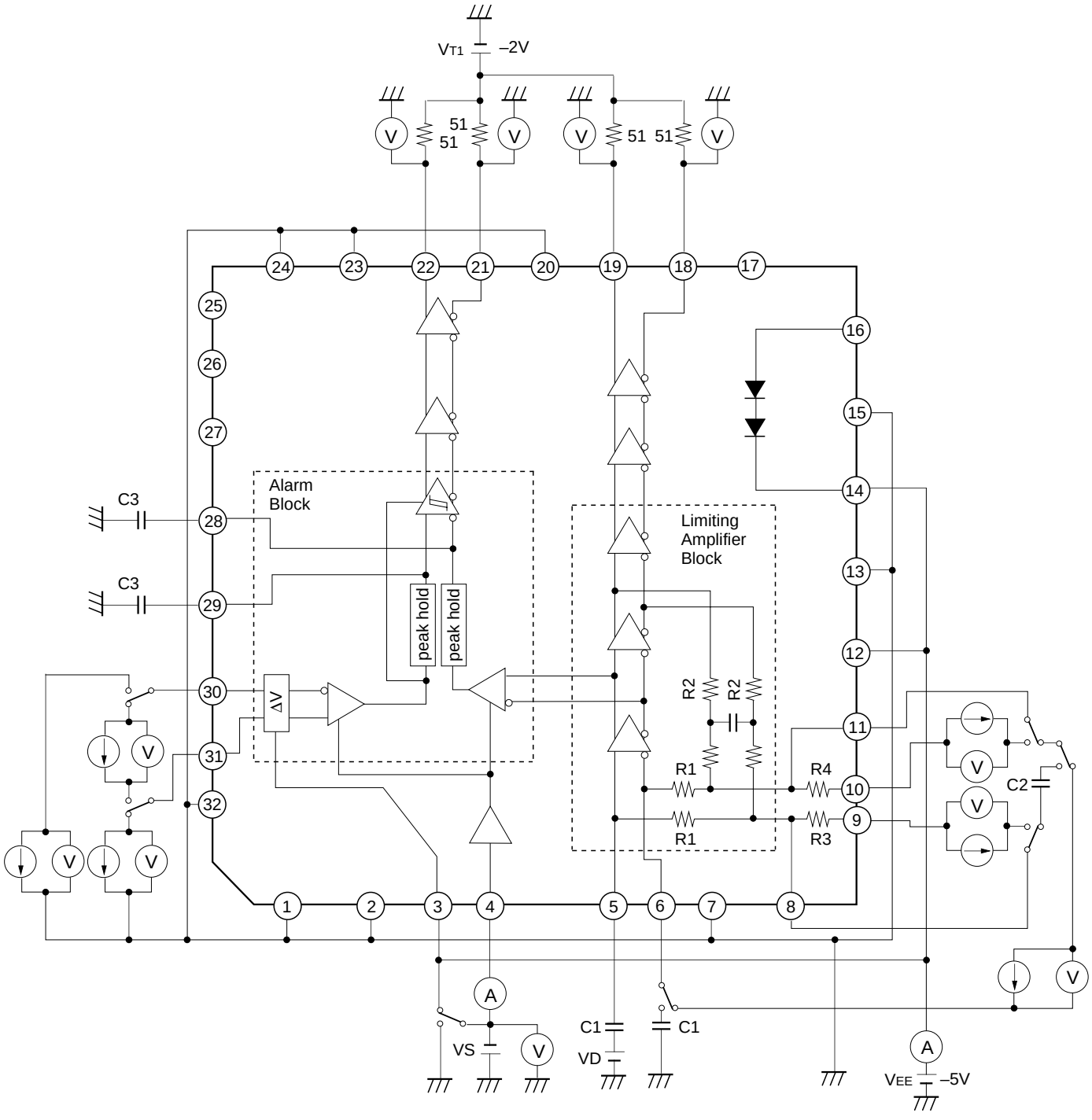
*1 V_{UP} – V_{DOWN} = 100mV, Vin = 100mVp-p (single ended), SW pin: High
Peak hold capacitance (CAP2, CAP3 pins) of 470pF; connect V_{EE}I to V_{EE}.

*2 V_{UP} – V_{DOWN} = 100mV, Vin = 1Vp-p (single ended), SW pin: High
Peak hold capacitance (CAP2, CAP3 pins) of 470pF; connect V_{EE}I to V_{EE}.

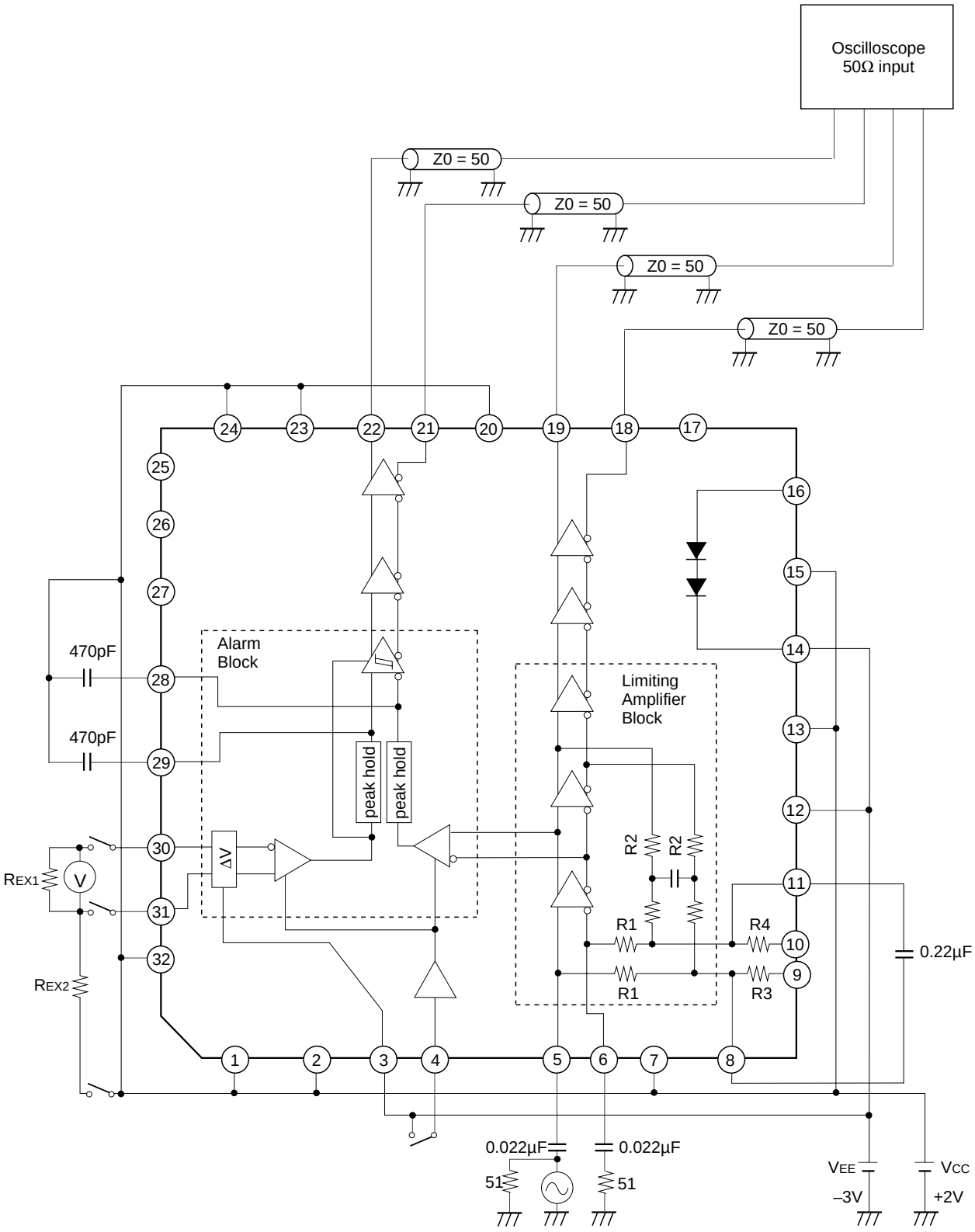
*3 Vin = 50mVp-p (single ended), SW pin: Low
Peak hold capacitance (CAP2, CAP3 pins) of 470pF; connect V_{EE}I to V_{EE}.

*4 Vin = 1Vp-p (single ended), SW pin: Low
Peak hold capacitance (CAP2, CAP3 pins) of 470pF; connect V_{EE}I to V_{EE}.

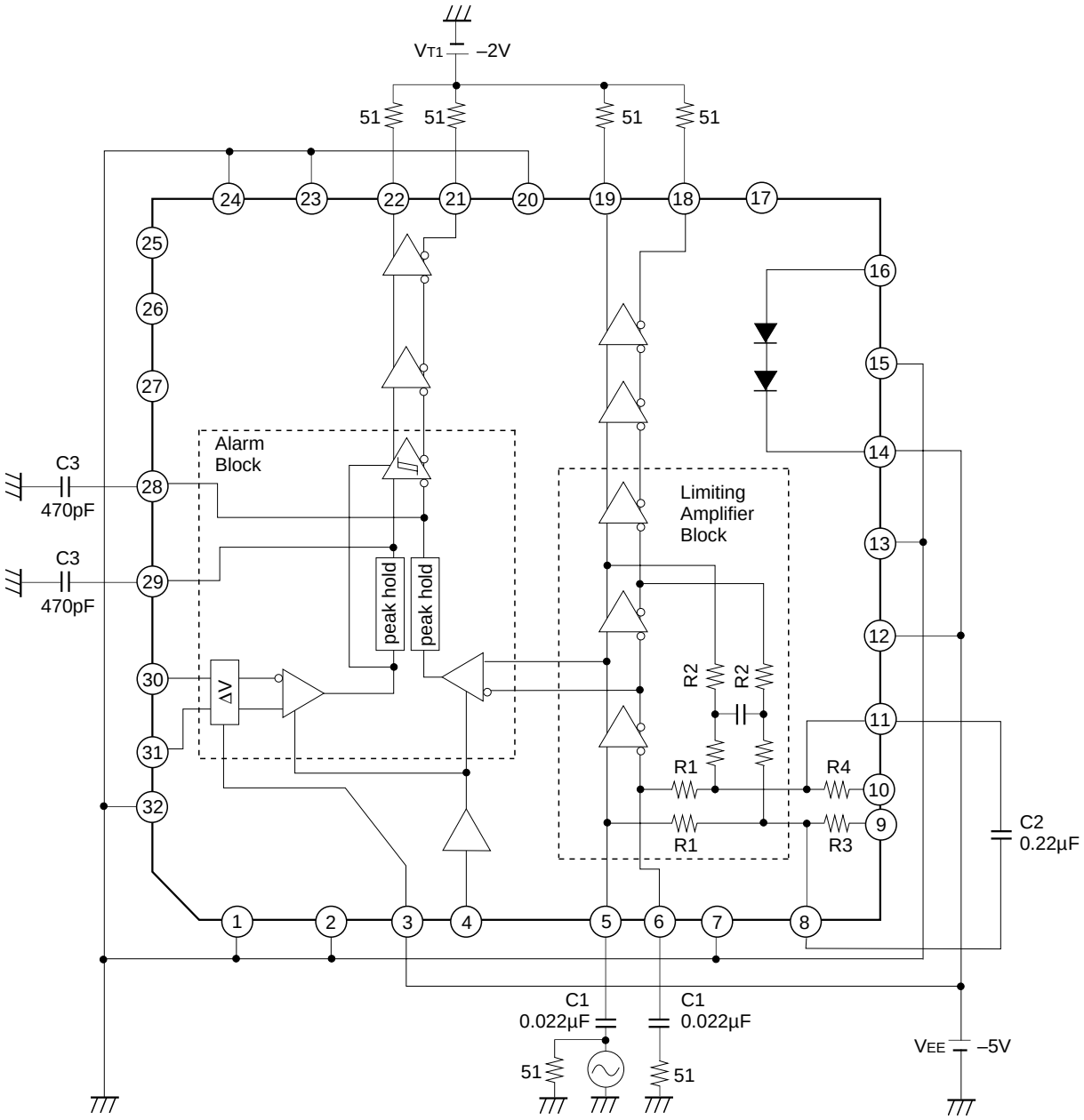
DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Limiting amplifier block

The limiting amplifier block is equipped with the auto-offset canceler circuit. When external capacitors C1 and C2 are connected as shown in Fig. 1, the DC bias is set automatically in this block. External capacitor C1 and IC internal resistor R1 determine the low input cut-off frequency f2 as shown in Fig. 2. Similarly, external capacitor C2 and IC internal resistor R2 determine the high cut-off frequency f1 for DC bias feedback. Since peaking characteristics may occur in the low frequency area of the amplifier gain characteristics depending on the f1/f2 combination, set the C1 and C2 so as to avoid the occurrence of peaking characteristics. The target values of R1 and R2 and the typical values of C1 and C2 are as indicated below. When a single-ended input is used, provide AC grounding by connecting Pin 6 to a capacitor which has the same capacitance as capacitor C1.

R1 (internal): 1.5kΩ
C1 (external): 0.022µF
→ f2: 4.8kHz

R2 (internal): 10kΩ
C2 (external): 0.22µF
→ f1: 72Hz

1kΩ is incorporated between Pins 8 and 9; 2kΩ between Pins 10 and 11. A resistance value which is to be inserted in parallel with a capacitor f2 can be selected 5 ways (∞, 3kΩ, 2kΩ, 1kΩ, 1k//2kΩ) by external wiring, and DC feedback can be varied.

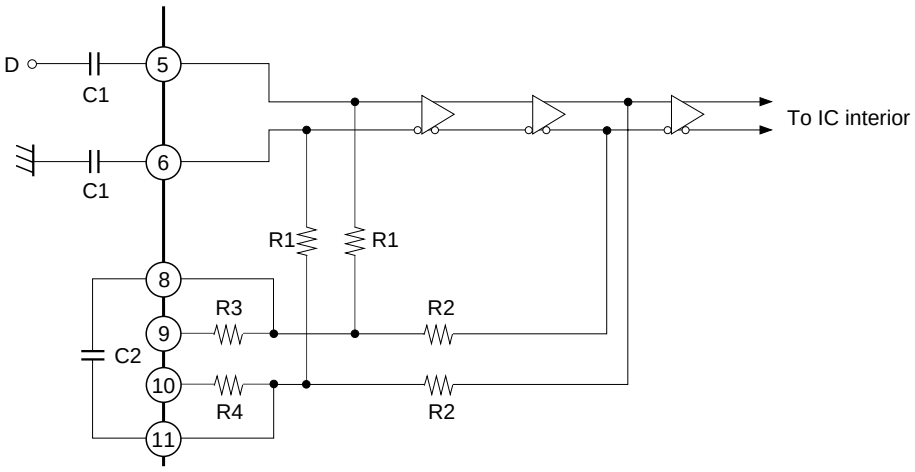


Fig. 1

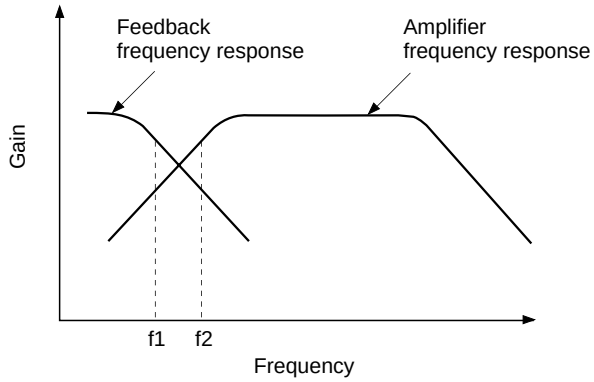


Fig. 2

2. Alarm block

In order to operate the alarm block, give the voltage difference between Pins 30 and 31 to set an alarm level and connect the peak hold capacitor C3 shown in Fig. 3.
This IC has two setting methods of alarm level; one is to connect V_{EE} to Pin 3 and leave Pins 30 and 31 open to set an alarm level default value (8mV for input conversion). The other is to connect Pin 3 to V_{EE} and set a desired alarm level using the external resistors R_{EX1} and R_{EX2} and R_{EX3} shown in Fig. 3.
Connect R_{EX1} between Pins 30 and 31, or between Pin 30 and V_{CC} when less alarm level is desired to be set than its default value; connect R_{EX2} between Pin 31 and Vcc potential when more alarm level is desired to be set than its default value. However, the Pin 31 voltage must be higher than that of Pin 30. Refer to Figs. 5, 8 to 13 for this alarm level setting.
This IC also features two-level setting of identification maximum voltage amplitude. The amplitude is set to 50mVp-p when Pin 4 is left open (High level) and it is set to 20mVp-p when Pin 4 is Low level. Therefore, noise margin can be increased by setting Pin 4 to Low level when small signal is input. The relation of input voltage and peak hold output voltage is shown in Fig. 6.
In the relation between the alarm setting level and hysteresis width, the hysteresis width is designed to maintain a constant gain (design target value: 6dB) as shown in Fig. 4. The C3 capacitance value should be set so as to obtain desired assert time and deassert time settings for the alarm signal.
The electrical characteristics for the SD response assert and deassert times are guaranteed only when the waveforms are input as shown in the timing chart of Fig. 7.
The typical values of R_{EX1}, R_{EX2}, R_{EX3} and C3 are as follows: (Approximately 10pF capacitor is built in Pins 28 and 29 each.)

R_{EX1} : 217Ω (when the alarm level is set to 4mV for input conversion.)
R_{EX2} : 634Ω (when the alarm level is set to 19mV for input conversion.)
R_{EX3} : 4kΩ (when the alarm level is set to 4mV for input conversion.)
C3 : 470pF

The table below shows the alarm logic.

Optical signal input state	SD	$\overline{SD}$
Signal input	High level	Low level
Signal interruption	Low level	High level

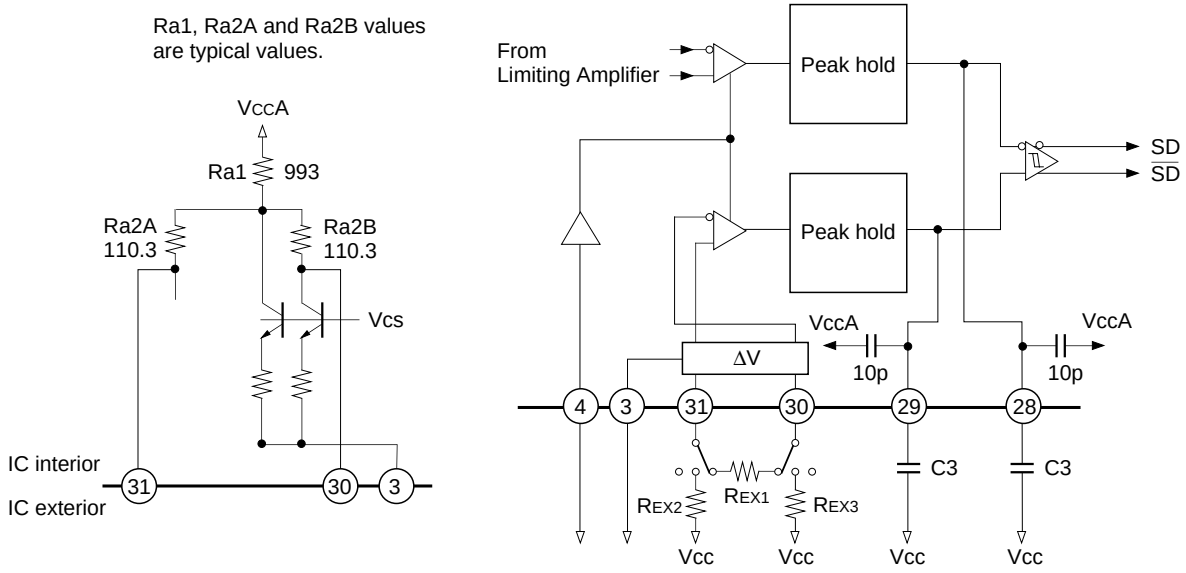


Fig. 3

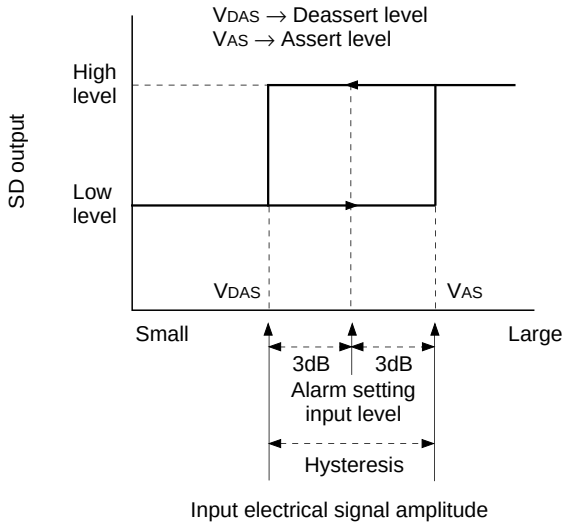


Fig. 4

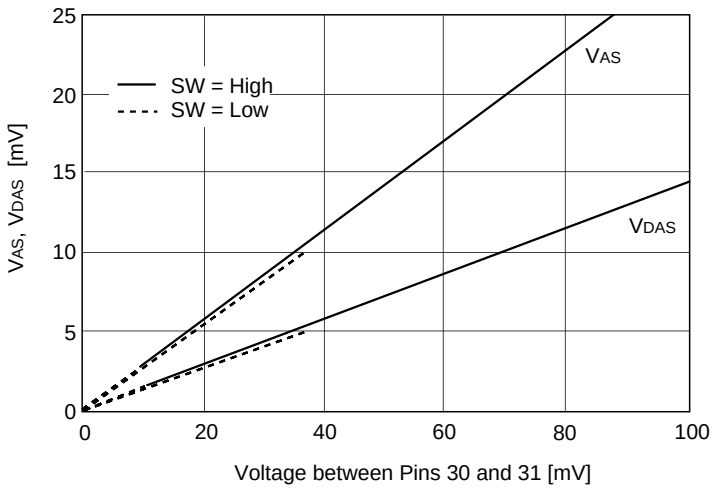


Fig. 5

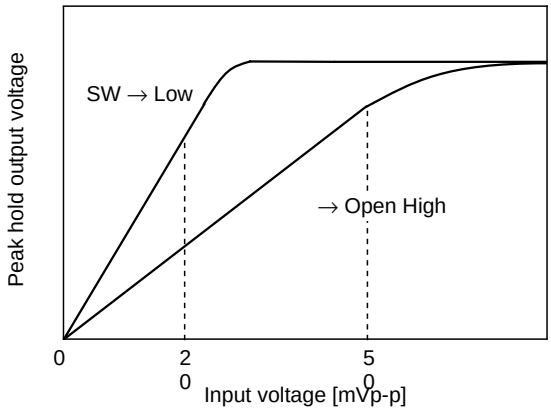


Fig. 6

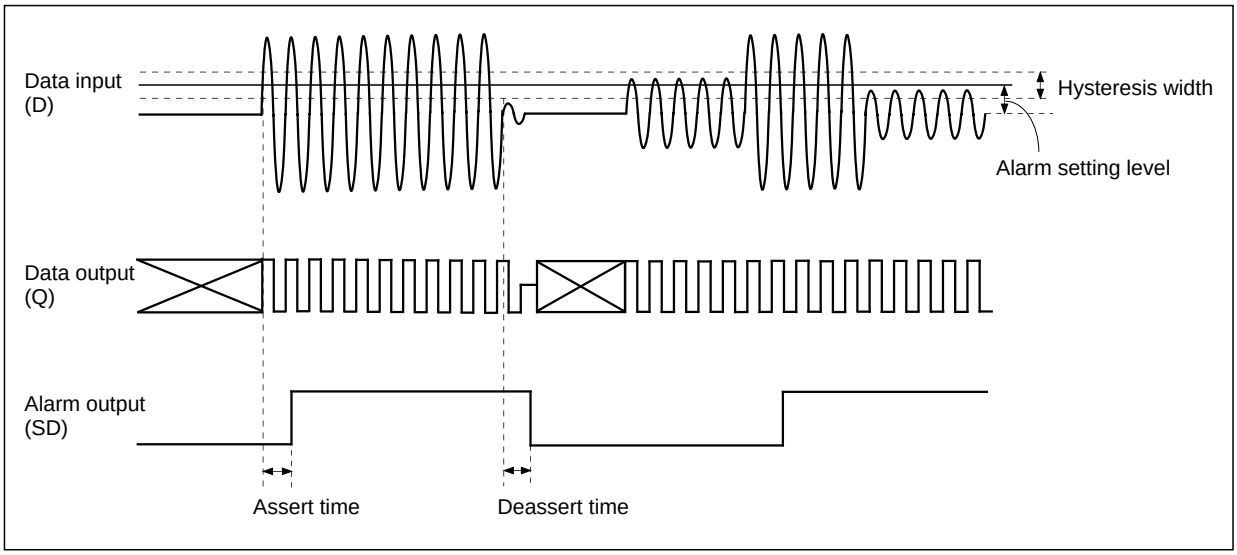


Fig. 7

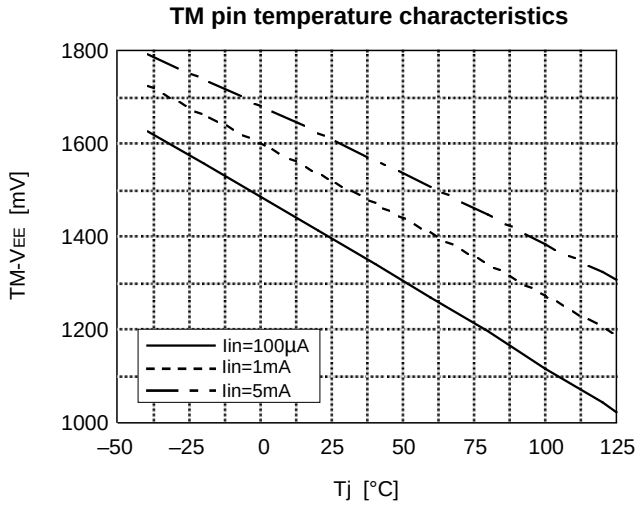


Fig. 8

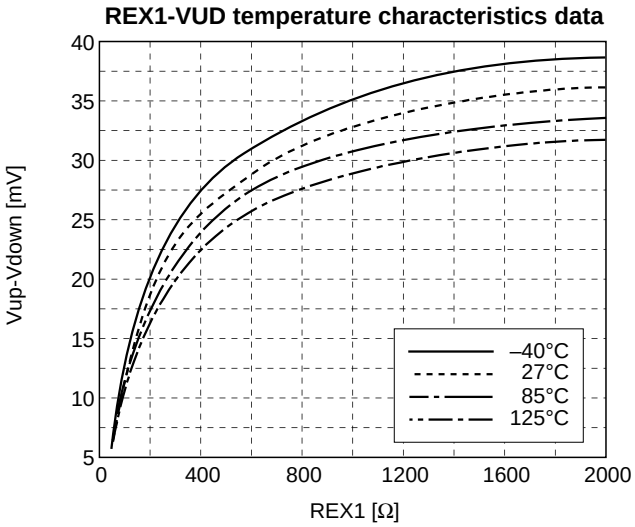


Fig. 9

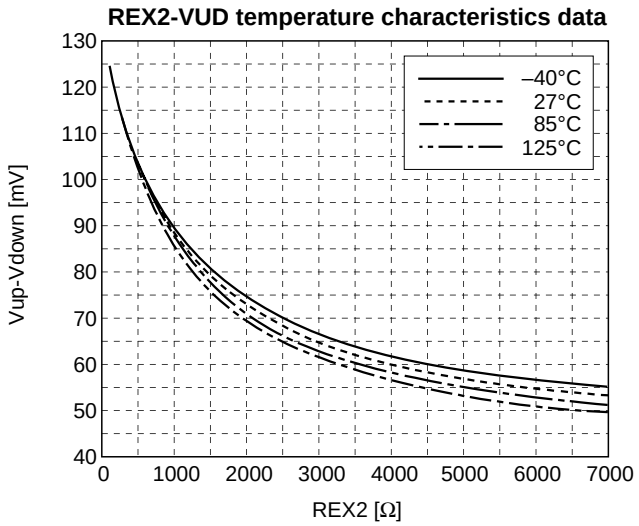


Fig. 10

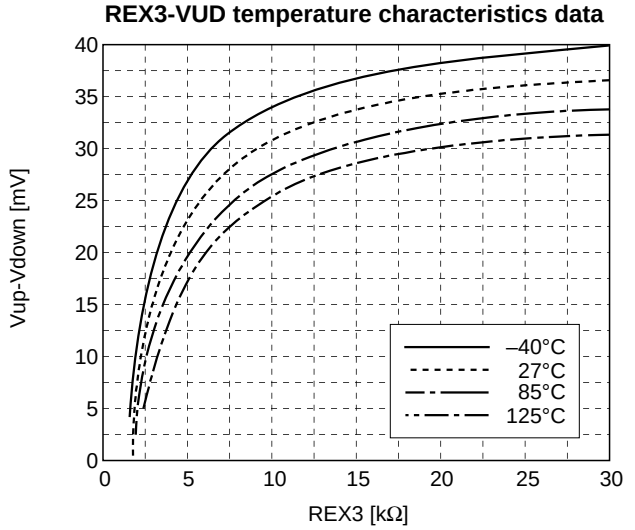


Fig. 11

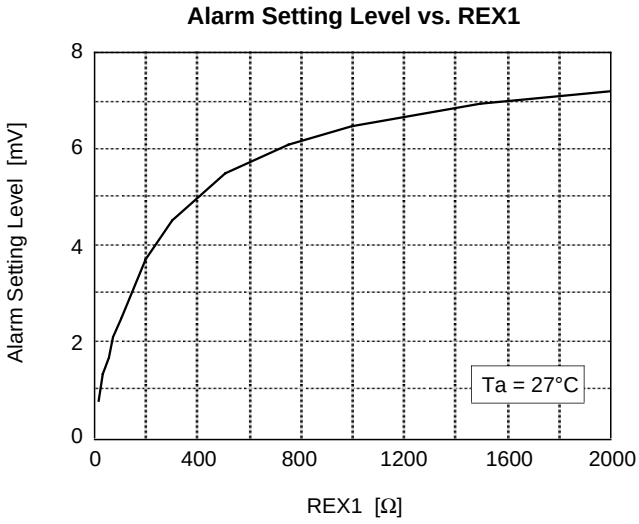


Fig. 12

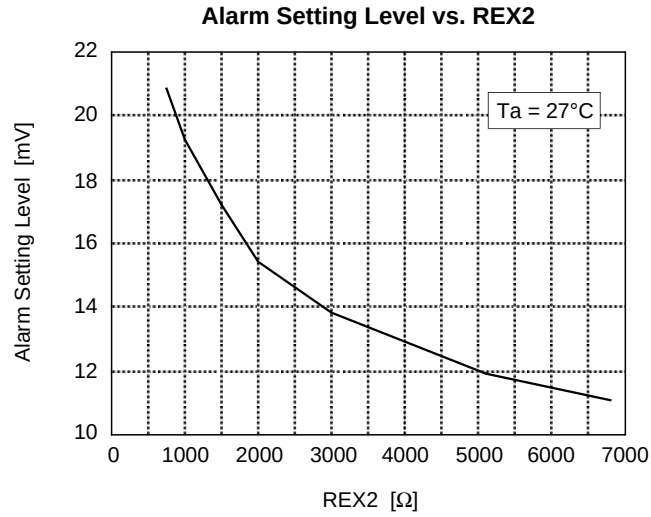


Fig. 13

3. Others

Pay attention to handling this IC because its electrostatic discharge strength is weak.

Example of Representative Characteristics

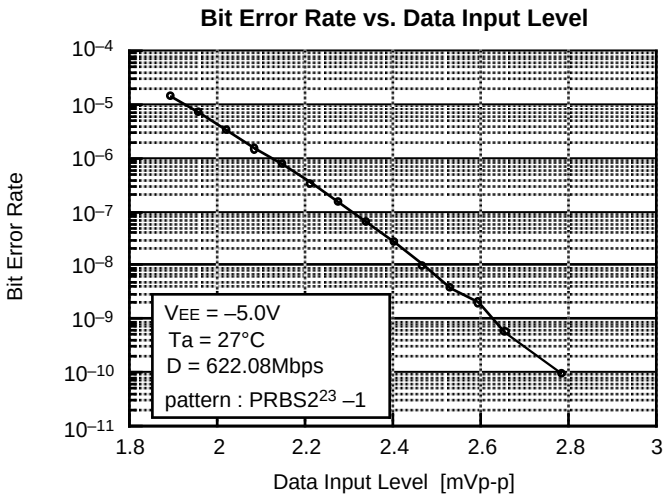


Fig. 14

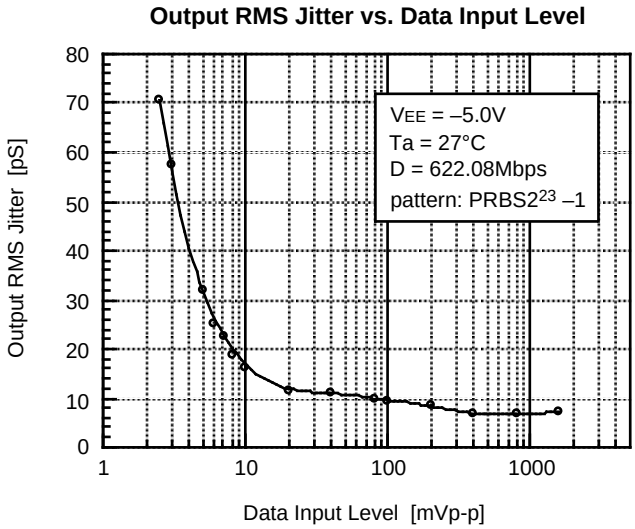


Fig. 15

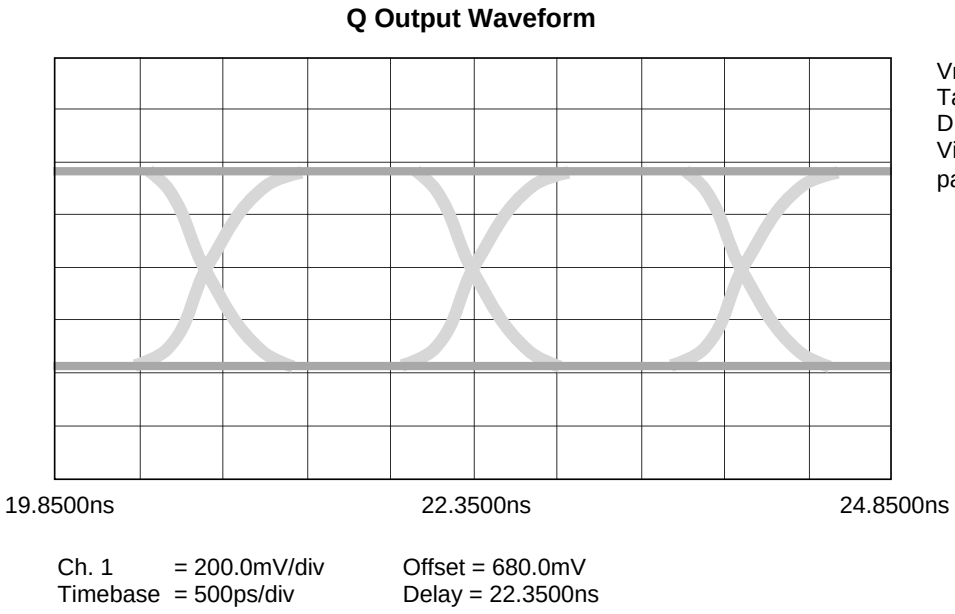
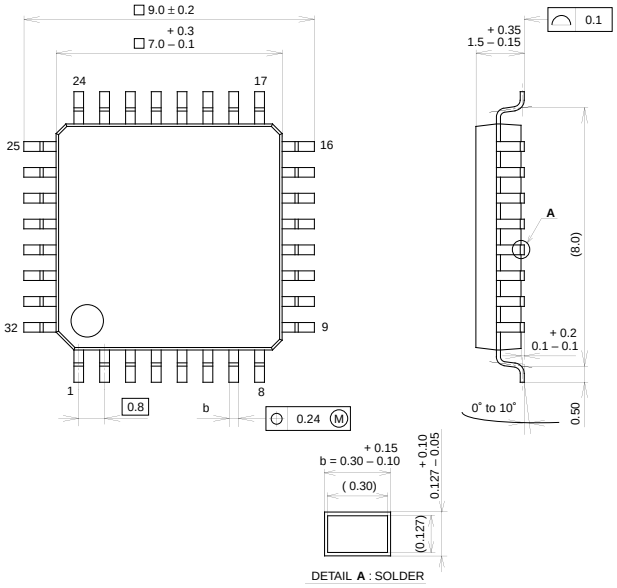


Fig. 16

Package Outline Unit: mm

32PIN QFP (PLASTIC)



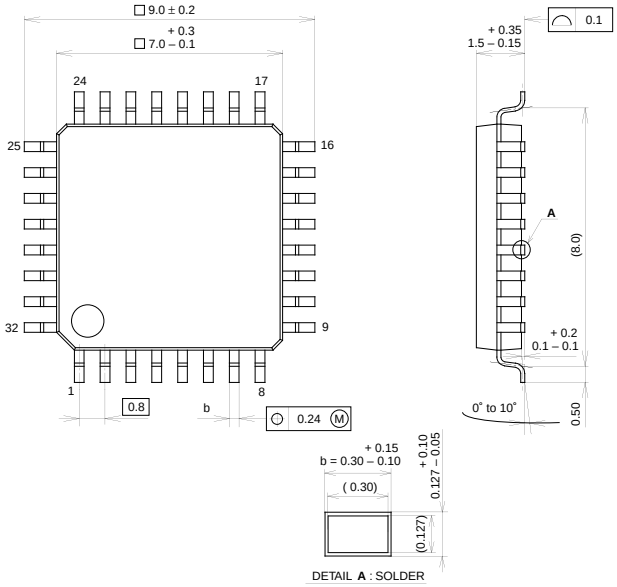
SONY CODE	QFP-32P-L01
EIAJ CODE	P-QFP32-7x7-0.8
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.2g

Kokubu Ass'y

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	P-QFP32-7x7-0.8
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.2g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm