CIRRUS LOGIC®

CS7410

CD/MP3/WMA Audio Controller

Features

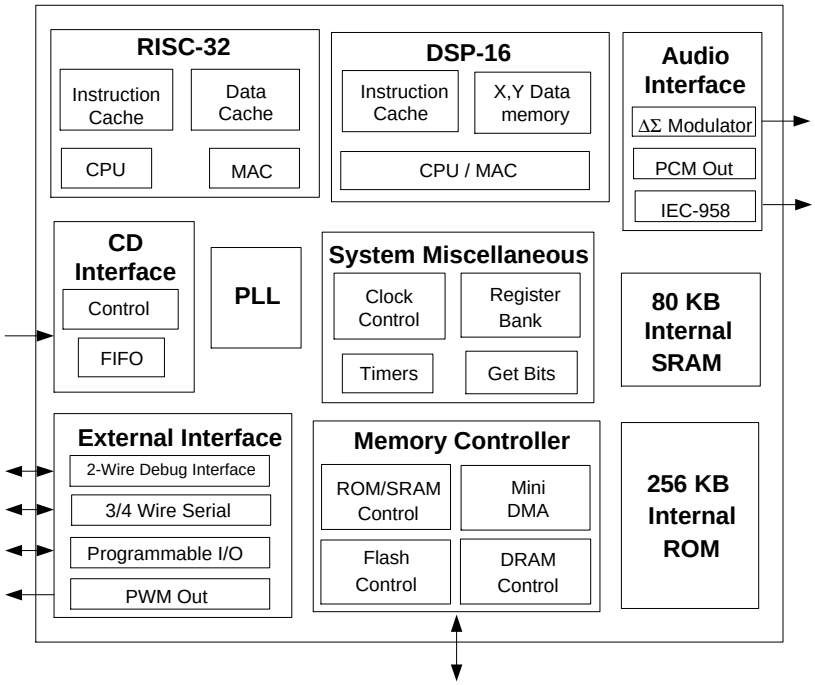
- Super on-chip Integration for low cost and low count bill of materials
- 32-Bit RISC Processor performs audio decode and system management functions
- 16-bit DSP for audio special effects
- 80 Kbytes internal SRAM, and 256 Kbytes internal ROM
- Interfaces to external SDRAM or EDO DRAM (for shock protection), and to external ROM/FLASH (for custom program storage)
- CD serial interface with advanced pattern matching and software error handling
- Integrated DAC functionality
- Simultaneous 4 channels PCM audio output and IEC-958 output.
- Large number of GPIO pins for servo control, key scan, LCD control, etc.
- Three serial control/status ports
- Sophisticated clock management and low power consumption
- Supports ISO9660 and multi-session write methods
- Low power 0.18 micron technology
- 100-pin MQFP package
- 100-pin LQFP package

Description

The CS7410 is a true system-on-a-chip for the CD-based digital audio market. With a powerful RISC processor, one DSP, integrated audio ΔΣ modulator, large internal SRAM and program ROM, and glueless interface to popular CD chip sets, the CS7410 is a complete single chip low-power programmable audio decoder. This powerful architecture is easily capable of MP3, WMA, and other future audio formats. The CS7410's flexible architecture and low power consumption make it an ideal low-cost solution for a wide range of player applications. For portable audio systems, the memory interface can be used to add DRAM or SRAM for Electronic Shock Protection (ESP). A flexible set of interfaces are available for end-user I/O such as a keypad and LCD control for use in mass market CD players, boom boxes, and shelf-top systems.

ORDERING INFORMATION

CS7410-CM	0° to 70° C	100-pin MQFP
CS7410-CQ	0° to 70° C	100-pin LQFP



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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http://www.cirrus.com/corporate/contacts/sales.cfm

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1. CHARACTERISTICS AND SPECIFICATIONS

1.1 AC AND DC PARAMETRIC SPECIFICATIONS

(AGND, DGND=0V, all voltages with respect to 0V)

1.1.1 Absolute Maximum Rating

Symbol	Description	Min.	Max.	Unit
VDD_{IO}	Power Supply Voltage on I/O ring	-0.5	4.6	Volts
VDD_{CORE}	Power Supply Voltage on core logic and PLL	-0.5	2.5	Volts
V_I	Digital Input Applied Voltage (power applied)	-0.5	5.5	Volts
I_I	Digital Input Forced Current	-10	10	mA
I_O	Digital Output Forced Current	-50	50	mA
T_{SOL}	Lead Soldering Temperature		260	^oC
T_{VSOL}	Vapor Phase Soldering Temperature		235	^oC
T_{STOR}	Storage Temperature (no power applied)	-40	125	^oC
T_{AMB}	Ambient Temperature (power applied)	0	70	^oC
P_{TOT}	Power consumption		1	W

CAUTION: Operating beyond these Minimum and Maximum limits can result in permanent damage to the device. Cirrus Logic recommends that CS7410 devices operate at the settings described in the next table.

1.1.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage, IO	V_{DD}	3.0	3.3	3.6	Volts
Supply Voltage, core and PLL	V_{DD}	1.62	1.8V	1.98	Volts
Ambient Temperature (power applied)	T_{AMB}	0	25	70	^oC

1.1.3 Electrical Specifications

(TA = 0 to 70 ^oC)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Current, IO	I_{DD}	Normal Operating		13		mA
Supply Current, core and PLL	I_{DD}	Normal Operating		70		mA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Digital Pins						
Input Voltage, High	V_{IH}		2.0			Volts
Input Voltage, Low	V_{IL}				0.8	Volts
Input Current	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS}	-1		+1	µA
Input Pull up/down resistor	R_I			75		KΩ
Output Voltage, High	V_{OH}	@ buffer rating	2.4			Volts
Output Voltage, Low	V_{OL}	@ buffer rating			0.4	Volts
High-Z-state Leakage	I_{OZ}	$V_{OUT} = V_{SS}$ or V_{DD}	-1		+1	µA

1.1.4 DC CHARACTERISTICS

(TA= 25°C; VDD_PLL=VDD_CORE=1.8V±10%, VDD_IO=3.3V±10%)

1.1.4.1 SDRAM Interface

Symbol	Description	Min	Typ	Max	Unit
t_{mper}	DR_CKO Period	22			ns
t_{mco}	Output Delay from DR_CKO active edge			19	ns
t_{mdow}	M_D[15:0] delay from DR_CKO			19	ns
t_{mhw}	M_D[15:0] valid time after DR_CKO	5			ns
t_{msur}	M_D[15:0] setup to DR_CKO	13			ns
t_{mhr}	M_D[15:0] hold time after DR_CKO	0			ns

Table 1. SDRAM Characterization Data

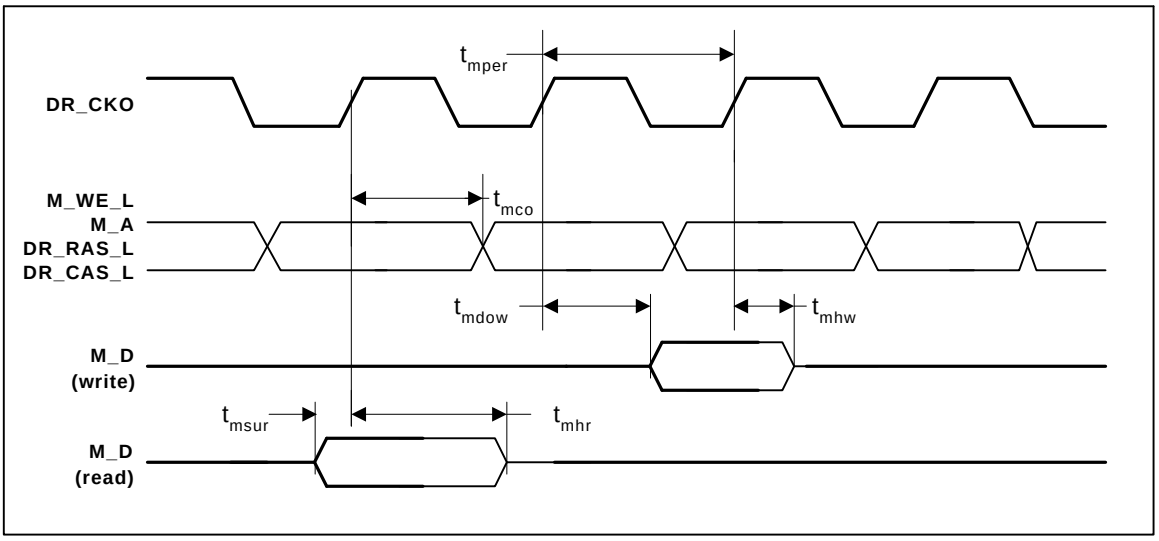


Figure 1. SDRAM Timing

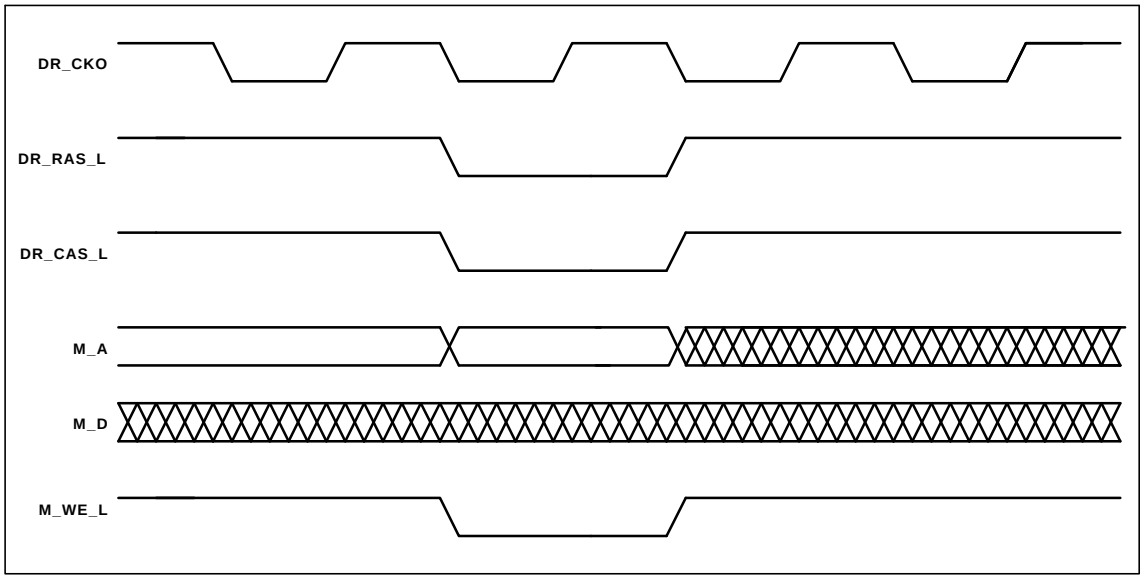


Figure 2. SDRAM Load Mode

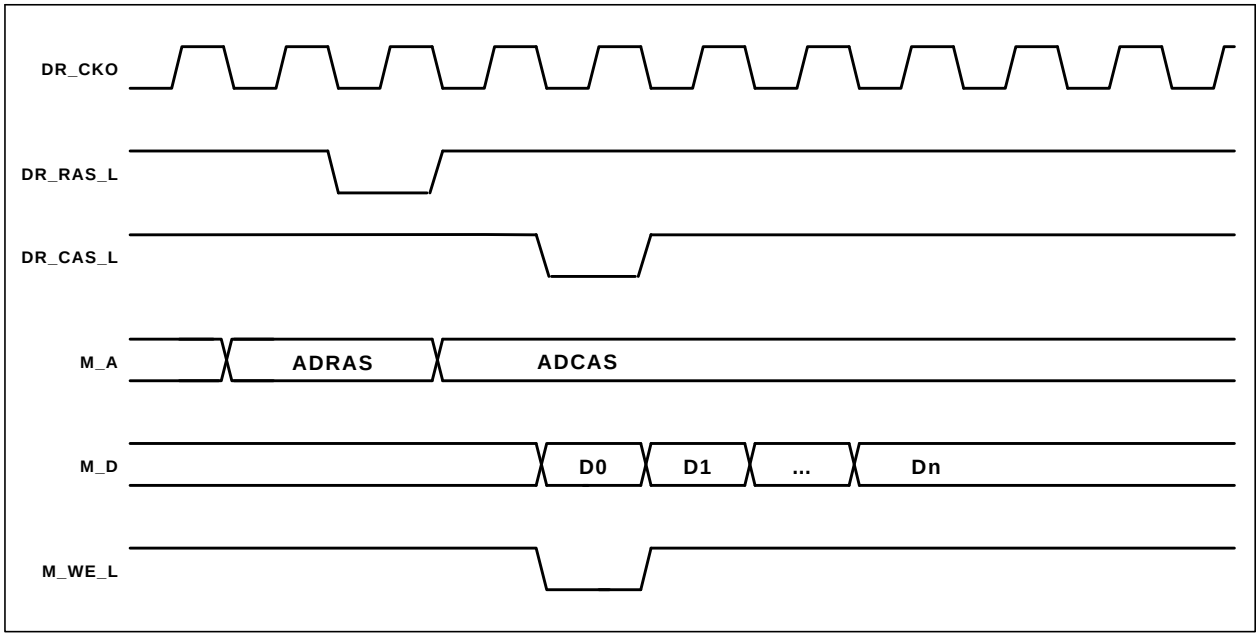


Figure 3. SDRAM Burst Write

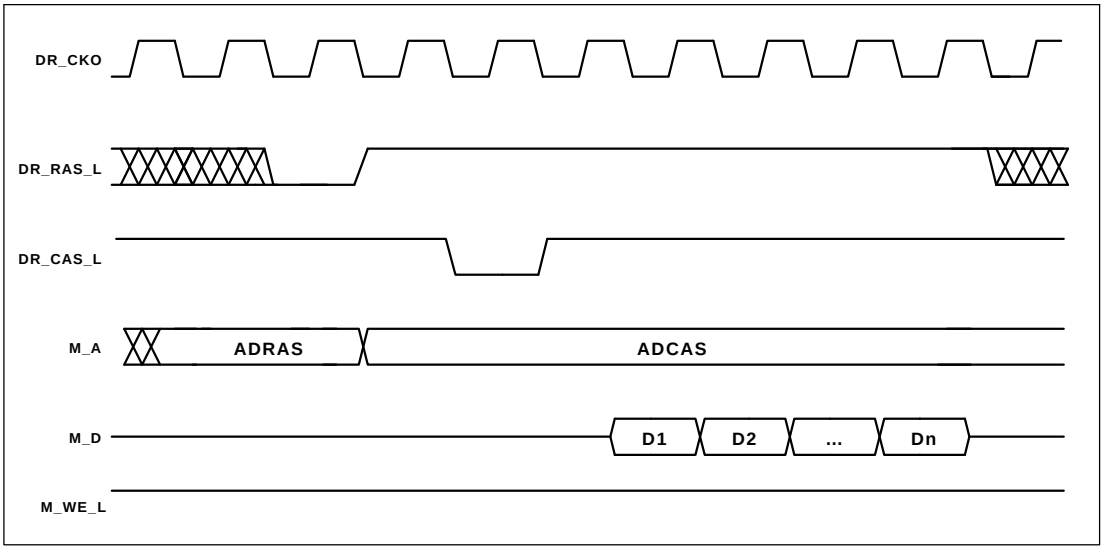


Figure 4. SDRAM Burst Read

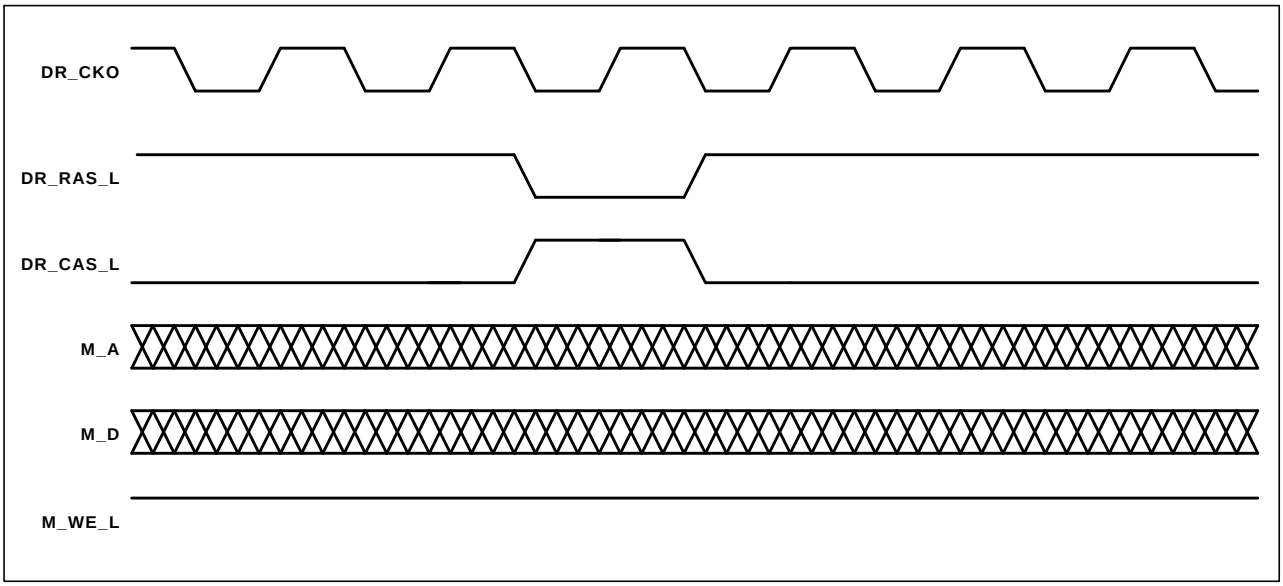


Figure 5. SDRAM Refresh

1.1.4.2 Serial Interface

Symbol	Description	Min	Typ	Max	Unit
t_{clk_per}	Clock period	66			ns
t_{DMs}	Master-mode data setup	28			ns
t_{DMh}	Master-mode data hold	28			ns
t_{DSs}	Slave-mode data setup	15			ns
t_{CMs}	Master chip select to clock setup	28			ns
t_{DSh}	Slave mode data hold	0			ns

Table 2. Serial Interface Characterization Data

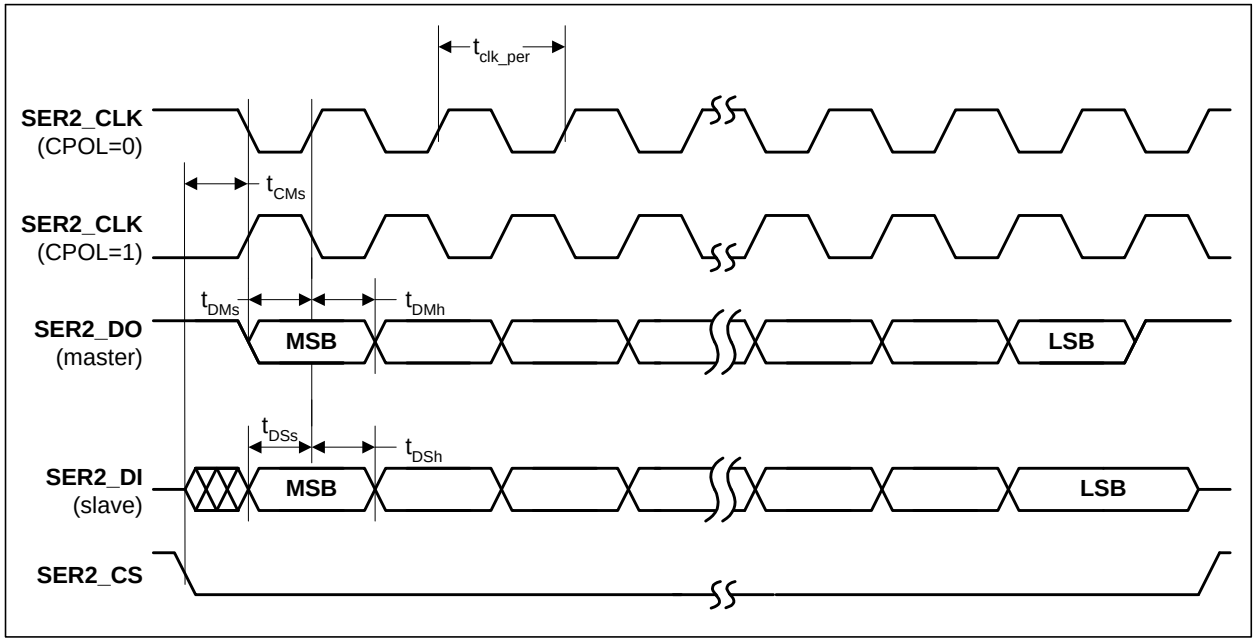


Figure 6. Serial Interface Timing Diagram

1.1.4.3 EDO DRAM interface

Symbol	Description	Min	Typ	Max	Unit
^tRAS	RAS low time	72			ns
^tRP	RAS high pulse time	40			ns
^tRCL	RAS fall to CAS fall	38			ns
^tCAS	CAS low time	30			ns
^tCPN	CAS high time	15			ns
^tCAH	CAS fall to address row	29			ns
^tASR	Address row to RAS fall	10			ns
^tRAH	RAS fall to address column	18			ns
^tASC	second address column (burst) to CAS fall	10			ns
^tAA	Column address to data setup			35	ns
^tCAC	CAS fall to data setup			17	ns
^tCSR	CAS fall to RAS fall	19			ns
^tCHR	RAS fall to CAS rise	18			ns
^tCRH	CAS rise to RAS rise	6			ns
^tWDS	Write data setup to CAS fall	12			ns
^tWDH	Write data hold to CAS fall	29			ns
^tWS	Write enable setup to CAS fall	13			ns
^tWH	Write enable hold to CAS fall	20			ns
^tROE	RAS fall to OE fall	-5		5	ns
^tOER	RAS rise to OE rise	-5		5	ns
^tDCH	Read data hold to CAS rise	0			ns

Table 3. EDO DRAM Characterization Data

Note:Values shown are for minimum internal clock period (11ns) and all programmed wait states enabled.

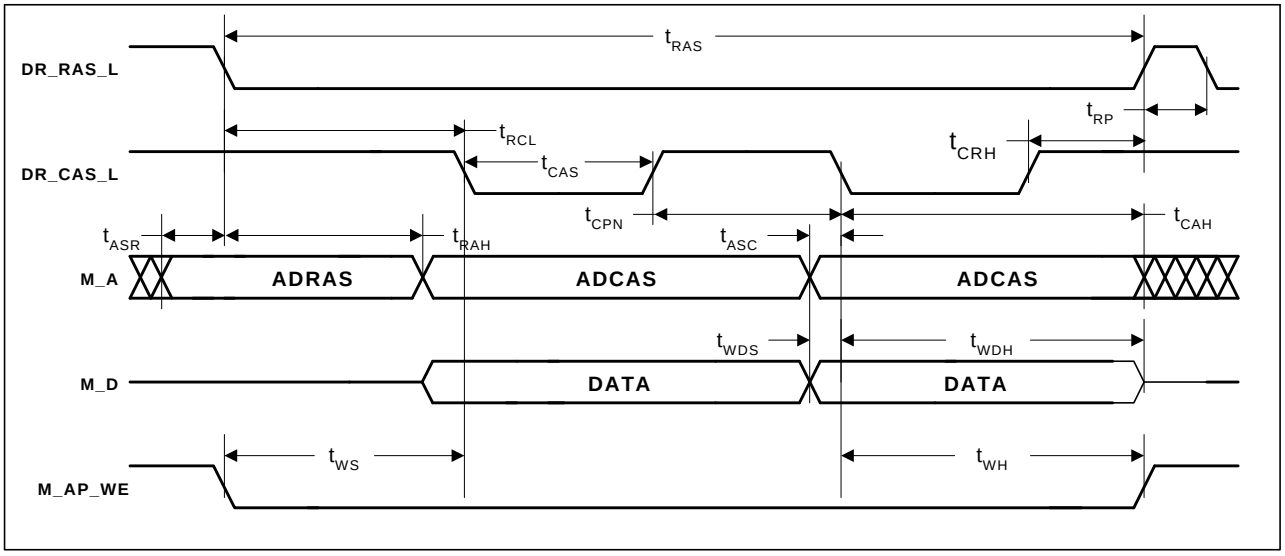


Figure 7. EDO Page Write Timing Diagram

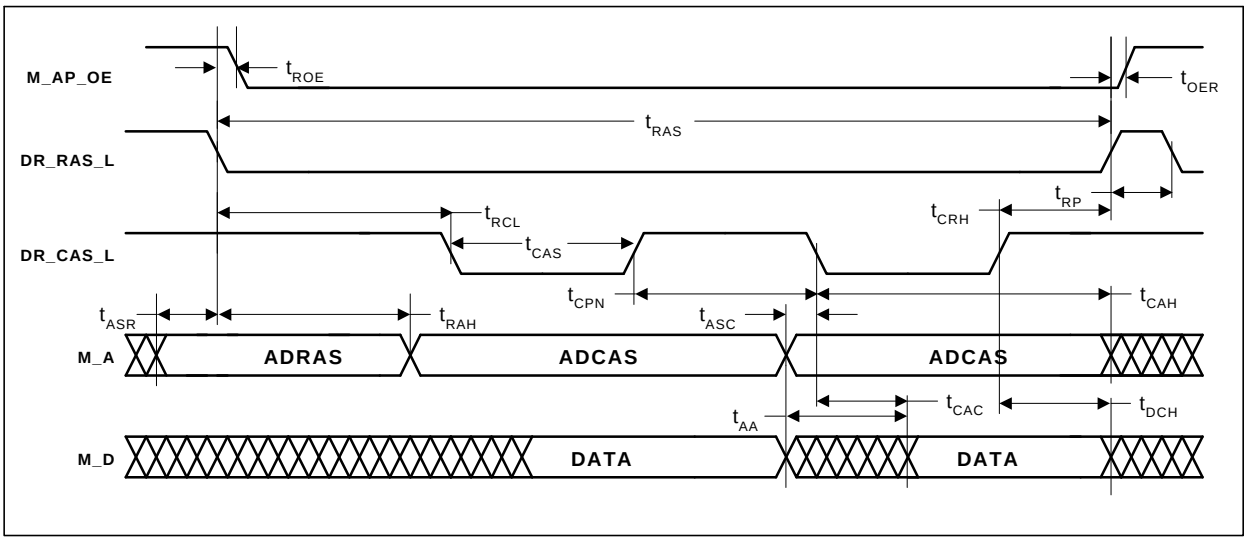


Figure 8. EDO Page Read Timing Diagram

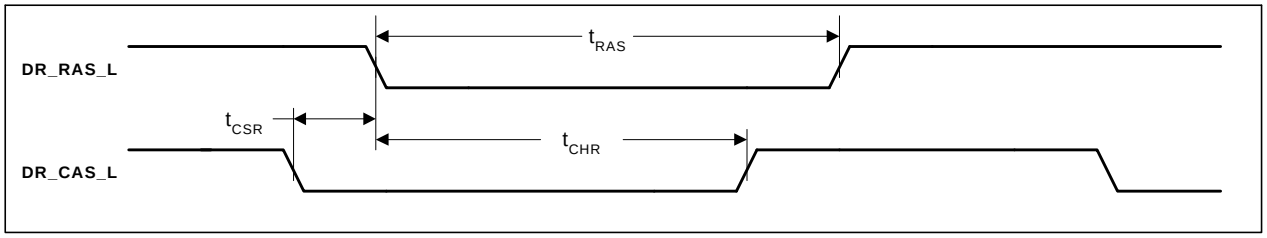


Figure 9. EDO Refresh Timing Diagram

1.1.4.4 FLASH / ROM Interface

Symbol	Description	Min	Typ	Max	Unit
^{t}CSpw	CE low period	135			ns
^{t}RDd1	CE fall to output enable fall	5			ns
^{t}RDd2	CE rise to output enable rise	-5		5	ns
^{t}ADs	Address setup to CE fall	-10		10	ns
^{t}DAs	Data setup after address[1]			28	ns
^{t}WRSU	All outputs setup before WE	95			ns
^{t}WRPW	WE pulse width	170			ns
^{t}WRH	All outputs hold after WE	95			ns

Table 4. FLASH/ROM Read Characterization Data

1. Value shown for 3 programmed wait states.

Note:Values shown are for minimum internal clock period (11ns) and no programmed wait states.

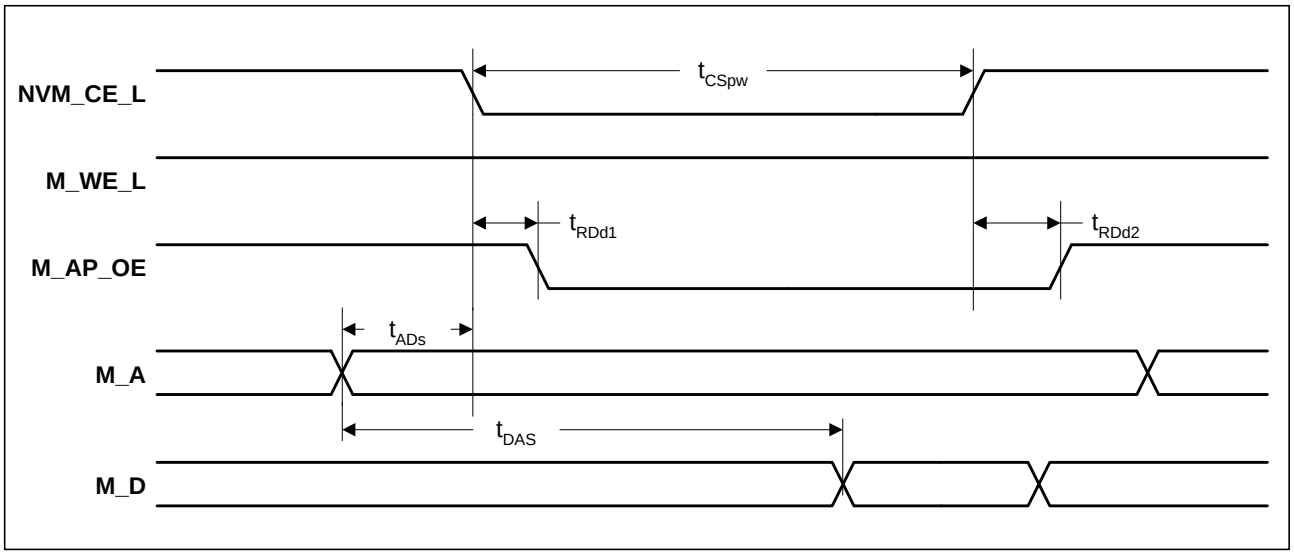


Figure 10. FLASH/ROM Read

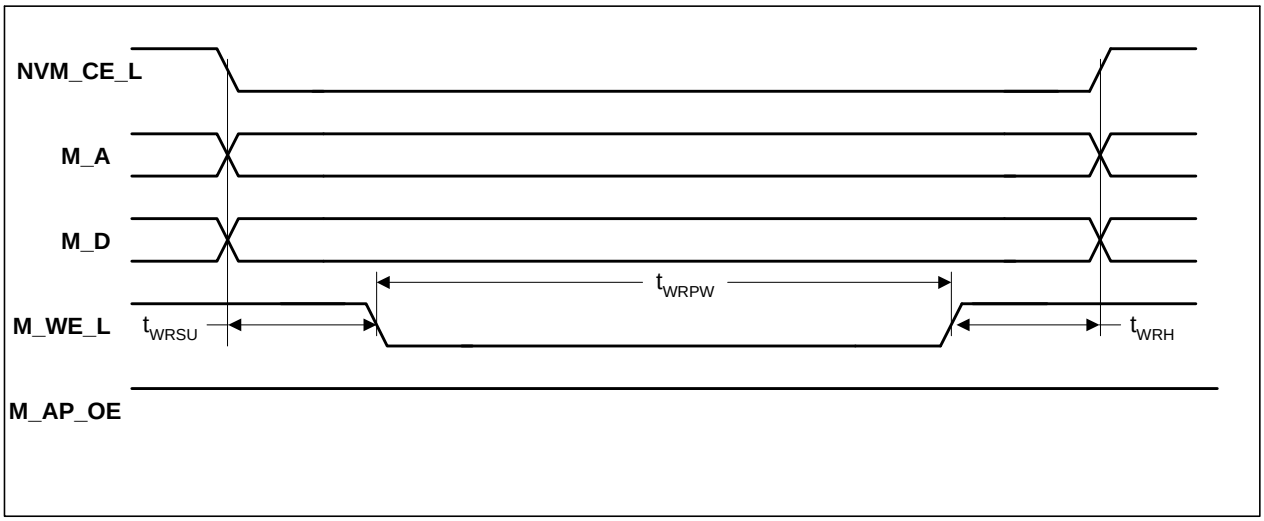


Figure 11. FLASH/ROM Write

1.1.4.5 Audio Output Interface

Symbol	Description	Min	Typ	Max	Units
t_{axch}	PCM_XCLK High Time (PCM_XCLK is Input/Output)	42	50		%
t_{axcl}	PCM_XCLK Low Time (PCM_XCLK is Input/Output	42	50		%
t_{axper}	PCM_XCLK period (Input/Output)	55			ns
t_{aoper}	PCM_BCK period (Output)	440			ns
t_{sdmo}	PCM_BCK delay from PCM_XCLK output transition[1]			5	ns
t_{sdmi}	PCM_BCK delay from PCM_XCLK input transition[1]			15	ns
t_{lrds}	PCM_LRCK delay from PCM_BCK transition[1]			5	ns
t_{adsm}	PCM_D[3:0] delay from PCM_BCK transition[1]			5	ns

Table 5. Audio Output Interface Symbols and Characterization Data

1. Active clock edge is programmable. Timing is referenced from the active edge.

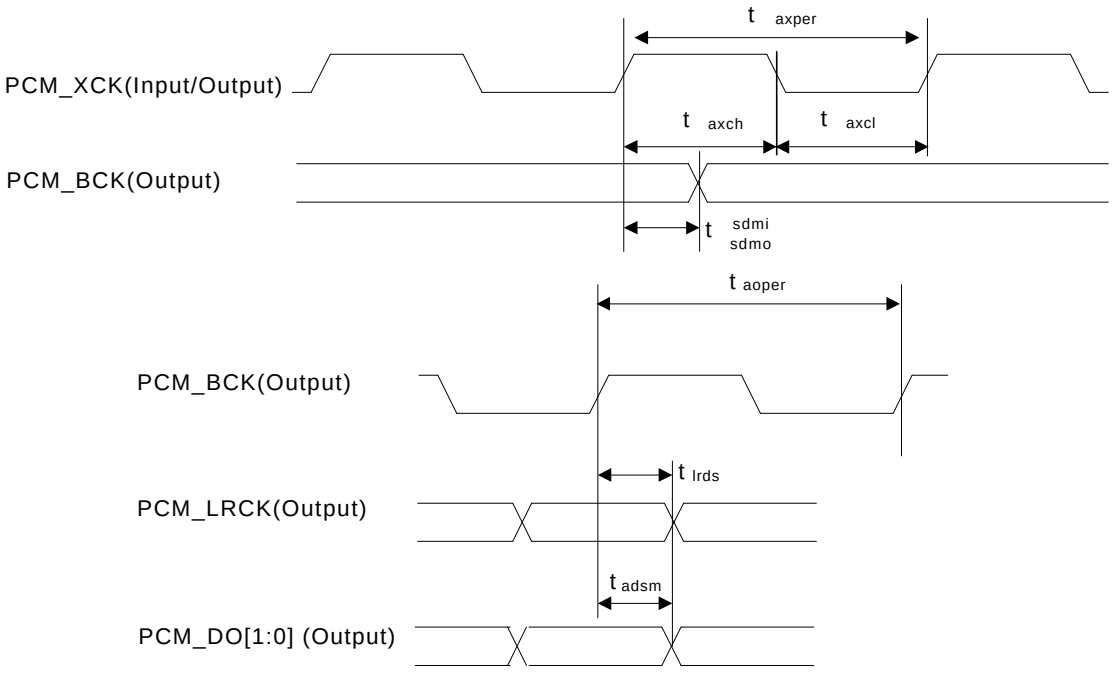


Figure 12. Audio Output Timing

1.1.4.6 CD Interface

Symbol	Description	Min	Typ	Max	Units
t_{slri}	CD_LRCK setup to CD_BCK active edge	7			ns
t_{sdi}	CD_DATA and CD_C2P0 setup to CD_BCK active edge	7			ns
t_{hsdi}	CD_DATA and CD_C2P0 hold time after CD_BCK active edge	3			ns

Note:Active edge of CD_BCLK is programmable

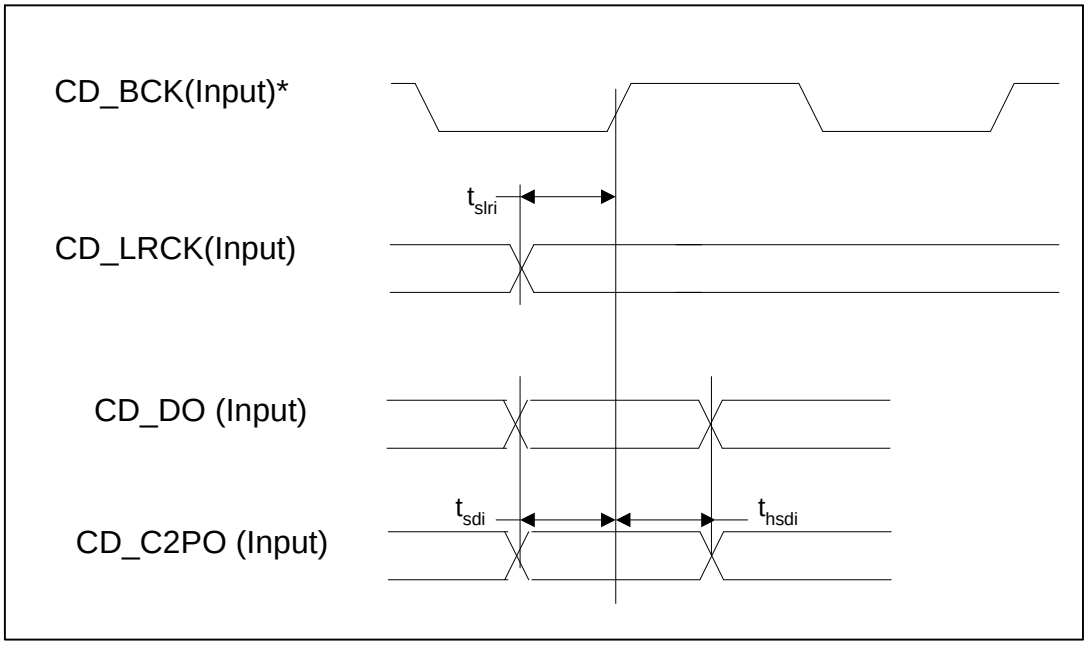
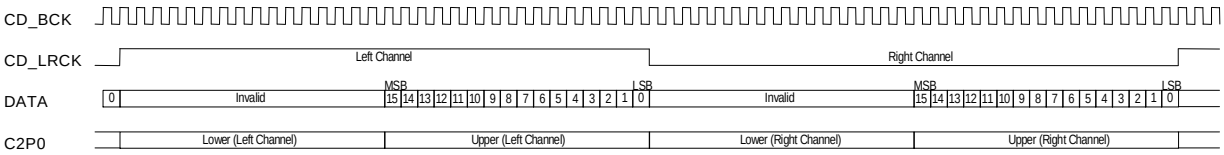
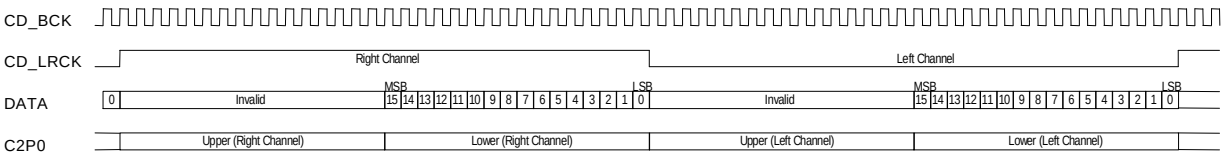


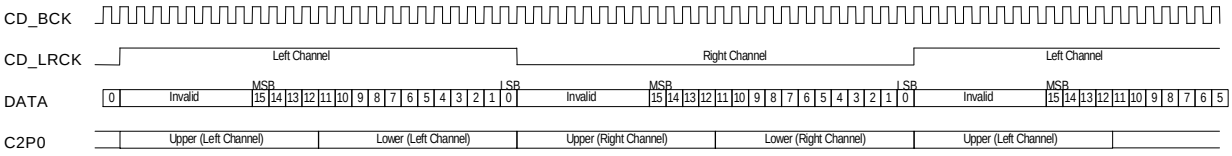
Figure 13. CD Interface Timing



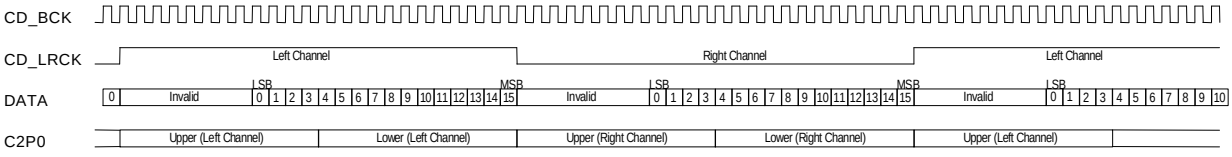
32-bit BCK, MSB First, Right Channel Low, C2P0 LSB First, Data latch timing high



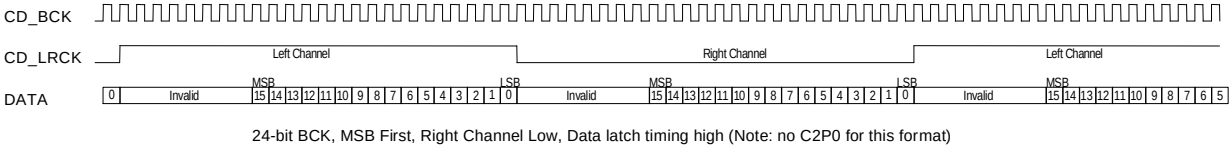
32-bit BCK, MSB First, Left Channel Low, C2P0 MSB First, Data latch timing low



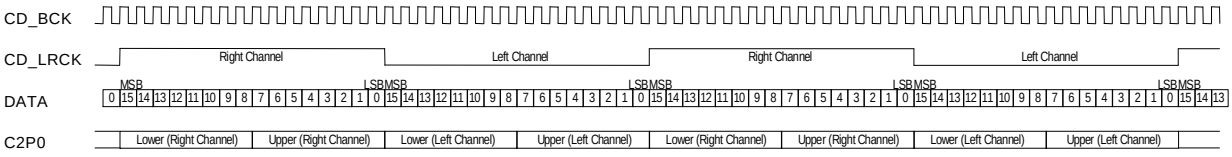
24-bit BCK, MSB First, Right Channel Low, C2P0 MSB First, Data latch timing high



24-bit BCK, LSB First, Right Channel Low, C2P0 MSB First, Data latch timing low



24-bit BCK, MSB First, Right Channel Low, Data latch timing high (Note: no C2P0 for this format)



16-bit BCK, MSB First, Left Channel Low, C2P0 LSB First, Data latch timing high

Figure 14. CD Interface Timing Diagrams

1.1.4.7 Miscellaneous Timings

Symbol	Description	Min	Typ	Max	Unit
t_{xclper}[1]	XTLCLK period		59.05		ns
t_{rstl}	RST_N Low Pulse Width	1000			ns
t_{gph}	GPIO PW High	50			ns
t_{gpl}	GPIO PW Low	50			ns

1. Value represents typical application with 16.934 MHz crystal

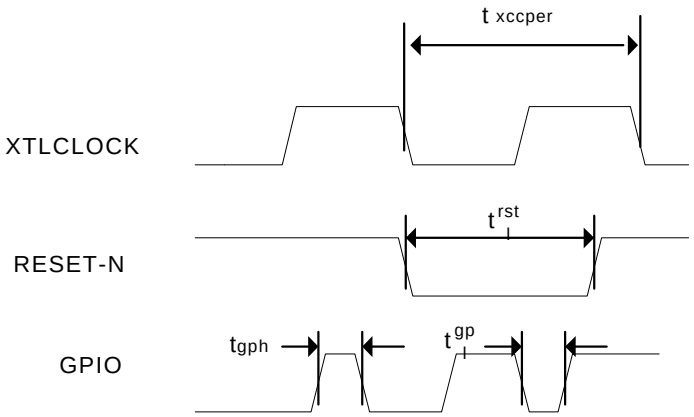


Figure 15. Miscellaneous Timings

2. CS7410 SUMMARY

2.1 CS7410 Typical Application

Figure 16 shows an example of a complete audio player using the CS7410.

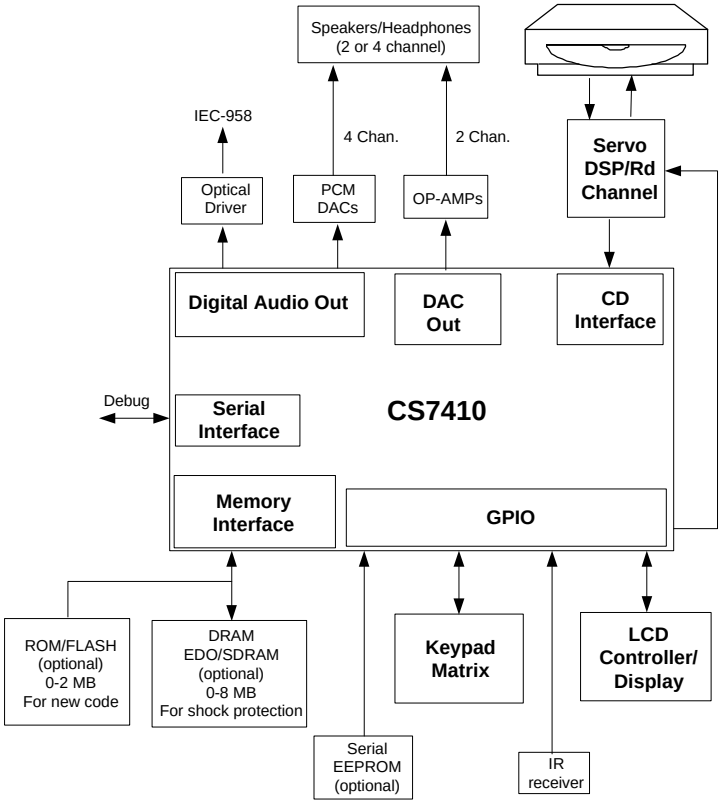


Figure 16. CS7410 Application

2.2 CS7410 Block Summaries

2.2.1 RISC-32

- Powerful 32-bit RISC processor
- Comprehensive development tool support
- Big or little endian data formats supported
- 32x32 (64-bit result) MAC, 2 cycles / multiply with C support
- 4 Kbyte instruction cache, 2 Kbyte data cache
- Single cycle instructions, runs up to 90 MHz

2.2.2 DSP-16

- Powerful 16-bit DSP processor
- 16-bit fixed point logic, with 36 bit accumulator.
- Single-cycle throughput, 2-cycle latency multiply accumulate, 16-bit simple integer logic
- 512 byte instruction cache, 8 Kbyte program visible local memory
- Single cycle instructions, runs up to 90 MHz
- DSP MAC is pipelined, 1 cycle / multiply

2.2.3 System Controls

- Includes 32 hardware lockable semaphore registers
- Two general-purpose registers for inter-proces-

sor communication
- Three 32-bit timers for I/O and other uses, with programmable interval rates
- "Getbits" module accelerates peripheral stream parsing
- Both hardware and software interrupts on data or debug

2.2.4 Memory System

- Large internal SRAM (80 Kbyte) and internal program ROM (256 Kbyte)
- Supports both Synchronous and EDO DRAM (256 KBytes to 8 MBytes) for ESP
- Supports one bank of FLASH and ROM (up to 2 MBytes) for nonvolatile storage
- 4-, 8-, or16-bit data bus for DRAM, 8-bit data bus for ROM

2.2.5 CD Interface

- Glueless interfaces to CD servo chip set, supporting all standard CD formats
- Includes pattern matching hardware to support fast ESP recovery

2.2.6 Audio Interface

- Supports 4 channels PCM, I^2S connectivity at up to 24 bits
- Flexible audio clocking scheme using internal PLL and dividers, or external pins
- Simultaneous IEC-958 output with programmable channel status and user data
- Integrated sigma-delta (ΔΣ) stereo audio modulator

2.2.7 External Interface

- 2-wire serial slave port, used for debug
- 3- or 4-wire synchronous serial master/slave port for external controller or slave peripheral
- Separate synchronous serial master port optimized for receiving CD sub-codes
- Up to 29 programmable bi-directional I/O (GPIO) and up to 9 output only (GPO) pins (some multiplexed with other peripherals)
- All pins defined as GPIOs can be used to receive edge or level detection interrupts.
- Pulse-width modulated (PWM) output pin can be used to create simple ADC using low-cost comparator (i.e., for battery voltage monitor)

2.2.8 System Functions

- Internal oscillator uses external crystal, or receives clock (i.e. 16.9 MHz) from CD servo
- Internal PLL generates any system clock frequency, chip can run up to 90 MHz
- Includes clock divider and clock shutoff circuits for low power/sleep modes
- Advanced 0.18 micron CMOS technology, runs off 1.8 V and 3.3 V
- All I/O pins are 3.3 V, with 5 V tolerance
- 100-pin MQFP package
- 100-pin LQFP package

3. FUNCTIONAL DESCRIPTION

3.1 RISC-32 Processor

The CS7410 includes a powerful, proprietary 32-bit RISC processor backed by powerful software development tools. The RISC-32 has a MAC engine which performs multiply/accumulate in 2 cycles with C support, effectively achieving single cycle throughput.

There are other instructions that are designed to help with performing audio decoding. The RISC processor coordinates on-chip multi-threaded tasks, as well as supervises system activities such as keypad and front panel display control.

3.2 DSP-16 Processor

The CS7410 contains a proprietary digital signal processor (DSP) called DSP-16, which is optimized for audio and sound applications. In the CS7410, the DSP-16 assists with audio decoding and provides added functions such as surround sound and equalization. The DSP performs 16-bit simple integer operations, and has a 16-bit fixed point logic unit with a 32-bit accumulator.

There are 24 general-purpose registers, and eight independent address generation registers, featuring: post-increment ALU, linear and circular buffer operations, bit reverse ALU operations, and dual operand read from memory. The multiply-accumulator has single-cycle throughput, with two cycle latency. The DSP is optimized for bit packing and unpacking operations. The interface to main memory is designed for bursting flexible block sizes and skip counts.

3.3 Memory Control

The Memory Controller performs the arbitration functions for all the other modules in the CS7410, allowing access to internal ROM and SRAM, and to external ROM and DRAM. The Memory Controller services and arbitrates a number of clients and stores their code and/or data within the local memory. This arbitration and scheduling guarantees the allocation of sufficient bandwidth to the various clients. An optimal application will use only internal ROM and SRAM for code and data storage, which results in the best timing and lowest power consumption.

External DRAM may be used for runtime code storage or for ESP RAM. In both of these applications, the data throughput requirement is low, and the Memory Controller acts as a DMA engine to move data between external and internal memory with minimal power consumption. The internal ROM contains most of the code required for audio decoding and system functions.

Additional code can be stored in external ROM (managed by the Memory Controller) or a small serial ROM (controlled by GPIOs). The CS7410 also supports code storage in external FLASH with in-system write capability for customer code updates. Future firmware releases will provide a complete solution requiring no external ROM.

3.4 CD Interface

The CD Interface receives compressed or uncompressed (direct audio) data from the CD servo/read channel chip, performs descrambling and CRC checking, and writes the data to an internal FIFO. Additional C3 error decoding is done in software. The CD interface is compatible with all commonly used CD formats.

The CS7410 contains a hardware pattern matching circuit to scan the incoming CD data for a pattern of up to 64 bytes. This circuit is used to assist the Electronic Shock Protection function by quickly locating and matching the incoming data with data stored in the ESP RAM.

3.5 System Control Functions

The system control functions are used to coordinate the activities of the multiple processors, and to provide the supporting system operations. Two 32-bit communication registers are available for inter-

processor communication, and 32 semaphore registers are used for resource locking. Three timers are available for general-purpose functions, as well as more specialized functions, such as watchdog timers and performance monitoring.

The large number of general purpose I/Os offers flexibility in system configurations. Three separate synchronous serial interfaces, conforming to industry-standard protocols, are available for a variety of system interface functions. Four general purpose software interrupts and twelve hardware interrupts help reduce peripheral overhead and improve UI responsiveness. Power-down control of the internal clocks is also possible. An internal PLL is used to generate the internal system and memory clocks as well as audio clocks for all supported sample rates.

3.6 Audio Output

Decoded audio data is written into an output FIFO in 16-, 18-, 20- or 24-bit PCM format. A flexible audio output stage can simultaneously output 4 channels of PCM data to external audio DACs, plus an independent IEC-958 encoded output. The IEC-958 output has fully programmable channel status (commercial), and provides a flexible solution to support all IEC-958 modes for user data. The audio output circuit contains an auto-mute detect circuit, which can generate internal or external mute controls

PCM FIFO data up to 18 bits can also be output by the on-board sigma-delta stereo modulator. The sigma-delta modulator yields a typical 85 dB signal-to-noise ratio with few external components required, resulting in a low-cost, low parts count analog front end. The modulator has a 32x upsampling filter, followed by a 32x interpolator, and finally a 5^{th}-order Sigma-Delta modulator. The auto-mute circuit also works on the modulator output, and there are separate programmable attenuators for the modulator output and both PCM outputs.

4. PIN DESCRIPTION

4.1 Pin Identification

Figure 17 shows the CS7410 pins grouped by function, also showing the number of pins in each group.

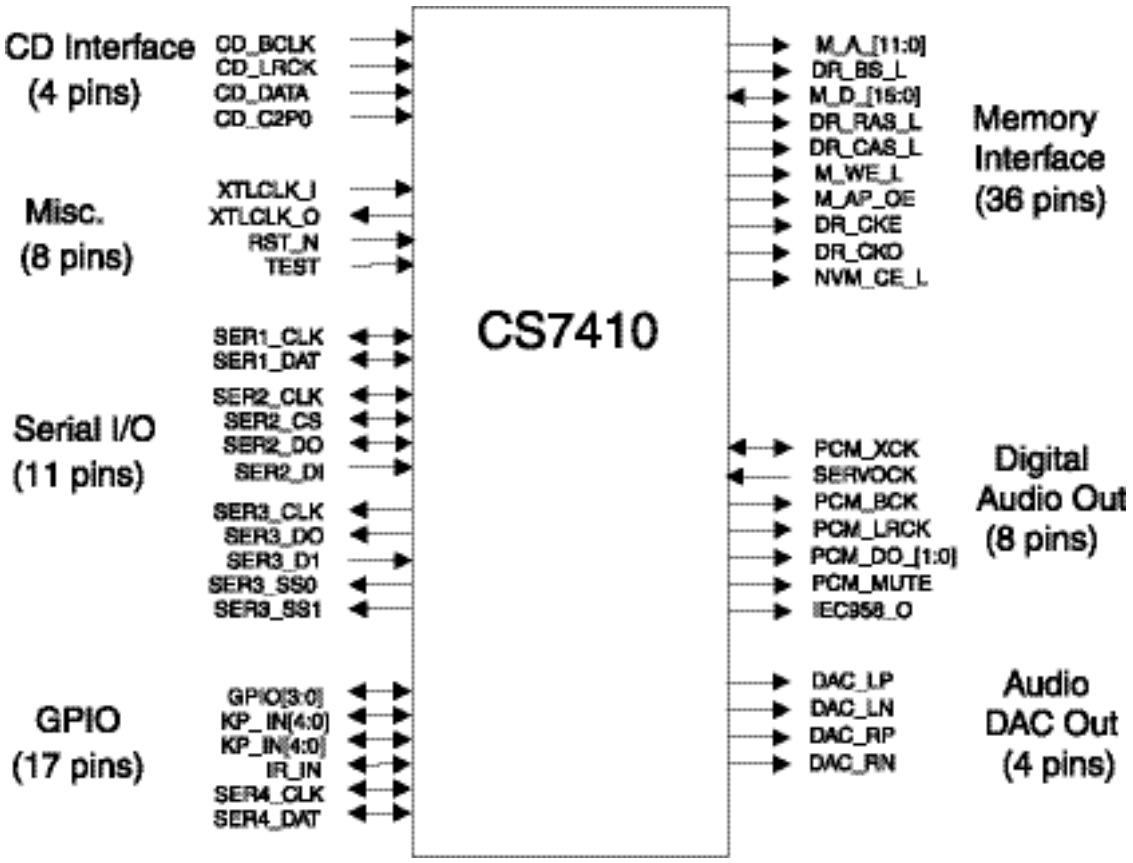


Figure 17. CS7410 Pin Identification

Table 6 lists the conventions used to identify the pin type and direction.pin assignments.

I: Input
S: Schmitt trigger on input
U: Pull up resistor
O: Output
O4: Output – 4mA drive
T4: High Z output – 4mA drive
B: Bi-direction
B4: Bi-direction – 4mA drive
D4: Bi-direction with 4mA open drain output

Table 6. Pin Type and Direction Legend

Pwr: +2.5V or +3.3V power supply voltage
Gnd: Power supply ground
Name_N: Low active
Name_L: Low active

Table 6. Pin Type and Direction Legend (Continued)

Table 7 lists the pin number, pin name, and pin type for the 100-pin CS7410 package. For signal pins, the pin direction after reset is shown. The primary function and pin direction is shown for all signal pins. For some signal pins, a secondary function and direction are also shown.

Pin	Name	Type	Reset	Function #1	Dir	Function #2	Dir	Note
1	PLL_GND	Gnd		PLL Ground				
2	PLL_1V8	Pwr		PLL Power				
3	M_D_15	B4	I	DRAM Data[15]	B	NVMem Address[19]	O	
4	M_D_14	B4	I	DRAM Data[14]	B	NVMem Address[18]	O	
5	M_D_13	B4	I	DRAM Data[13]	B	NVMem Address[17]	O	
6	M_D_12	B4	I	DRAM Data[12]	B	NVMem Address[16]	O	
7	M_D_11	B4	I	DRAM Data[11]	B	NVMem Address[15]	O	
8	M_D_10	B4	I	DRAM Data[10]	B	NVMem Address[14]	O	
9	M_D_9	B4	I	DRAM Data[9]	B	NVMem Address[13]	O	
10	M_D_8	B4	I	DRAM Data[8]	B	NVMem Address[12]	O	
11	M_D_7	B4	I	DRAM Data[7]	B	NVMem Data[7]	B	
12	CORE_1V8	Pwr		Core Power				
13	M_D_6	B4	I	DRAM Data[6]	B	NVMem Data[6]	B	
14	CORE_GND	Gnd		Core Ground				
15	M_D_5	B4	I	DRAM Data[5]	B	NVMem Data[5]	B	
16	IO_3V3	Pwr		I/O Power				
17	XTLCLK_O	O	O	Oscillator Out	O			

Table 7. Pin Assignments

Pin	Name	Type	Reset	Function #1	Dir	Function #2	Dir	Note
18	XTLCLK_I	I	I	Oscillator In	I			
19	IO_GND	Gnd		I/O Ground				
20	M_D_4	B4	I	DRAM Data[4]	B	NVMem Data[4]	B	
21	M_D_3	B4	I	DRAM Data[3]	B	NVMem Data[3]	B	
22	M_D_2	B4	I	DRAM Data[2]	B	NVMem Data[2]	B	
23	M_D_1	B4	I	DRAM Data[1]	B	NVMem Data[1]	B	
24	M_D_0	B4	I	DRAM Data[0]	B	NVMem Data[0]	B	
25	M_A_11	B4	I	DRAM Address[11]	O	NVMem Address[11]	O	1
26	M_A_10	B4	I	DRAM Address[10]	O	NVMem Address[10]	O	1
27	M_A_9	B4	I	DRAM Address[19]	O	NVMem Address[9]	O	1
28	M_A_8	B4	I	DRAM Address[8]	O	NVMem Address[8]	O	1
29	M_A_7	B4	I	DRAM Address[7]	O	NVMem Address[7]	O	1, 3
30	M_A_6	B4	I	DRAM Address[6]	O	NVMem Address[6]	O	1, 3
31	M_A_5	B4	I	DRAM Address[5]	O	NVMem Address[5]	O	1, 3
32	M_A_4	B4	I	DRAM Address[4]	O	NVMem Address[4]	O	1, 3
33	M_A_3	B4	I	DRAM Address[3]	O	NVMem Address[3]	O	1, 3
34	M_A_2	T4	I	DRAM Address[2]	O	NVMem Address[2]	O	3
35	M_A_1	T4	I	DRAM Address[1]	O	NVMem Address[1]	O	3
36	M_A_0	T4	I	DRAM Address[0]	O	NVMem Address[0]	O	3
37	DR_RAS_L	T4	I	DRAM RAS_L	O			
38	CORE_1V8	Pwr		Core Power				
39	DR_CAS_L	T4	I	DRAM CAS_L	O			

Table 7. Pin Assignments (Continued)

Pin	Name	Type	Reset	Function #1	Dir	Function #2	Dir	Note
40	CORE_GND	Gnd		Core Ground				
41	M_WE_L	T4	I	DRAM WE_L	O	NVM_WE_L		
42	IO_GND	Gnd		I/O Ground				
43	DR_CKO	T4	I	SDRAM CKO	O			
44	IO_3V3	Pwr		I/O Power				
45	DR_CKE	T4	I	SDRAM CKE	O			
46	DR_BS_L	B4	I	SDRAM BS_L	O	NVMem Address[20]		1
47	M_AP_OE	B4	I	SDRAM AP, EDO DRAM OE_L	O	NVM_ OE_L		1
48	NVM_CE_L	T4	I	NVM_CE_L	O			
49	KP_IN_0	B4U	I	GPIO[19]	B			
50	KP_IN_1	B4U	I	GPIO[20]	B			
51	KP_IN_2	B4U	I	GPIO[21]	B			
52	KP_IN_3	B4U	I	GPIO[22]	B			
53	KP_IN_4	B4U	I	GPIO[23]	B			
54	KP_OUT_0	B4	I	GPIO[24]	B			
55	KP_OUT_1	B4	I	GPIO[25]	B			
56	KP_OUT_2	B4	I	GPIO[26]	B			
57	KP_OUT_3	B4	I	GPIO[27]	B			
58	KP_OUT_4	B4	I	GPIO[28]	B			
59	IR_IN	B4S	I	GPIO[4]	B			
60	SER1_CLK	D4S	I	Debug Port Clock	B			
61	SER1_DAT	D4S	I	Debug Port Data	B			
62	SER4_CLK	B4S	I	GPIO[5]	B			
63	SER4_DAT	B4S	I	GPIO[6]	B			
64	IO_GND	Gnd		I/O Ground				
65	SER2_CLK	B4	I	Serial2 Clock	B	GPIO[7]	B	
66	SER2_DI	B4	I	Serial2 Data In	B	GPIO[8]	B	
67	SER2_DO	B4	I	Serial2 Data Out	B	GPIO[9]	B	

Table 7. Pin Assignments (Continued)

Pin	Name	Type	Reset	Function #1	Dir	Function #2	Dir	Note
68	SER2_CS	B4	I	Serial2 Chip Select	B	GPIO[10]	B	
69	SER3_CLK	B4	I	Serial3 Clock	O	GPIO[11]	B	
70	SER3_DO	B4	I	Serial3 Data Out	O	GPIO[12]	B	
71	CORE_1V8	Pwr		Core Power				
72	SER3_DI	B4	I	Serial3 Data In	I	GPIO[13]	B	
73	CORE_GND	Gnd		Core Ground				
74	SER3_SS0	B4	I	Serial3 Chip Select0	O	GPIO[14]	B	
75	IO_3V3	Pwr		I/O Power				
76	SER3_SS1	B4	I	Serial3 Chip Select1	O	GPIO[15]	B	
77	SERVOCK	B4	I	Servo Clock In	I	GPIO[17]	B	
78	PCM_XCK	B4	I	PCM_XCK	B			
79	PCM_MUTE	B4	I	PCM_MUTE	O	GPO[4]	O	1
80	CD_C2P0	B4	I	CD_C2P0	I	GPIO[16]	B	
81	CD_BCLK	IS	I	CD_BCLK	I			
82	CD_LRCK	I	I	CD_LRCK	I			
83	CD_DATA	I	I	CD_DATA	I			
84	DAC_LP	O4	O	ΔΣ DAC Left Positive Out	O	GPO[5]	O	
85	DAC_LN	O4	O	ΔΣ DAC Left Negative Out	O	GPO[6]	O	
86	IO_GND	Gnd		I/O Ground				
87	DAC_RP	O4	O	ΔΣ DAC Right Positive Out	O	GPO[7]	O	
88	DAC_3V3	Pwr		ΔΣ DAC I/O Power				
89	DAC_RP	O4	O	ΔΣ DAC Right Negative Out	O	GPO[8]	O	
90	RST_N	IS	I	Reset_L	I			
91	TEST	I	I	Manufacturing Test	I			
92	PCM_BCK	B4	O	PCM_BCK	O	GPO[0]	O	1
93	PCM_LRCK	B4	O	PCM_LRCK	O	GPO[1]	O	1
94	PCM_DO_0	B4	O	PCM_Dout[0]	O	GPO[2]	O	2
95	PCM_DO_1	B4	O	PCM_Dout[1]	O	GPO[3]	O	1
96	IEC958_O	B4	I	IEC-958 Out	O	GPIO[18]	B	
97	GPIO_0	B4	I	GPIO[0]	B			

Table 7. Pin Assignments (Continued)

Pin	Name	Type	Reset	Function #1	Dir	Function #2	Dir	Note
98	GPIO_1	B4	I	GPIO[1]	B	PWM_Out	O	
99	GPIO_2	B4	I	GPIO[2]	B			
100	GPIO_3	B4	I	GPIO[3]	B			

Table 7. Pin Assignments (Continued)

1. Optional pull up or pull down resistor may be connected to configure internal ROM program
2. Required external resistor required to select processor boot from internal ROM (pull down) or external ROM (pull up).
3. Drives for a short time after reset, then reverts to high impedance

4.2 Miscellaneous Pins

These pins described in Table 8 are used for used for basic functions such as clocking, reset and infrared receiver interface. The main system clock can be derived from an external crystal connected between the XTLCLK_I and XTLCLK_O pins, or can be received from the CD servo chip via the XTLCLK_I pin. The CS7410 can accommodate a variety of input frequencies, such as 44.1 KHz x 256, x 384, or x 512.

Pin	Signal Name	Type	Description
17	XTLCLK_O	O	Crystal output
18	XTLCLK_I	I	Crystal input, or oscillator input
90	RST_N	I	Asynchronous reset input, active low
91	TEST	I	Manufacturing test, tie to ground

Table 8. Miscellaneous Interface Pins

4.3 Serial Interface Pins

The CS7410 Serial Interface pins are described in Table 9. CS7410 has three dedicated serial ports, each with different protocols. The 2-wire serial port (SER1) supports industry standard protocols. This port is typically used for debug, with the CS7410 as the slave. The slave chip select address is programmable, and defaults to a 7-bit value of 0x1B. A second serial controller (SER2) supports industry standard 3-wire and 4-wire protocols. In master mode, this interface can control a front panel or a small non-volatile memory. In slave mode, it can operate under control of an external processor, for example, in a combination unit. The third serial port (SER3) is a 5-wire master device optimized for reading CD subcodes from the servo chip, and can also be used a general-purpose serial port.

Pin	Signal Name	Type	Description
60	SER1_CLK	B	Debug port serial clock
61	SER1_DAT	B	Debug port serial data
65	SER2_CLK	B	Clock for 4-wire serial port (output for master mode, input for slave mode)
66	SER2_DI	I	Input data for 4-wire serial port
67	SER2_DO	B	Output data for 4-wire serial port – may function as bidirectional data in 3-wire mode.

Table 9. Serial Interface Pins

68	SER2_CS	B	Chip select for 4-wire serial port (output if master, input if slave mode). Can also be used as bidirectional ready line.
69	SER3_CLK	O	Clock output
70	SER3_DO	O	Data output – up to 32 bits per transfer.
72	SER3_DI	I	Data input – up to 96 bits per transfer.
74	SER3_SS0	O	Slave select for first peripheral (programmable polarity)
76	SER3_SS1	O	Slave select for second peripheral (programmable polarity)

Table 9. Serial Interface Pins (Continued)

4.4 SDRAM / DRAM Interface

These pins are used to interface the CS7410 with external synchronous or EDO DRAMs. Data widths of 4 to 16 bits are supported. The CS7410 supports word or block transfers (partial word transfers are not required). Table 10 gives instructions on how to interface to any particular configuration of SDRAM. Table 11 gives pin definitions for interfacing to EDO DRAM.

Pin	Signal Name	Type	Description
3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 15, 20, 21, 22, 23, 24	DRAM Data[15..0]	B	Memory Data Bus.
25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36	DRAM Address[11..0]	O	Memory Address Bus. Connect in order starting with DR_Addr[0] to all RAM address pins not already connected to DR_BS_L or DR_AP.
37	DR_RAS_L	O	Memory Row Address Strobe
39	DR_CAS_L	O	Memory Column Address Strobe
41	M_WE_L	O	Memory Write Enable
43	DR_CKO	O	SDRAM Clock
45	DR_CKE	O	SDRAM Clock Enable
46	DR_BS_L	O	Bank Selection. Always connect to RAM BS or BS0 pin.
47	M_AP_OE	O	Memory Auto Pre-charge. Always connect to RAM AP pin.

Table 10. SDRAM Interface

Pin	Signal Name	Type	Description
3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 15, 20, 21, 22, 23, 24	DRAM Data[15..0]	B	Memory Data Bus.

Table 11. EDO DRAM Interface

Pin	Signal Name	Type	Description
25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36	DRAM Address[11..0]	O	Memory Address Bus.
37	DR_RAS_L	O	Memory Row Address Strobe
39	DR_CAS_L	O	Memory Column Address Strobe
41	M_WE_L	O	Memory Write Enable
47	M_AP_OE	O	Memory Output Enable

Table 11. EDO DRAM Interface (Continued)

4.5 ROM/NVRAM Interface

The ROM/NVRAM Interface pins are described in Table 12. This interface connects to the non-volatile memory that contains the firmware. The memory could be ROM, NVRAM (FLASH), EEPROM, or any combination of these memory types. This interface can also connect to SRAM that would emulate a ROM on a development system. The bus width is always 8 bits. Most of these pins are shared with the DRAM interface, which operates simultaneously with the ROM/NVRAM interface. A number of pins are defined to accept configuration input at power-up (see Table 7), allowing different branches to be taken in the firmware. A configuration resistor is required on pin PCM_DO_0 to select whether the processor will boot from internal or external ROM.

Pin	Signal Name	Type	Description
11, 13, 15, 20, 21, 22, 23, 24	NVMem Data[7..0]	B	Memory Data Bus (shared with bits [7:0] of DRAM data bus).
25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36	NVM_Addr[11..0]	O	Memory Address Bus[11..0] (shared with DRAM address bus)
3, 4, 5, 6, 7, 8, 9, 10	NVM_Addr[19..12]	O	Memory Address Bus[19..12] (shared with bits [15..8] of DRAM data bus).
46	NVM_Addr[20]	O	Memory Address Bus[20] (DRAM BS_L pin).
41	NVM_WE_L	O	NVRAM Write Enable (shared with DRAM WE_L pin)
47	NVM_OE_L	O	NVRAM Write Enable (shared with DRAM WE_L pin)
48	NVM_CE_L	O	ROM/NVRAM Chip Enable.

Table 12. ROM/NVRAM Interface

4.6 Digital Audio Output Interface

The Digital Audio Output Interface pins are described in Table 13. This is the audio PCM interface that connects to an audio PCM DAC. The sample rate and the size of the samples are programmable to accommodate any commercially available DAC. The CS7410 has two data output pins, for up to 4 channels of PCM output, and a separate output pin to simultaneously output IEC-958 encoded data (either compressed or uncompressed).

Pin	Signal Name	Type	Description
78	PCM_XCK	B	Audio 256x/384x/512x Clock input or output to Serial DAC. When output, it's generated from CS7410 internal PLL.
77	SERVOCK	I	Optional source of Audio 256x/384x/512x Audio Clock. May be used for CD direct audio to match input and output clocks.
79	PCM_MUTE	O	Audio Mute control to external DAC. Polarity is programmable and is three-stated at power up.
92	PCM_BCK	O	Audio Bit Clock output to serial DAC. Polarity is programmable.
93	PCM_LRCK	O	Audio Out Left/Right Clock to serial DAC.
94	PCM_DO_0	O	Audio Serial PCM Data Out[0].
95	PCM_DO_1	O	Audio Serial PCM Data Out[1].
96	IEC958_O	O	IEC-958 Output

Table 13. Audio Output Interface

4.7 ΔΣ Modulator Interface

The ΔΣ Interface pins are described in Table 14. The CS7410 contains a stereo Delta-Sigma (ΔΣ) modulator, which outputs two differential digital signals on four pins. These outputs are design to drive an external op-amp based integrator circuit (contact Cirrus Logic Applications Engineering for details).

Pin	Signal Name	Type	Description
84	DAC_LP	O	ΔΣ left channel, positive output
85	DAC_LN	O	ΔΣ left channel, negative output
87	DAC_RP	O	ΔΣ right channel, positive output
89	DAC_RN	O	ΔΣ right channel, positive output

Table 14. ΔΣ Output Interface

4.8 CD Interface

The CD Interface pins are described in Table 15. This interface is used to read serial CD data from a CD servo/read channel chip. The interface supports all standard formats, including 16 MHz, 24 MHz and 32 MHz clocks per container. Control of the CD servo chip is done by the RISC processor using GPIOs, and CD subcode data is read using the dedicated serial interface (SER3).

Pin	Signal Name	Type	Description
81	CD_BCLK	I	CD clock input – polarity is programmable
82	CD_LRCK	I	CD left-right clock input
83	CD_DATA	I	CD serial data input
80	CD_C2P0	I	CD error signaling input

Table 15. CD Interface

4.9 General Purpose Input/Output (GPIO)

The CS7410 provides a number of General Purpose Input/Output (GPIO) pins, each with individual output three-state controls, and a number of General Purpose Output (GPO) pins. Table 16 shows the 17 dedicated GPIO pins. A naming scheme for these pins was chosen to encourage system designers to adhere to standardized pin usage. Table 17 shows the GPIO and GPO pins that can be redefined from other functions. For redefined pins, mode control register bits select the normal function or GPIO/GPO function for the pins. Table 17 also indicates which mode bit controls each pin.

Pin	Signal Name	Type	Description
100, 99, 98, 97	GPIO[3:0]	B	4 General purpose I/O on dedicated pins
53, 52, 51, 50, 49	KP_IN[4:0]	B	5 General purpose I/O on dedicated pins
58, 57, 56, 55, 54	KP_OUT[4:0]	B	5 General purpose I/O on dedicated pins
59	IR_IN	B	General purpose I/O on dedicated pin
62	SER4_CLK	B	General purpose I/O on dedicated pin
63	SER4_DAT	B	General purpose I/O on dedicated pin

Table 16. Dedicated General Purpose I/O Pins

Pin	Signal Name	Type	Description
65	SER2_CLK	B	GPIO controlled by Mode bit 2
67	SER2_DO	B	GPIO controlled by Mode bit 2
68	SER2_CS	B	GPIO controlled by Mode bit 2
66	SER2_DI	B	GPIO controlled by Mode bit 3
69	SER3_CLK	B	GPIO controlled by Mode bit 4
70	SER3_DO	B	GPIO controlled by Mode bit 4
72	SER3_DI	B	GPIO controlled by Mode bit 4
74	SER3_SS0	B	GPIO controlled by Mode bit 4
76	SER3_SS1	B	GPIO controlled by Mode bit 5
80	CD_C2P0	B	GPIO controlled by Mode bit 6
77	SERVOCK	B	GPIO controlled by Mode bit 7
92	PCM_BCK	O	GPO controlled by Mode bit 8
93	PCM_LRCK	O	GPO controlled by Mode bit 9
94	PCM_DO_0	O	GPO controlled by Mode bit 10
95	PCM_DO_1	O	GPO controlled by Mode bit 11
79	PCM_MUTE	O	GPO controlled by Mode bit 12
84	DAC_LP	O	GPO controlled by Mode bit 13

Table 17. Redefined General Purpose Pins

Pin	Signal Name	Type	Description
85	DAC_LN	O	GPO controlled by Mode bit 13
87	DAC_RP	O	GPO controlled by Mode bit 13
89	DAC_RN	O	GPO controlled by Mode bit 13
96	IEC958_O	B	GPIO controlled by Mode bit 14

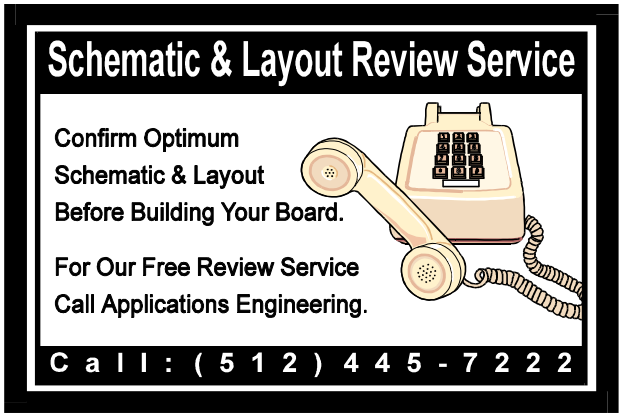
Table 17. Redefined General Purpose Pins (Continued)

4.10 Power and Ground

Table 18 describes the power and ground pins. The CS7410 requires 3 different types of power supplies for the PLLs, internal logic, and IO pins. The PLLs and internal logic use 1.8 V supply voltage. The IO pins use 3.3 V supply voltage. An optional separate supply can be used to provide clean 3.3 V to the Sigma-Delta DACs digital output pads. It is recommended that you use good layout techniques to provide isolation between the supply types on the board. Contact Cirrus Logic applications engineering for layout guidelines.

Pin	Signal Name	Type	Description
1	PLL_GND		Ground for internal PLLs
2	PLL_1V8		1.8V for internal PLLs
14, 40, 73	CORE_GND		Ground for internal core logic
12, 38, 71	CORE_1V8		1.8V for internal core logic
19, 42, 64, 86	IO_GND		Ground for Digital I/Os
16, 44, 75	IO_3V3		3.3V for Digital I/Os
88	DAC_3V3		3.3V for Sigma Delta DAC Digital I/Os

Table 18. Power and Ground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5. 100-PIN MQFP PACKAGE SPECIFICATIONS (20X14X2.85mm)

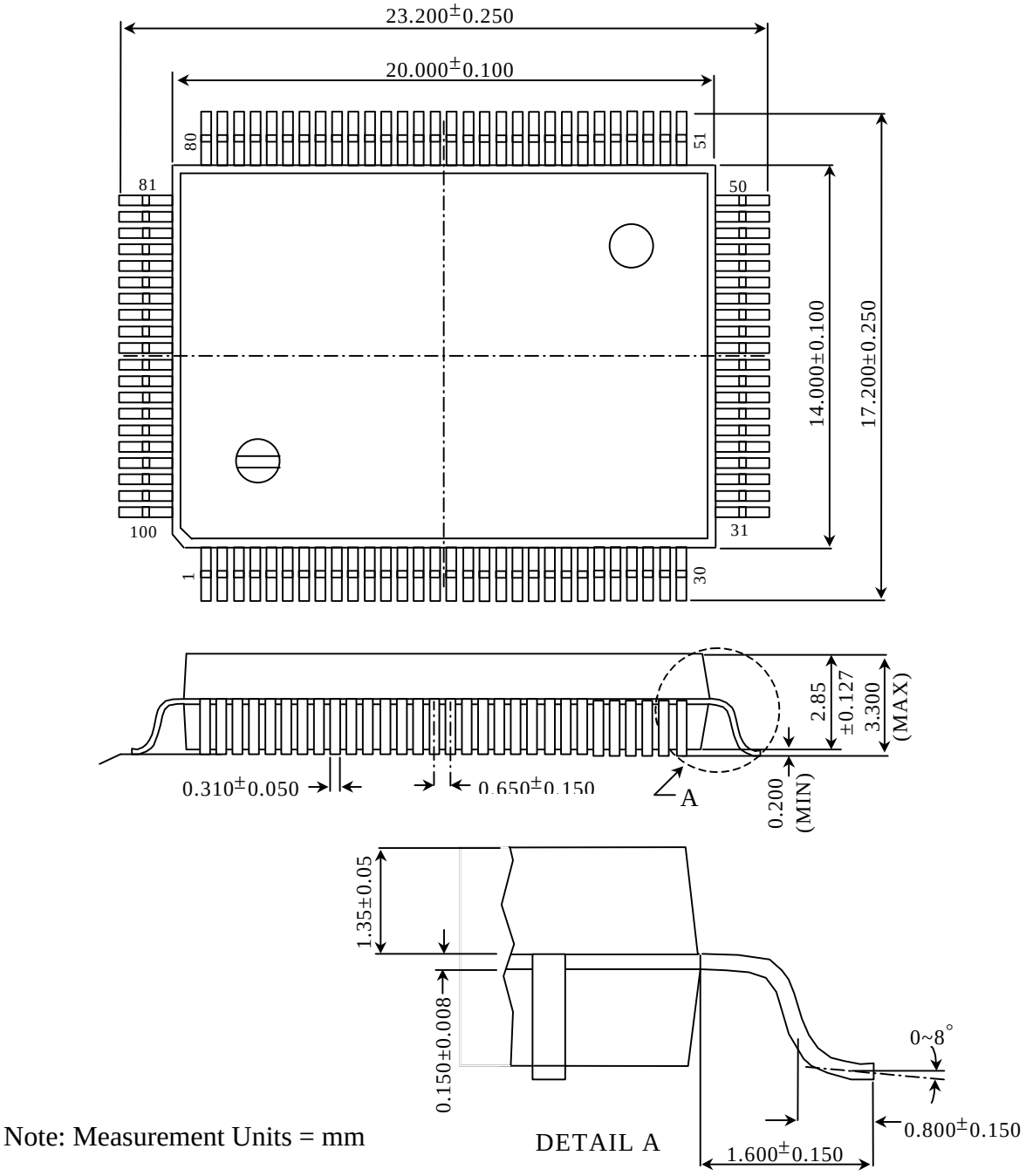
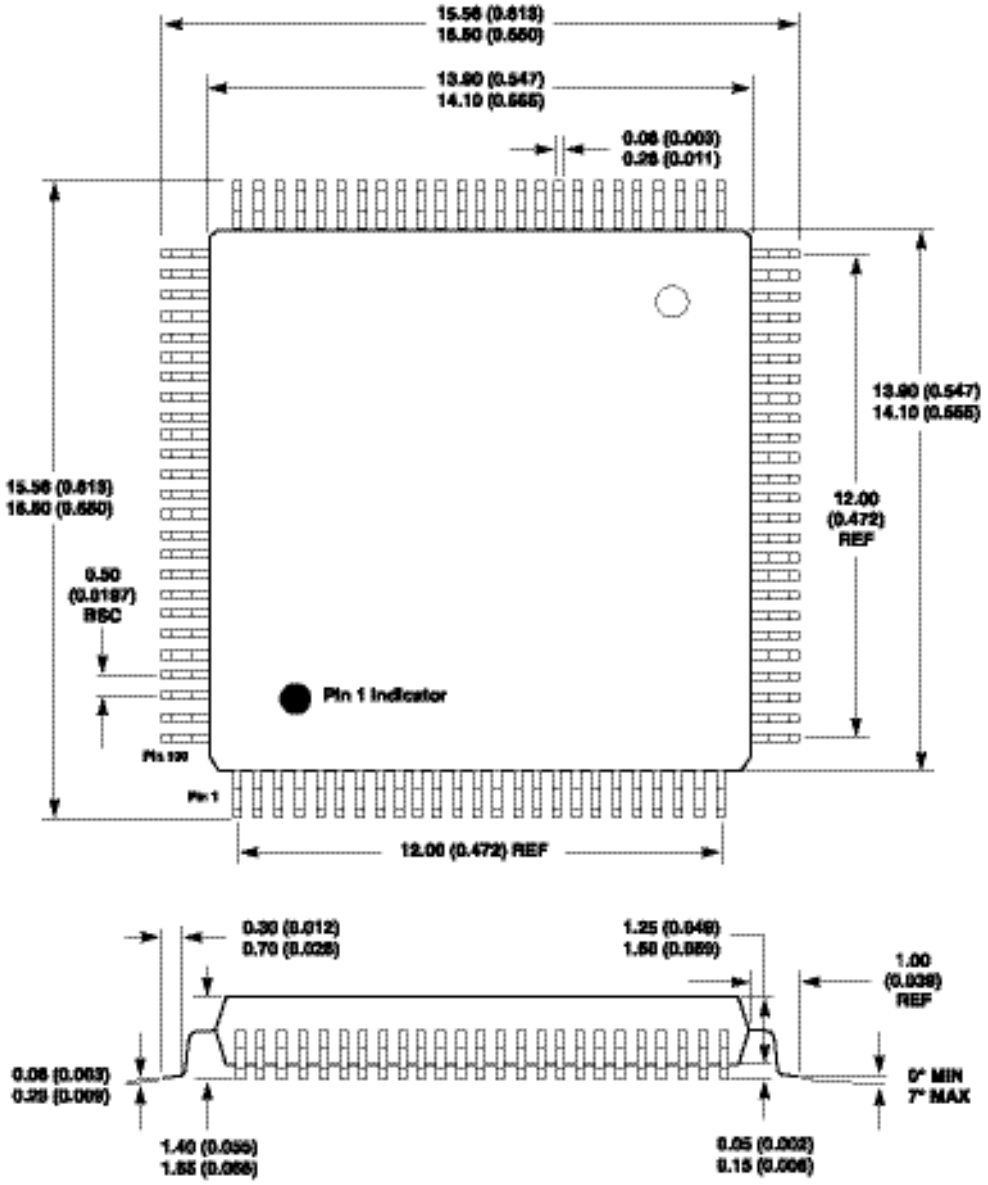


Figure 18. 100-Pin MQFP Package (20x14x2.85mm)

6. 100-PIN LQFP PACKAGE SPECIFICATIONS (14X14X1.4mm)



NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Package body dimensions do not include mold protrusion, which is 0.25 mm (0.010 in).
3) Pin 1 identifcation may be either ink dot or dimple .
4) Package top dimensions can be smaller than bottom dimensions by 0.20 mm (0.008 in).
5) The "lead width with plating" dimension does not include a total allowable dambar protrusion of 0.08 mm (at maximum material condition).
6) Ejector pin marks in molding are present on every package.

Figure 19. 100-Pin LQFP Package (14X14X1.4mm)