CS5529

16-bit, Programmable ΔΣ ADC with 6-bit Latch

Features

- Delta-sigma Analog-to-digital Converter
  - Linearity Error: 0.0015%FS
  - Noise-free Resolution: 16-Bits
- 2.5 V Bipolar/Unipolar Buffered Input Range
- 6-bit Output Latch
- Eight Digital Filters
  - Selectable Output Word Rates
  - Output Settles in One Conversion Cycle
  - 50/60 Hz ±3 Hz Simultaneous Rejection
- Simple Three-wire Serial Interface
  - SPI™ and Microwire™ Compatible
  - Schmitt Trigger on Serial Clock (SCLK)
- System/Self-calibration with R/W Registers
- Power Supply Configurations
  - VA+ = +5 V; VA- = 0 V; VD+ = +3 V to +5 V
  - VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V to +5 V
  - VA+ = +3.0 V; VA- = -3.0 V; VD+ = +3.0 V
- Low Power Consumption: 2.6 mW

General Description

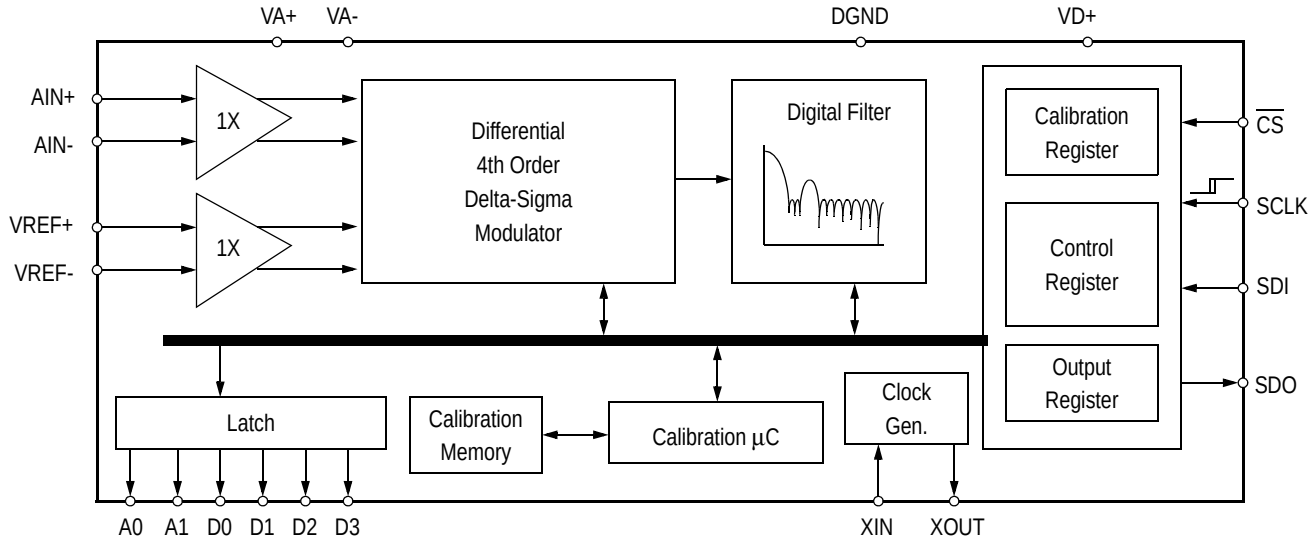
The 16-bit CS5529 is a low-power, programmable ΔΣ ADC (Analog-to-Digital Converter), which includes coarse/fine charge buffers, a fourth-order ΔΣ modulator, a calibration microcontroller, a digital filter with programmable decimation rates, a 6-bit output latch, and a three-wire serial interface. The ADC is designed to operate from single or dual analog supplies and a single digital supply.

The digital filter is programmable with output update rates between 1.88 Hz to 101 Sps. These output rates are specified for XIN = 32.768 kHz. Output word rates can be increased by approximately 3X by using XIN = 100 kHz. The filter is designed to settle to full accuracy for the selected output word rate in one conversion. When operated at word rates of 15 Sps or less, the filter rejects both 50 Hz and 60 Hz simultaneously.

Low power, single conversion settling time, programmable output rates, and the ability to handle negative input signals make this single- or dual-supply product an ideal solution for isolated and non-isolated applications.

ORDERING INFORMATION

See page 29.



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REVISION HISTORY

Revision	Date	Changes
F4	Sep '04	Added lead-free device ordering information..
F5	Aug '05	Updated legal notice. Added MSL data.

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CHARACTERISTICS & SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25 °C; VA± = ±2.5 V ±5%, VD+ = 5 V ±5%, VREF+ = 2.5 V, VREF- = 0.0 V, F_{CLK} = 32.768 kHz, OWR (Output Word Rate) = 15 Sps, Bipolar Mode, Input Range = ±2.5 V.) (See Notes 1 and 2.)

Parameter		Min	Typ	Max	Unit
Accuracy					
Linearity Error		-	±0.0015	±0.003	%FS
No Missing Codes		16	-	-	Bits
Bipolar Offset	(Note 3)	-	±1	±2	LSB_{16}
Unipolar Offset	(Note 3)	-	±2	±4	LSB_{16}
Offset Drift	(Notes 3 and 4)	-	11	-	nV/°C
Bipolar Gain Error		-	±8	±31	ppm
Unipolar Gain Error		-	±16	±63	ppm
Gain Drift	(Note 4)	-	1	-	ppm/°C

Noise (Notes 5 and 6)		
Output Word Rate (Hz)	**-3 dB Filter Frequency (Hz)**	**Noise (µV)**
1.88	1.64	4.5
3.76	3.27	5.0
7.51	6.55	7.0
15.0	12.7	15
30.0	25.4	45
61.6	50.4	190
84.5	70.7	900
101.1	84.6	3000

Notes:
1. Applies after system calibration at any temperature within -40 °C ~ +85 °C.
2. Specifications guaranteed by design, characterization, and/or test.
3. Specification applies to the device only and does not include any effects by external parasitic thermocouples.
4. Drift over specified temperature range after calibration at power-up at 25 °C.
5. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25 °C.
6. For peak-to-peak noise multiply by 6.6 for all ranges and output rates.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter			Min	Typ	Max	Unit
Analog Input						
Common Mode + Signal on AIN+ or AIN-	(Bipolar/Unipolar Mode)					
	Single Supply		0.0	-	VA+	V
	Dual Supply		VA-	-	VA+	V
Common Mode Rejection	dc		-	120	-	dB
	50, 60Hz		-	120	-	dB
Input Capacitance			-	10	-	pF
CVF Current	AIN+, AIN-	(Note 7)	-	16	-	nA
System Calibration Specifications						
Full Scale Calibration Range, with VREF = 2.5 V		(Note 8)	1.0	-	3.5	V
Offset Calibration Range	(Bipolar/Unipolar Mode)		-	-	±1.25	V
Voltage Reference Input						
Range	{(VREF+) - (VREF-)}	(Note 9)	1.0	2.5	5	V
REF+			VA-	-	VA+	V
REF-			VA-	-	VA+	V
Common Mode Rejection	dc		-	110	-	dB
	50, 60 Hz		-	130	-	dB
Input Capacitance			-	16	-	pF
CVF Current		(Note 7)	-	8	-	nA
Power Supplies						
DC Power Supply Currents	(Normal Mode)					
	I_{A+}		-	400	520	µA
	I_{D+}		-	110	150	µA
Power Consumption	Normal Mode	(Note 10)	-	2.6	3.5	mW
	Low Power Mode		-	1.8	2.5	mW
	Standby		-	1	-	mW
	Sleep		-	500	-	µW
Power Supply Rejection	dc Positive Supplies		-	80	-	dB
	dc Negative Supply		-	80	-	dB

Notes:
7. See the section of the data sheet which discusses Analog Input Models.
8. The minimum Full Scale Calibration Range (FSCR) is limited by the maximum allowed gain register value (with margin). The maximum FSCR is limited by the ΔΣ modulator's 1's density range. See "Analog Input" section for details. Also see "Limitations in Calibration Range".
9. VREF must be less than or equal to supply voltages.
10. All outputs unloaded. All inputs CMOS levels. Power consumption scales linearly with changes in supply voltage.

5V DIGITAL CHARACTERISTICS (T_A = 25 °C; VA± = ±2.5V ±5%, VD+ = 5V ± 5%.)(See Notes 2 and 11.)

Parameter			Symbol	Min	Typ	Max	Unit
High-level Input Voltage:	All Pins Except	XIN, SCLK	V_{IH}	0.6VD+	-	-	V
		XIN	V_{IH}	(VD+)-0.9	-	-	V
		SCLK	V_{IH}	(VD+)-0.45	-	-	V
Low-level Input Voltage:	All Pins Except	XIN, SCLK	V_{IL}	-	-	0.8	V
		XIN	V_{IL}	-	-	2.0	V
		SCLK	V_{IL}	-	-	0.6	V
High-level Output Voltage:	All Pins Except	SDO (Note 12)	V_{OH}	(VD+)-1.0	-	-	V
		SDO, I_{out} = -5.0mA	V_{OH}	(VD+)-1.0	-	-	V
Low-level Output Voltage:	All Pins Except	SDO, I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
		SDO, I_{out} = 5.0mA	V_{OL}	-	-	0.4	V
Input Leakage Current			I_{in}	-	±1	±10	µA
3-state Leakage Current			I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance			C_{out}	-	9	-	pF

Notes: 11. All measurements performed under static conditions.

12. I_{out} = -100 µA unless stated otherwise. (V_{OH} = 2.4 V @ I_{out} = -40 µA).

3 V DIGITAL CHARACTERISTICS (T_A = 25 °C; VA± = ±2.5 V ±5%, VD+ = 3.0 V ±5%.) (See Notes 2 and 11.)

Parameter			Symbol	Min	Typ	Max	Unit
High-level Input Voltage:	All Pins Except	XIN, SCLK	V_{IH}	0.6VD+	-	-	V
		XIN	V_{IH}	(VD+)-0.9	-	-	V
		SCLK	V_{IH}	(VD+)-0.45	-	-	V
Low-level Input Voltage:	All Pins Except	XIN, SCLK	V_{IL}	-	-	0.16 VD+	V
		XIN	V_{IL}	-	-	0.5	V
		SCLK	V_{IL}	-	-	0.6	V
High-level Output Voltage:	All Pins Except	SDO, I_{out} = -400 µA	V_{OH}	(VD+)-0.3	-	-	V
		SDO, I_{out} = -5.0 mA	V_{OH}	(VD+)-1.0	-	-	V
Low-level Output Voltage:	All Pins Except	SDO, I_{out} = 400 µA	V_{OL}	-	-	0.3	V
		SDO, I_{out} = 5.0 mA	V_{OL}	-	-	0.4	V
Input Leakage Current			I_{in}	-	±1	±10	µA
3-state Leakage Current			I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance			C_{out}	-	9	-	pF

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Modulator Sampling Frequency	f_s	XIN/4	Hz
Filter Settling Time to 1/2 LSB (Full Scale Step)	t_s	$1/f_{out}$	s

ABSOLUTE MAXIMUM RATINGS (DGND = 0 V) (See Note 13.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 14 and 15)					
Positive Digital		VD+	-0.3	-	+6.0	V
Positive Analog		VA+	-0.3	-	+6.0	V
Negative Analog		VA-	-6.0	-	+0.3	V
Input Current, Any Pin Except Supplies	(Notes 16 and 17)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 18)	PDN	-	-	8	mW
Analog Input Voltage	AIN and VREF pins	V_{INA}	(VA-) + (-0.3)	-	(VA+)+0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+)+0.3	V
Ambient Operating Temperature		T_A	-40	-	+85	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 13. All voltages with respect to ground.

14. VA+ and VA- must satisfy {(VA+) - (VA-)} ≤ +6.3 V; and |VA-| must be ≤ VA+.

15. VD+ and VA- must satisfy {(VD+) - (VA-)} ≤ +7.75 V.

16. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.

17. Transient current of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

18. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

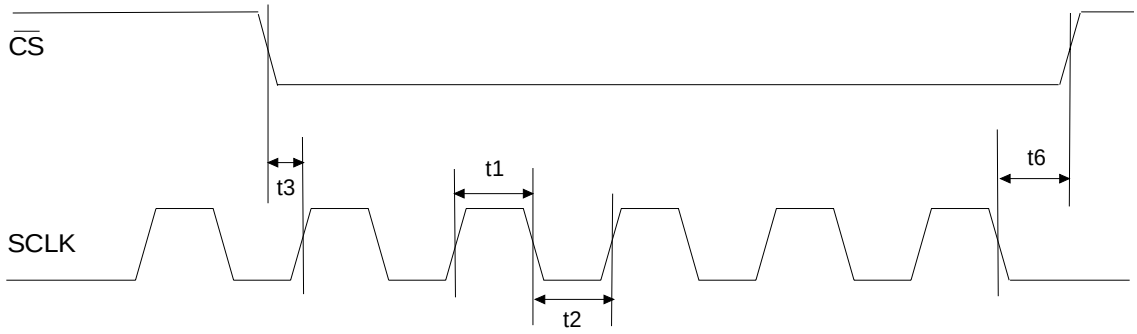
SWITCHING CHARACTERISTICS (T_A = 25 °C; VA± = ±2.5 V ±5%, VD+ = 3 V ±5% or 5 V ±5%; Input Levels: Logic 0 = 0 V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency:	External Clock or Internal Oscillator (Note19)	XIN	30	32.768	100	kHz
Master Clock Duty Cycle			40	-	60	%
Rise Times	(Note 20)	t_{rise}				
	Any Digital Input Except SCLK		-	-	1.0	µs
	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Fall Times	(Note 20)	t_{rise}				
	Any Digital Input Except SCLK		-	-	1.0	µs
	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Start-up						
Oscillator Start-up Time	XTAL = 32.768 kHz (Note 21)	t_{ost}	-	500	-	ms
Power-on Reset Period		t_{por}	-	1002	-	XIN cycles
Serial Port Timing						
Serial Clock Frequency		SCLK	0	-	2	MHz
Serial Clock	Pulse Width High	t_1	250	-	-	ns
	Pulse Width Low	t_2	250	-	-	ns
SDI Write Timing						
$\overline{CS}$ Enable to Valid Latch Clock		t_3	50	-	-	ns
Data Set-up Time prior to SCLK rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable		t_6	100	-	-	ns
SDO Read Timing						
$\overline{CS}$ to Data Valid		t_7	-	-	150	ns
SCLK Falling to New Data Bit		t_8	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_9	-	-	150	ns

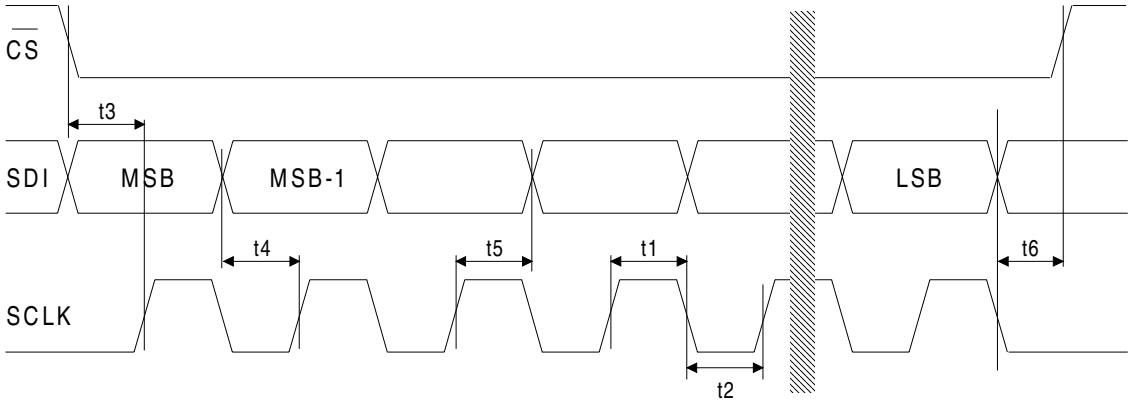
Notes: 19. Device parameters are specified with 32.768 kHz clock, however, clocks up to 100 kHz can be used for increased throughput.

20. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

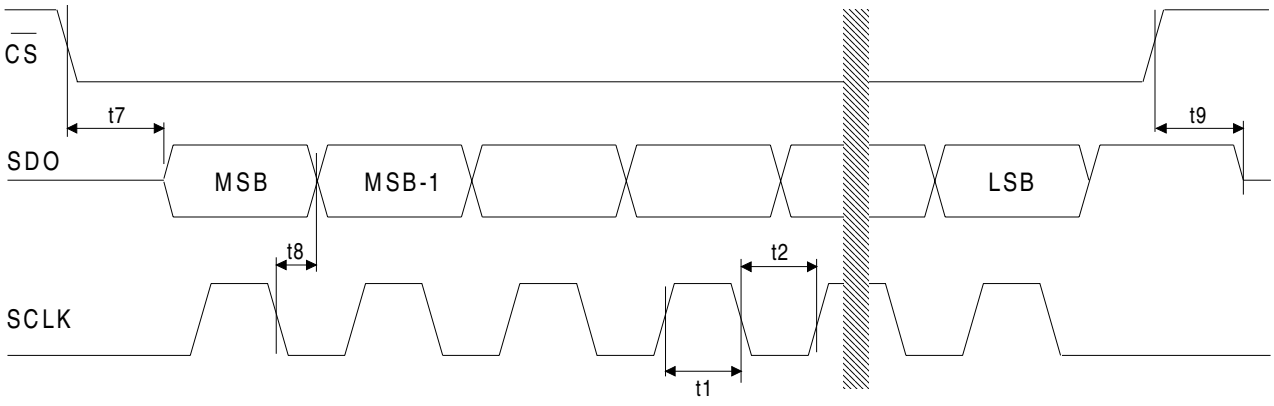
21. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.



Continuous Running SCLK Timing (Not to Scale)



SDI Write Timing (Not to Scale)



SDO Read Timing (Not to Scale)

GENERAL DESCRIPTION

The CS5529 is a 16-bit ΔΣ Analog-to-Digital Converter (ADC) which includes coarse/fine charge buffers, a fourth order ΔΣ modulator, a calibration microcontroller, eight digital filters which provide selectable decimation rates, a 6-bit output latch, and a three-wire serial interface. The ADC is optimized to digitize unipolar or bipolar signals in industrial applications.

The digital filters provide eight selectable output word rates (OWRs) of 1.88 Sps, 3.76 Sps, 7.51 Sps, 15.0 Sps, 30.0 Sps, 61.6 Sps, 84.5 Sps, 101.1 Sps when operated from a 32.768 kHz watch crystal or equivalent clock (output word rates can be increased by approximately 3X by using 100 kHz clock). The filters are designed to settle to full accuracy for the selected output word rate in one conversion. When operated at word rates of 15 Sps or less (XIN = 32.768 kHz), the filter rejects both 50 Hz and 60 Hz line interference simultaneously.

Analog Input

The CS5529 provides a nominal 2.5 V input span when the gain register is 1.0 decimal and the differential reference voltage between VREF+ and VREF- is 2.5 V. The gain registers content is used during calibration to set the gain slope of the ADC's transfer function. The differential reference voltage magnitude and the gain register are two factors that can be used to scale the nominal 2.5 V input span. After reset, the gain register defaults to 1.0 decimal. In this case, the external voltage between the VREF+ pin and the VREF- pin sets the ADC's nominal full scale input span to 2.5 V. If a user want to modify the input span, either the gain register or the reference voltage's magnitude needs to be changed. For example, if a 1.25 V reference is used in place of the nominal 2.5 V input, the full-scale span is cut in half. To achieve the same 1.25V input span, the user could simply use a 2.5 V reference and modify the gain register to 2.0 decimal.

Note that to keep from saturating the analog front end, the input span must stay at or below 1.5 times the reference voltage. This corresponds to a gain register of 0.666... when a 2.5 V reference voltage is used.

Note: When a smaller reference voltage is used, the resulting code widths are smaller. Since the output codes exhibit more changing codes for a fixed amount of noise, the converter appears noisier.

Calibration can also affect the ADC's full scale span because system gain calibration can be used to increase or decrease the full scale span of the ADC's transfer functions. At its limit, the input full scale can be reduced to the point in which the gain register reaches its upper limit of 3.999... (this will occur when the ADC is gain calibrated with an input signal less than or equal to approximately 1/4 of its nominal full scale, if the ADC does not have intrinsic gain error). Calibration and its effects on the analog input span is detailed in a later section of the data sheet.

Analog Input Model

Figure 1 illustrates the input models for the AIN pins. The model includes a coarse/fine charge buffer which reduces the dynamic current demands from the signal source. The buffer is designed to accommodate rail to rail (common-mode plus signal) input voltages. Typical CVF (sampling) current is about 16nA (XIN = 32.768 kHz, see Figure 1). Application Note 30, "Switched-Capacitor A/D Input Structures", details various input architectures.

Voltage Reference Input Model

Figure 2 illustrates the input models for the VREF pins. It includes a coarse/fine charge buffer which reduces the dynamic current demand of the external reference. Typical CVF (sampling) current is about 8nA (XIN = 32.768 kHz, see Figure 2).

The reference's buffer is designed to accommodate rail-to-rail (common-mode plus signal) input volt-

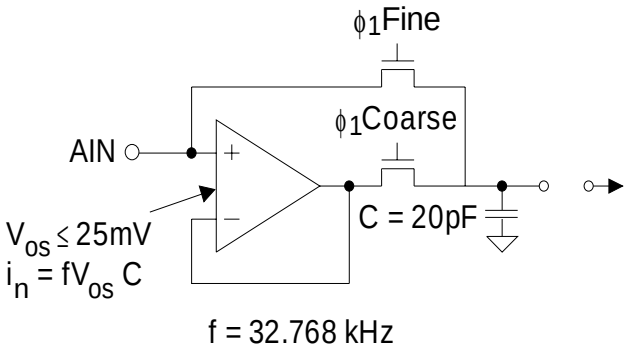


Figure 1. Input models for AIN+ and AIN- pins.

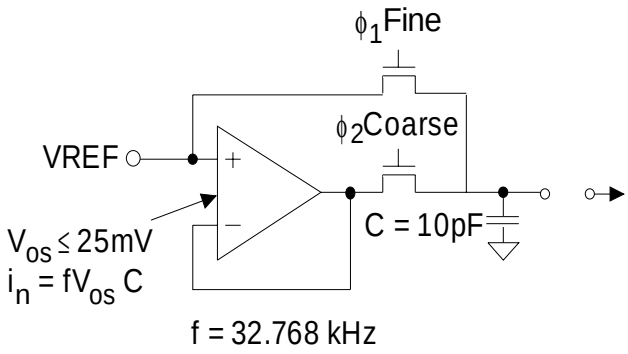


Figure 2. Input model for VREF+ and VREF- pins.

ages. The differential voltage between VREF+ and VREF- sets the nominal full scale input span of the converter. For a single-ended reference voltage, such as the LT1019-2.5, the reference output is connected to the VREF+ pin of the CS5529 and the ground reference for the LT1019-2.5 is connected to the VREF- pin.

Serial Port

The CS5529 includes a microcontroller with a command register, a configuration register, a conversion data register (read only), and a gain and offset register for calibration. All registers, except the 8-bit command register, are 24-bits in length. Figure 3 illustrates a block diagram of all the internal register.

After a system initialization or reset, the serial port is set to the command mode. The converter stays in this mode until a valid 8-bit command is received (the first 8-bits into the serial port). Once a valid 8-bit command is received and interpreted by the ADC's command register, the serial port enters the data mode. In data mode the next 24 serial clock pulses shift data either into or out of the serial port (72 serial clock pulses are needed if the setup register command is issued). The Command Register Descriptions section illustrates all valid commands.

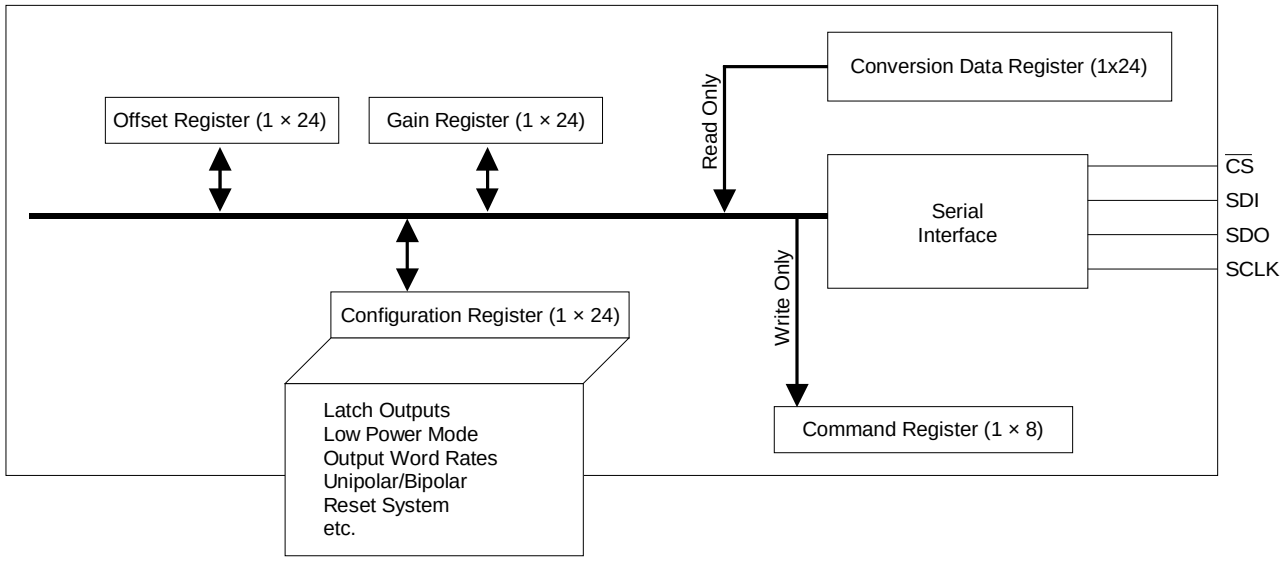


Figure 3. CS5529 Register Diagram.

Command Register Descriptions

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
CB	SC	CC	R/$\overline{W}$	RSB2	RSB1	RSB0	PS/$\overline{R}$

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, CB	0 1	Null command (no operation). All command bits, including CB must be 0. Logic 1 for executable commands.
D6	Single Conversion, SC	0 1	Single Conversion not active. Perform a conversion.
D5	Continuous Conversions, CC	0 1	Continuous Conversions not active. Perform conversions continuously.
D4	Read/Write, R/W	0 1	Write to selected register. Read from selected register.
D3-D1	Register Select Bit, RSB2-RSB0	000 001 010 011 100 101 110 111	Offset Register Gain Register Configuration Register Conversion Data Register (read only) Set-up Registers (Offset, Gain, Configuration) Reserved Reserved Reserved
D0	Power Save/Run, PS/R	0 1	Run Power Save

Table 1. Command Set

Perform Single Conversion

7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0

This command instructs the ADC to perform a single conversion.

Perform Continuous Conversions

7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0

This command instructs the ADC to perform continuous conversions.

Power Save/$\overline{Run}$

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	PS/$\overline{R}$

If PS/$\overline{R}$ = 0, normal run mode is entered. If PS/$\overline{R}$ = 1, power save mode is entered.

Null

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

This command is used to clear the port flag in the continuous conversion mode when the port flag bit in the configuration register is set to logic 1.

SYNC1

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1

Part of the serial port re-initialization sequence (see text for use of command).

SYNC0

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	0

End of the serial port re-initialization sequence.

Read/$\overline{\text{Write}}$ Registers

7	6	5	4	3	2	1	0
1	0	0	R/$\overline{W}$	RSB2	RSB1	RSB0	0

These commands are used to perform a write to or a read from a specific register. The register to be accessed is selected with the RSB2-RSB0 bits of the command word.

R/$\overline{W}$ 0 Write Register

1 Read Register

RSB[4:0] Register address binary encoded 0 to 31 as follows. All registers are 24 bits long.

Address	Description
000	Read or Write Offset Register
001	Read or Write Gain Register
010	Read or Write Configuration Register
011	Read Conversion Data Register
100	Read or Write Offset Gain and Configuration Registers in this sequence (i.e. one 8-bit command is followed by 72-bits of data to access the Offset, then the Gain, and then the Configuration register)

Serial Port Interface

The CS5529's serial interface consists of four control lines: $\overline{CS}$, SDI, SDO, and SCLK.

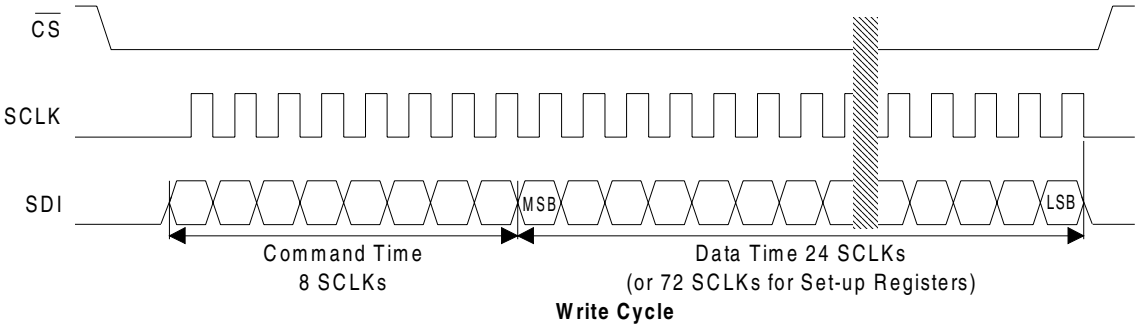
$\overline{CS}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied to logic 0, the port can function as a three wire interface.

SDI, Serial Data In, is the data signal used to transfer data to the converters.

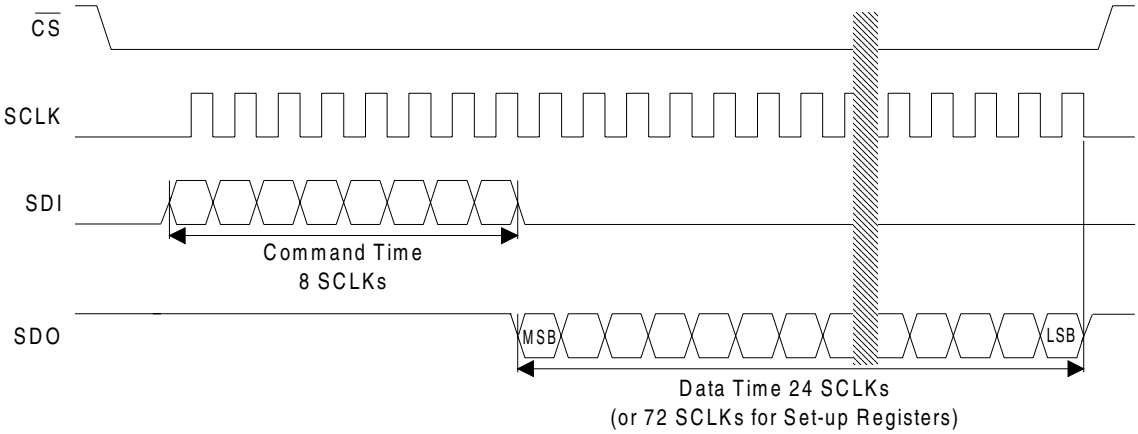
SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held at logic 0 before SCLK transitions can be recognized by the port logic. To accommodate opto-isolators SCLK is designed with a Schmitt-trigger input to allow an opto-isolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an opto-isolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.

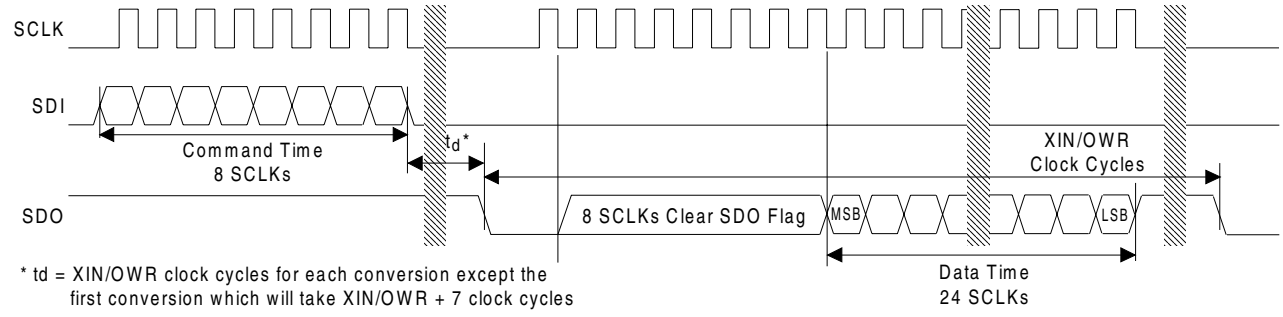
Figure 4 illustrates the serial sequence necessary to write to, or read from the serial port's registers. A transfer of data is always initiated by sending the appropriate 8-bit command (MSB first) to the serial port (SDI pin). It is important to note that some commands use information from the configuration registers to perform the function. For those commands it is important that the correct information is written to the configuration register first.



Write Cycle



Read Cycle



SDO Continuous Conversion Read (PF bit = 1)

Figure 4. Command and Data Word Timing.

Serial Port Initialization

The serial port is initialized to the command mode whenever a power-on reset is performed or when the port initialization sequence is completed. The port initialization sequence involves clocking fifteen (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE). This sequence places the chip in the command mode where it waits until a valid command is received. This function does not reset the internal registers to their default settings. It only resets the serial port to the command mode.

System Initialization

When power to the CS5529 is applied, the chip is held in a reset condition until the 32.768 kHz oscillator has started and a counter-timer elapses. Due to the high Q of the 32.768 kHz crystal, the oscillator takes 400-600 ms to start. The counter-timer counts 1002 oscillator clock cycles to make sure the oscillator is fully stable. During this time-out period the serial port logic is reset and the RV (Reset Valid) bit in the configuration register is set to indicate that a valid reset occurred. After a reset, the on-chip registers are initialized to the following states and the converter is placed in the command mode where it waits for a valid command.

Configuration Register:	000040(H)
Offset Register:	000000(H)
Gain Register:	400000(H)

Note: A system reset can be initiated at any time by writing a logic 1 to the RS (Reset System) bit in the configuration register. After a reset, the RV (Reset Valid) bit is set until the configuration register is read. The user must then write a logic 0 to the RS bit to take the part out of the reset mode.

Configuration Register

The configuration register is a 24 bit register used to modify the functions of the ADC. The following sections detail the functions of the bits in the configuration register.

Latch Output Pins

The D3-D0 pins of the converter mimic the D21-D18 bits of the configuration register. D3-D0 can be used to control multiplexers and other digital logic functions outside the converter. The D0-D3 outputs are powered from VD+ and DGND. Their output voltage will be VD+ for a logic 1 and DGND for a logic 0. The A1-A0 pins of the converter mimic the D23-D22 bits of the configuration register and can be used to control analog switches. These outputs are powered from VA+ and VA-, hence, their output voltage will be either VA+ for a logic 1 or VA- for a logic 0.

All outputs can sink or source at least 1 mA, but it is recommended to limit drive currents to less than 20 µA to reduce self-heating of the chip.

Power Consumption

The CS5529 accommodates four power consumption modes: normal, low power, standby, and sleep. The normal mode, the default mode, is entered after a power-on-reset and typically consumes 2.5 mW. The low power mode is an alternate mode that reduces the consumed power to 1.4 mW. It is entered by setting bit D16 (the low power mode bit) in the configuration register to logic 1. Since the converter's noise and linearity performance improves with increased power consumption, slightly degraded noise or linearity performance should be expected in the low power mode.

The final two modes are the power save modes. These modes power down most of the analog portion of the chip and stop filter convolutions. The power save modes are entered whenever the Power Save (0x81 hexadecimal) command is issued to the serial port. The particular power save mode entered depends on state of bit D4 (the power save select bit) in the configuration register. If D4 is logic 0, the converter enters the standby mode reducing the power consumption to 1 mW. The standby mode leaves the oscillator and the on-chip bias generator

running. This allows the converter to quickly return to the normal or low power mode once the PS/$\overline{R}$ bit is set back to a logic 0. If D4 in the configuration register is logic 1 and Power Save command is issued, the sleep mode is entered reducing the consumed power to less than 10 µW. Since the sleep mode disables the oscillator, approximately a 500 ms crystal oscillator start-up delay period is required before returning to the normal or low power mode. If an external clock is used, the chip should start within a few microseconds.

Output Word Rate

The WR2-WR0 bits of the configuration register set the output conversion word rate of the converter as shown in the Configuration Register Descriptions table. The word rates indicated in the table assume a master clock of 32.768 kHz. Upon reset the converter is set to operate with an output word rate of 15.0 Sps.

Digital Filter

The CS5529 has eight different linear phase digital filters which set the output word rates (OWRs) as stated in Configuration Register Descriptions. These rates assume that XIN is 32.768 kHz. Each of the filters has a magnitude response similar to that shown in Figure 5. The filters are optimized to settle to full accuracy every conversion and yield better than 80 dB rejection for both 50 Hz and 60 Hz with output word rates at or below 15.0 Sps (XIN = 32.768 kHz).

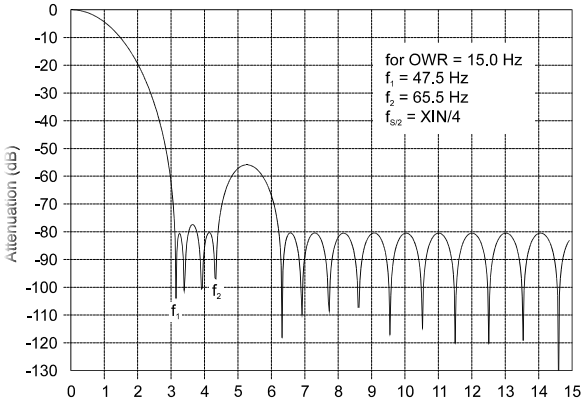


Figure 5. Filter Response (Normalized to Output Word Rate = 1).

The converter's digital filters scale with XIN. For example with an output word rate of 15 Sps, the filter's corner frequency is typically 12.7 Hz. If XIN is increased to 64.536 kHz the OWR doubles and the filter's corner frequency moves to 25.4 Hz.

Clock Generator

The CS5529 includes a gate which can be connected with an external crystal to provide the master clock for the chip. The chip is designed to operate using a low-cost 32.768 kHz "tuning fork" type crystal. One lead of the crystal should be connected to XIN and the other to XOUT. Lead lengths should be minimized to reduce stray capacitance. Note that the converter will operate with an external (CMOS compatible) clock with frequencies up to 100 kHz.

Reset System

The reset system bit permits the user to perform a hardware reset. A hardware reset can be initiated at any time by writing a logic 1 to the RS (Reset System) bit in the configuration register. After a hardware reset cycle is complete, the serial port logic is reset and the RV (Reset Valid) bit in the configuration register is set to indicate that a valid reset occurred. After a reset, the on-chip registers are initialized to the following states and the converter is placed in the command mode where it waits for a valid command.

Configuration Register:	000040(H)
Offset Register:	000000(H)
Gain Register:	400000(H)

Note: A system reset can be initiated at any time by writing a logic 1 to the RS (Reset System) bit in the configuration register. After a reset, the RV (Reset Valid) bit is set until the configuration register is read. The user must then write a logic 0 to the RS bit to take the part out of the reset mode.

Port Flag

The port flag bit in the configuration register allows the user to select the mode in which conversions will be presented to the serial port. With the port flag bit cleared, the user must read the conversion data register. With the port flag bit set to logic 1, the user can read the conversion data from the serial port by first issuing the NULL command to clear the SDO flag and then issuing 24 SCLKs to read the conversion word.

Calibration

Calibration is used to set the zero and gain slope of the ADC's transfer function. The calibration control bits in the configuration register allow the user to perform either self calibration or system calibration.

The offset and gain calibration steps each take one conversion cycle to complete. At the end of the calibration step, the calibration control bits will be set back to logic 0, and the DF (Done Flag) bit will be set to a logic 1. For the combination self-calibration (CC2-CC0= 011; offset calibration followed by gain calibration), the calibration will take two conversion cycles to complete and will set the DF bit after the gain calibration is completed.

Note: 1) The DF bit will be cleared any time the data register, the offset register, the gain register, or the setup register is read. Reading the configuration register alone will not clear the DF bit.
2) After the CS5529 is reset, the converter is functional and can perform measurements without being calibrated. In this case, the converter will utilize the initialized values of the on-chip registers (Gain = 1.0, Offset = 0.0) to calculate output words. Any initial offset and gain errors in the internal circuitry of the chip will remain.

Calibration Registers

The offset calibration result is stored in the offset register. The result is used during the conversion process to nullify offset errors. One LSB in the offset register is 2^{-24} proportion of the input span (bipolar span is 2 times the unipolar span). The MSB in the offset register determines if the offset to be trimmed is positive or negative (0 positive, 1 negative). The converter can typically trim ±50 percent of the input span. Refer to the following Offset Register and Gain Register descriptions for details.

Offset Register

23(MSB)	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**
Sign	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}
0	0	0	0	0	0	0	0	0	0	0	0
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}
0	0	0	0	0	0	0	0	0	0	0	0

One LSB represents 2^{-24} proportion of the input span (bipolar span is 2 times unipolar span).
Offset and data word bits align by MSB (bit MSB-4 of offset register changes bit MSB-4 of data). After reset, all bits are '0'.

Gain Register

23(MSB)	22	21	20	19	18	17	16	15	14	13	12
2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}
0	0	0	0	0	0	0	0	0	0	0	0
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}
0	0	0	0	0	0	0	0	0	0	0	0

The gain register span is from 0 to ($4-2^{-22}$). After Reset the (MSB-1) bit is '1', all other bits are '0'.

The gain calibration results is stored in the gain register. The result sets the slope of the ADC's transfer function. The gain register spans from 0 to ($4 - 2^{-22}$). The decimal equivalent meaning of the gain register is

$$D = b_{MSB}2^{1} + (b_0 2^{0} + b_1 2^{-1} + \ldots + b_N 2^{-N}) = b_{MSB}2^{1} + \sum_{i=0}^{N} b_i 2^{-i}$$

where the binary numbers have a value of either zero or one (b_0 corresponds to bit MSB-1, N = 22).

Self Calibration

The CS5529 offers both self offset and self gain calibrations. For the self-calibration of offset, the converter internally ties the inputs of the modulator together and routes them to the VREF- pin as shown in Figure 6. Also self offset calibration requires that VREF- be tied to a fixed voltage between VA+ and VA-. For self-calibration of gain, the differential inputs of the modulator are connected to VREF+ and VREF- as shown in Figure7.

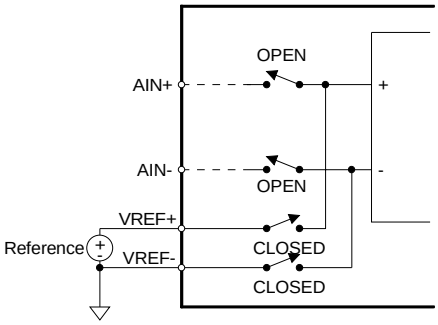


Figure 7. Self Calibration of Gain.

System Calibration

For the system calibration functions, the user must input signals which represent system ground and system full scale to the converter. When a system offset calibration is performed a ground reference signal must be applied to the converter (see Figure 8). When a system gain calibration is performed, the user must input a signal representing the positive full scale point as shown in Figure 9. In either case, calibration signals must be within the specified calibration limits for each specific calibration step (refer to the System Calibration Specifica-

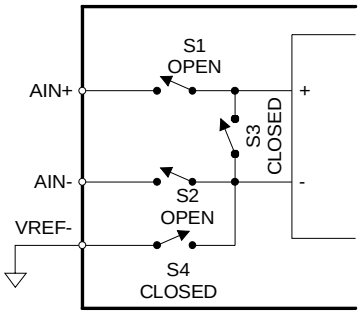


Figure 6. Self Calibration of Offset.

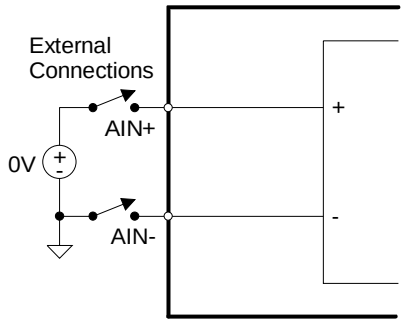


Figure 8. System Calibration of Offset.

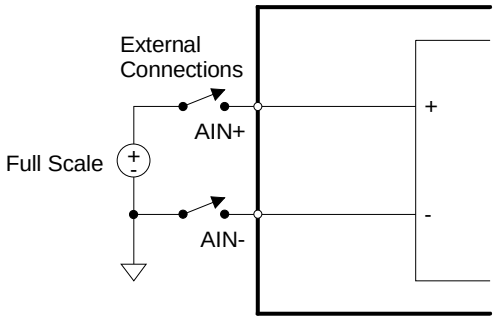


Figure 9. System Calibration of Gain.

tions). If a system gain calibration is performed, the calibrated input must not cause the resulting gain register's content, decoded in decimal, to exceed 3.9999998. The above condition requires that the full scale input voltage to be greater than 25 percent of the differential reference voltage (i.e. a 625mV input signal must be applied if the differential reference voltage is 2.5V).

Limitations in Calibration Range

System calibration can be limited by signal headroom in the analog signal path inside the chip as discussed under the Analog Input section of this data sheet. For gain calibration the full scale input signal can be reduced to the point in which the gain register reaches its upper limit of ($4\text{-}2^{-22}$ decimal) or FFFFFF (hexadecimal). Under nominal conditions, this occurs with a full scale input signal equal to about 1/4 the reference voltage. With the converter's intrinsic gain error, this full scale input signal may be higher or lower. In defining the minimum Full Scale Calibration Range (FSCR) under "Analog Characteristics", margin is retained to accommodate the intrinsic gain error. Alternatively the input full scale signal can be increased to a point which exceeds the operating range of the analog circuitry. This occurs when the input voltage is approximately 1.5X the differential reference voltage (Gain Register = 1.0).

Calibration Tips

Calibration steps are performed at the output word rate selected by the WR2-WR0 bits of the configuration register. Since higher word rates result in conversion words with more peak-to-peak noise, calibration should be performed at lower output word rates. Also, to minimize digital noise near the device, the user should wait for each calibration step to be completed before reading or writing to the serial port.

Factory calibration can be performed in a user's system by using the system calibration capabilities of the CS5529. After the ADC is calibrated in the user's system, the offset and gain register contents can be read by the system microcontroller and recorded in EEPROM. These same calibration words can then be uploaded into the offset and gain registers of the converter when power is first applied to the system.

A user can scale the input range by modifying the gain register. For example, if a self or system calibration is performed with a full scale of 2.5 V and a full scale of 1.25 V is desired, the user can modify the gain register to double its slope. This can be done by reading the gain register, shifting the binary word one position to the left (this multiplies the gain word by 2), and writing this word back into the gain register. The gain register can be scaled by any amount as long as it does not exceed a decimal range of 0.25 to 4.0.

One of two methods can be used to determine when a calibration is complete: 1) if the PF (Port Flag) bit of the configuration register is set to logic 1, SDO falls to logic 0 at the completion of a calibration; or 2) regardless of the PF bit, the DF (Done Flag) bit in the configuration register is set at completion of calibration. The user can either monitor the DF bit or SDO to determine when a calibration is complete. Whichever method is used, the calibration control bits (CC2-CC0) automatically return to logic 0 upon completion of any calibration.

Configuration Register Descriptions

D23(MSB)	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
A1	A0	D3	D2	D1	D0	NU	LPM	WR2	WR1	WR0	U/B

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NU	NU	NU	NU	RS	RV	PF	PSS	DF	CC2	CC1	CC0

BIT	NAME	VALUE		FUNCTION
D23-D22	Latch Outputs, A1-A0	00	R*	Latch Output Pins A1-A0 mimic the D23-D22 Register bits.
D21-D18	Latch Outputs, D3-D0	0000	R*	Latch Output Pins D3-D0 mimic the D21-D18 Register bits.
D17	Not Used, NU	0	R	Must always be logic zero.
D16	Low Power Mode, LPM	0 1	R	Normal Mode (≅ 2.5 mW) Reduced Power Mode (≅ 1 mW)
D15-D13	Word Rate, WR2-0 (Note: Rates valid for XIN = 32.768 kHz)	000 001 010 011 100 101 110 111	R	15.0 Sps (2180 XIN cycles) 30.0 Sps (1092 XIN cycles) 61.6 Sps (532 XIN cycles) 84.5 Sps (388 XIN cycles) 101.1 Sps (324 XIN cycles) 1.88 Sps (17444 XIN cycles) 3.76 Sps (8724 XIN cycles) 7.51 Sps (4364 XIN cycles)
D12	Unipolar/Bipolar, U/B	0 1	R	Bipolar Measurement mode Unipolar Measurement mode
D11-D8	Not Used, NU	0	R	Must always be logic 0.
D7	Reset System, RS	0 1	R	Normal Operation Activate a Reset cycle. To return to normal operation this bit must be written back to logic zero.
D6	Reset Valid , RV	0 1	 R	No reset has occurred or bit has been cleared (read only). Valid Reset has occurred. (Cleared when read.)
D5	Port Flag, PF	0 1	R	Port Flag mode inactive Port Flag mode active
D4	Power Save Select, PSS	0 1	R	Standby Mode (Oscillator active, allows quick power-up) Sleep Mode (Oscillator inactive)
D3	Done Flag, DF	0 1	R	Done Flag bit is cleared (read only). Calibration or Conversion cycle completed (read only).
D2-D0	Calibration Control Bits, CC2-CC0	000 001 010 011 100 101 110 111	R	Normal operation (no calibration) Offset -- Self-Calibration Gain -- Self-Calibration Offset self-cal followed by Gain self-calibration Not Used. Offset -- System Calibration Gain -- System Calibration Not Used.

* R indicates the bit value after the part is reset

Performing Conversions

The CS5529 offers two modes of performing conversions: single conversion and continuous conversions. The sections that follow detail the differences and provides examples illustrating how to use the modes. Note that it is assumed that the configuration register has been initialized before conversions are performed.

Performing Conversions with PF bit = 0

A single conversion is performed after the user transmits the single conversion command (0xC0 Hexadecimal). At the completion of the conversion, the DF (Done Flag) bit of the configuration register will be set to a logic 1. While the conversion is being performed, the user can read the configuration register to determine if the DF bit is set. Once DF has been set, the read conversion data register command (0x96 Hexadecimal) can be issued to read the conversion data register to obtain the conversion data word.

Note: 1)The DF bit of the configuration register will be cleared to logic 0 when the conversion data register, the gain register, or the offset register is read. Reading only the configuration register will not clear the DF flag bit.
2) If another single conversion command is issued to the converter while it is performing a conversion, the filter will abandon the current conversion and restart a new convolution cycle.

Performing Conversions with PF bit = 1

The PF (Port Flag) bit in the configuration register eliminates the need for the user to monitor the DF (Done Flag) in the configuration register to determine if the conversion is available. When PF is set to a logic 1, SDO's output pin behaves as a flag signal indicating when conversions are completed. SDO will fall to logic 0 once a new conversion is complete.

Single Conversion

A single conversion is performed after the user transmits the single conversion command (0xC0 Hexadecimal). At the completion of the conversion, SDO will fall to logic 0 to indicate that the conversion is complete. To acquire the conversion, the user must issue 8 SCLKs with SDI = logic 0 (i.e. the NULL command) to clear the SDO flag. Upon the falling edge of the 8th SCLK, the SDO pin will present the first bit (MSB) of the conversion word. 24 SCLKs (high, then low) are then required to read the conversion word from the port.

Note: 1) The user must not give an explicit command (other than the NULL command) to read the conversion data register when the PF bit is set to logic 1.
2) The data conversion word must be read before a new command can be entered as the converter will remain in the data mode until the conversion word is read.
3) Once the conversion is read the converter returns to the command mode.

Continuous Conversions

Continuous conversions are performed after the user transmits the continuous conversions command (0xA0 Hexadecimal). At the completion of a conversion, SDO will fall to logic 0 to indicate that the conversion is complete. To read the conversion word, the user must issue 8 SCLKs with SDI = logic 0 (i.e. the NULL command) to clear the SDO flag. Upon the falling edge of the 8th SCLK, the SDO pin will present the first bit (MSB) of the conversion word. 24 SCLKs (high, then low) are then required to read the conversion word from the port.

When operating in the continuous conversion mode, the user need not read every conversion. If the user chooses not to read a conversion after SDO falls, SDO will rise one XIN clock cycle before the next conversion word is available and then fall again to signal that another conversion word is available. To exit the continuous conversion mode, the user must issue any valid command, other than the NULL command, to the SDI input when the

SDO flag falls. For instance, the user can just read the conversion data register again to exit the continuous conversion mode.

Note: 1) If the user begins to clear the SDO flag and read the conversion data, this action must be finished before the conversion cycle which is occurring in the background is complete if the user wants to be able to read the new conversion data.
2) If a CC command is issued to the converter while it is performing a conversion, the filter will stop the current conversion and start a new convolution cycle to perform a new conversion.
3) Continuous conversions aren't allowed unless the port flag bit is set in the configuration register.
4) The converter will remain in data mode and continually perform conversions until the exit command is issued (i.e. to exit the user must read a register).

Output Coding

As shown in the Output Conversion Data Register Descriptions, the CS5529 presents output conversions as a 24-bit conversion word. The first 16 bits of the conversion word represent conversion data. The third byte contains two error flag bits.

In the third byte, D7-D4 are always logic 1; D3-D2 are always logic 0; and bits D1-D0 are the two flag bits. The OF (Overrange Flag) bit is set to a logic 1 any time the input signal is: 1) more positive than positive full scale, 2) more negative than zero (unipolar mode), 3) more negative than negative full scale (bipolar mode). It is cleared back to logic 0 whenever a conversion word occurs which is not overranged.The OD (Oscillation Detect) bit is set to a logic 1 any time that an oscillatory condition is detected in the modulator. This does not occur under normal operating conditions, but may occur whenever the input to the converter is extremely overranged. If the OD bit is set, the conversion data bits can be completely erroneous. The OD flag bit will be cleared to logic 0 when the modulator becomes stable.

Table 2 and Table 3 illustrate the output coding for the CS5529. Unipolar conversions are output in binary format and bipolar conversions are output two's complement.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
MSB	14	13	12	11	10	9	8	7	6	5	4
D11	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
3	2	1	LSB	1	1	1	1	0	0	OD	OF

Table 2. Output Conversion Data Register Description (16 bits + flags).

Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFF	>(VFS-1.5 LSB)	7FFF
VFS-1.5 LSB	FFFF ----- FFFE	VFS-1.5 LSB	7FFF ----- 7FFE
VFS/2-0.5 LSB	8000 ----- 7FFF	-0.5 LSB	0000 ----- FFFF
+0.5 LSB	0001 ----- 0000	-VFS+0.5 LSB	8001 ----- 8000
<(+0.5 LSB)	0000	<(-VFS+0.5 LSB)	8000

Note: VFS in the table equals the voltage between ground and full scale for any of the unipolar gain ranges, or the voltage between ± full scale for any of the bipolar gain ranges. See text about error flags under overrange conditions.

Table 3. CS5529 16-bit Output Coding.

Power Supply Arrangements

The CS5529 is designed to operate from single or dual analog supplies and a single digital supply. The following power supply connections are possible:

VA+ = +5 V; VA- = 0 V; VD+ = +3 V to +5 V

VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V to +5 V

VA+ = +3.0 V; VA- = -3.0 V; VD+ = +3 V

Figure 10 illustrates the CS5529 connected with a single +5 V supply to measure differential inputs relative to a common mode of 2.5 V. Figure 11 illustrates the CS5529 connected with ±2.5 V bipolar

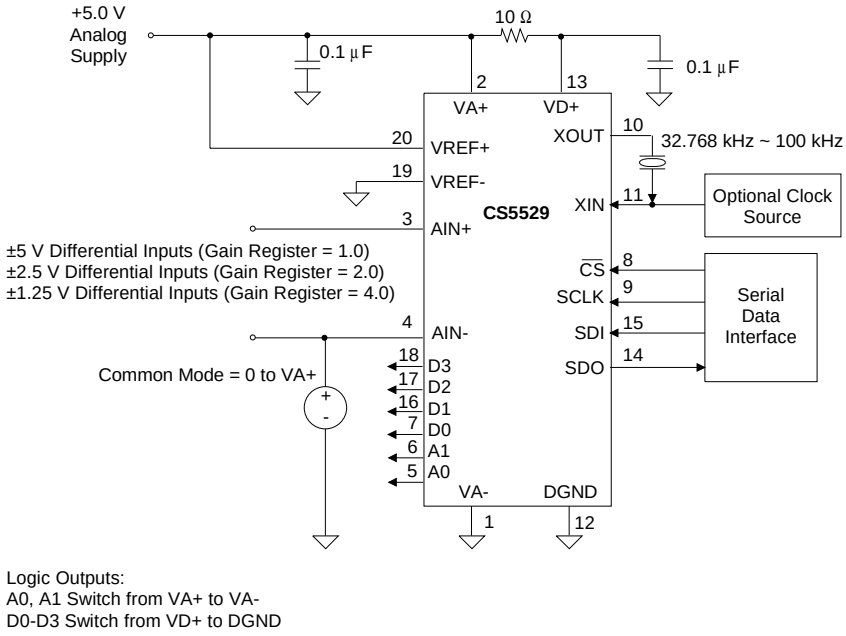


Figure 10. CS5529 Configured with a +5.0 V Analog Supply.

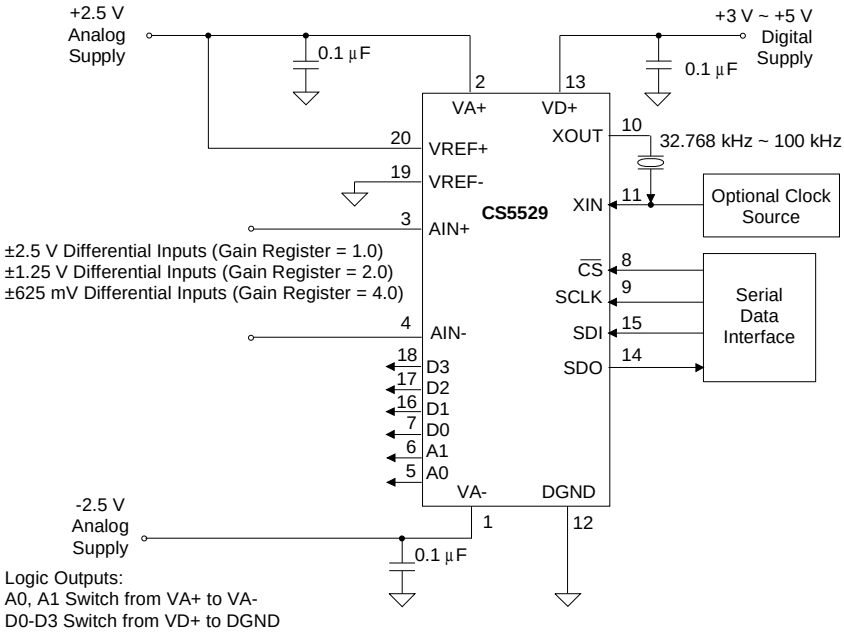


Figure 11. CS5529 Configured with ±2.5 V Analog Supplies.

analog supplies and a +3 V to +5 V digital supply to measure ground referenced bipolar signals. Figure 12 illustrates the CS5529 connected with ±3.0 V bipolar analog supplies and a +3 V digital supply to measure ground referenced bipolar signals.

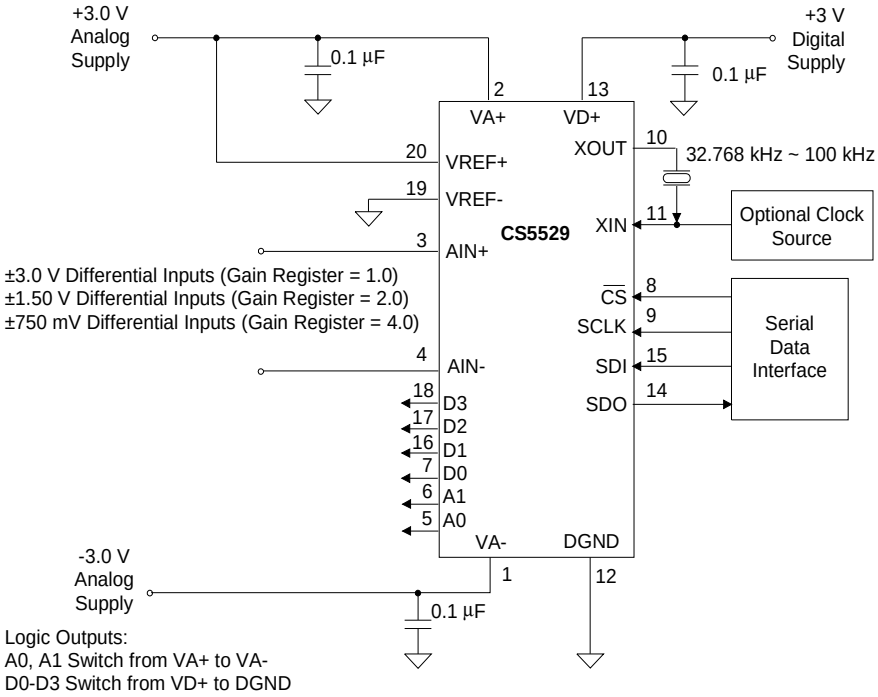


Figure 12. CS5529 Configured with ±3.0 V Supplies.

Getting Started

The CS5529 has many features. From a software programmer's perspective, what should be done first? To begin, a 32.768 kHz crystal takes approximately 500 ms to start-up. To accommodate for this, it is recommended that a software delay of approximately 500 ms to 1 second precede the processor's ADC initialization code before any registers are accessed in the ADC. This delay time is dependent on the start-up delay of the clock source. If a CMOS clock source with no start-up delay is being used to drive the ADC, then this delay is not necessary.

The converters include an on-chip power on reset circuit to automatically reset the ADCs shortly after power up. When power to the CS5529 is applied, the chip is held in a reset condition until the 32.768 kHz oscillator has started and a counter-timer elapses. The counter-timer counts 1002 oscillator clock cycles to make sure the oscillator is fully stable. During this time-out period the serial port logic is reset and the RV (Reset Valid) bit in the configuration register is set to indicate that a valid reset occurred. In normal start-up conditions, this power-on-reset circuit should reset the chip when power is applied. If your application may experience abnormal power start-up conditions, the following sequence of instructions should be performed to guarantee the converter begins proper operation:

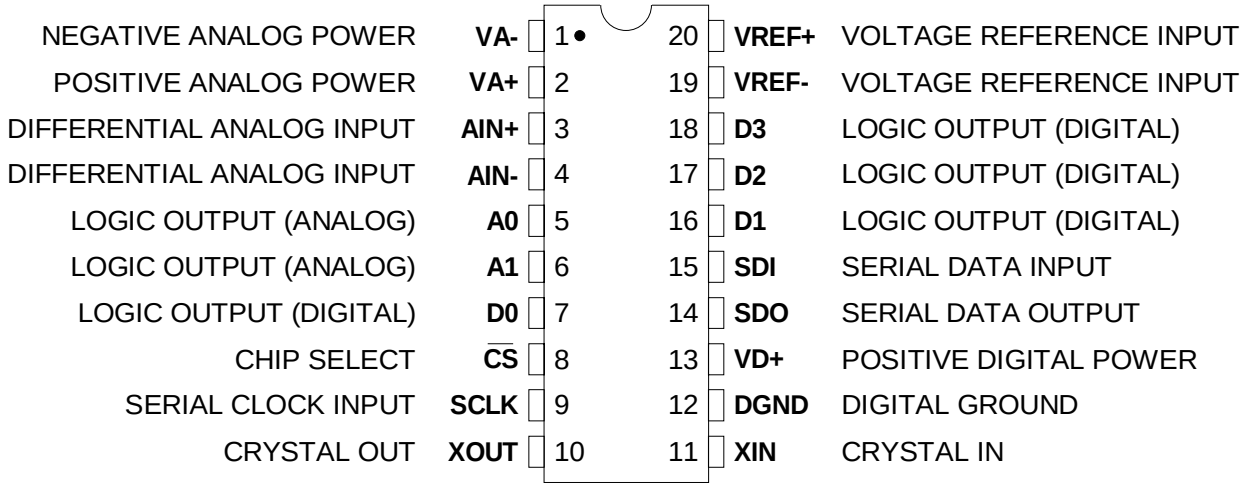
1) After power is applied, initialize the serial port using the serial port synchronization sequence.
2) Write a '1' to the reset bit (RS) of the configuration register to reset the converter.
3) Read the configuration register to determine if the reset valid bit (RV) is set to '1'. If the RV bit is not set, the configuration register should be read again.
4) When the RV bit has been set to '1', reset the RS bit back to '0' by writing to 0x000000 to the configuration register. Note that while the RS bit is set to '1' all other register bits in the ADC will be reset to their default state, and the RS bit must be set to '0' for normal operation of the converters.

Once the RS bit has been set to '0', the ADC is placed in the command state were it waits for a valid command to execute. The next step is to load the configuration register. If you need to do a factory calibration, perform offset and gain calibration steps. Then off-load the offset and gain register contents into EEPROM. These registers can then be initialized to these conditions when the instrument is used in normal operation. Once calibration is ready, input the command to start conversions in either single or continuous conversion mode. Monitor the SDO pin for a flag that the data is ready and read conversion data.

PCB Layout

The CS5529 should be placed entirely over an analog ground plane with the DGND pin of the device connected to the analog ground plane. If the design splits the ground plane, place the analog-digital plane split immediately adjacent to the digital portion of the chip.

PIN DESCRIPTIONS



Clock Generator

XIN; XOUT - Crystal In; Crystal Out, Pins 10, 11.

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock (powered relative to VD+) can be supplied into the XIN pin to provide the master clock for the device.

Control Pins and Serial Data I/O

$\overline{CS}$ - Chip Select, Pin 8.

When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{CS}$ should be changed when SCLK = 0.

SDI - Serial Data Input, Pin 15.

SDI is the input pin of the serial input port. Data will be input at a rate determined by SCLK.

SDO - Serial Data Output, Pin 14.

SDO is the serial data output. It will output a high impedance state if $\overline{CS}$ = 1.

SCLK - Serial Clock Input, Pin 9.

A clock signal on this pin determines the input/output rate of the data for the SDI/SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.

A0, A1 - Logic Outputs (Analog), Pin 5, 6.

The logic states of A0-A1 mimic the states of the D22-D23 bits of the configuration register. Logic Output 0 = VA-, and Logic Output 1 = VA+.

D0, D1, D2, D3 - Logic Outputs (Digital), Pin 7, 16, 17, 18.

The logic states of D0-D3 mimic the states of the D18-D21 bits of the configuration register. Logic Output 0 = DGND, and Logic Output 1 = VD+.

Measurement and Reference Inputs

AIN+, AIN- - Differential Analog Input, Pins 3, 4.

Differential input pins into the device.

VREF+, VREF- - Voltage Reference Input, Pins 20, 19.

Fully differential inputs which establish the voltage reference for the on-chip modulator.

Power Supply Connections

VA+ - Positive Analog Power, Pin 2.

Positive analog supply voltage.

VA- - Negative Analog Power, Pin 1.

Negative analog supply voltage.

VD+ - Positive Digital Power, Pin 13.

Positive digital supply voltage (+3.0 V or +5 V).

DGND - Digital Ground, Pin 12.

Digital Ground.

SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two end points of the A/D Converter transfer function. One end point is located 1/2 LSB below the first code transition and the other end point is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - 3/2 LSB]. Units are in LSBs.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above the voltage on the AIN- pin). When in unipolar mode ($U/\overline{B}$ bit = 1). Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below the voltage on the AIN- pin). When in bipolar mode ($U/\overline{B}$ bit = 0). Units are in LSBs.

ORDERING INFORMATION

Model Number	Linearity Error (Max)	Temperature Range	Package	Lead Free
CS5529-AP	±0.003%	-40°C to +85°C	20-pin 0.3" Plastic DIP	No
CS5529-AS	±0.003%	-40°C to +85°C	20-pin 0.2" Plastic SSOP	No
CS5529-ASZ	±0.003%	-40°C to +85°C	20-pin 0.2" Plastic SSOP	Yes

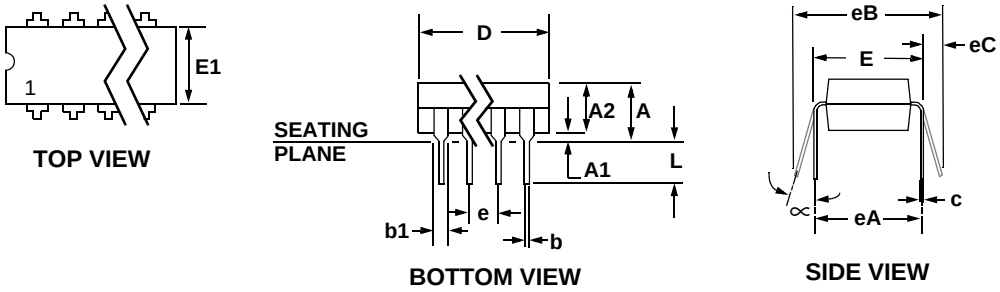
ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model	Peak Relfow Temp	MSL Rating*	Maximum Floor Life
CS5529-AP	260 °C	1	No Limit
CS5529-AS	240 °C	2	365 Days
CS5529-ASZ (Lead Free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

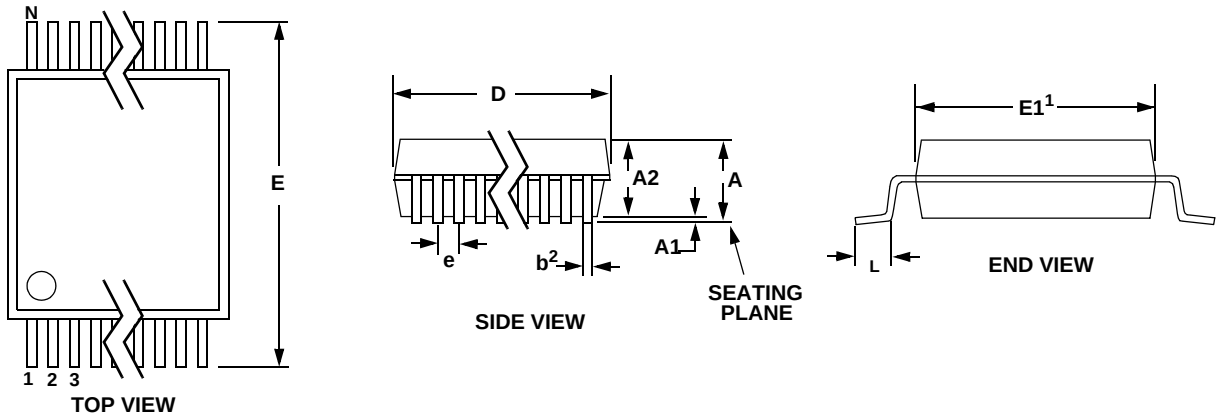
PACKAGE DIMENSIONS

20 PIN PLASTIC (PDIP) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.000	0.210	0.00	5.33
A1	0.015	0.025	0.38	0.64
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b1	0.045	0.070	1.14	1.78
c	0.008	0.014	0.20	0.36
D	0.980	1.060	24.89	26.92
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.090	0.110	2.29	2.79
eA	0.280	0.320	7.11	8.13
eB	0.300	0.430	7.62	10.92
eC	0.000	0.060	0.00	1.52
L	0.115	0.150	2.92	3.81
∝	0°	15°	0°	15°

20L SSOP PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	2,3
D	0.272	0.295	6.90	7.50	1
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	1
e	0.022	0.030	0.55	0.75	
L	0.025	0.041	0.63	1.03	
∝	0°	8°	0°	8°	

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.