

# Current Mode PWM Control Circuit with 50% Max Duty Cycle

## Description

The CS52845 provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS52845 incorporates a new precision temperature-controlled oscillator to minimize variations in frequency. An internal toggle flip-flop, which blanks the output every other clock cycle, limits the duty-cycle range to less than 50%.

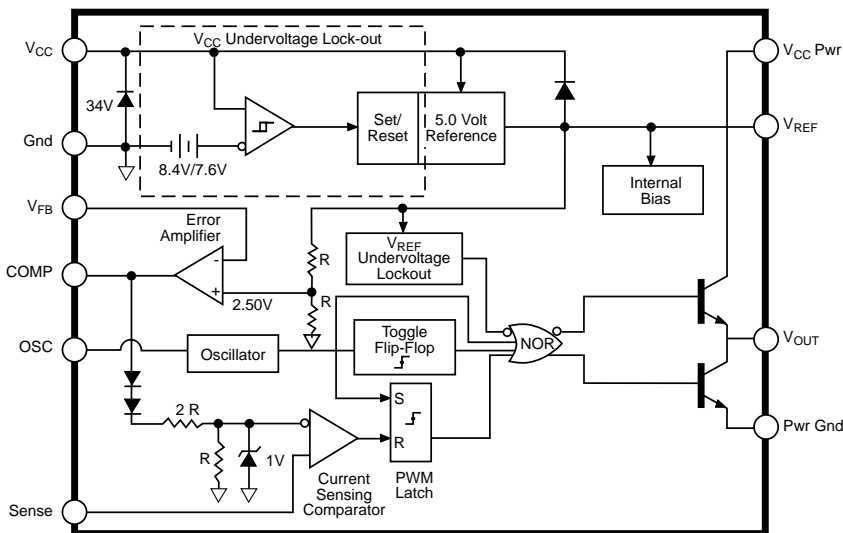
An undervoltage lockout ensures that  $V_{REF}$  is stabilized before the output stage is enabled. In the CS52845 turn on is at 8.4V and turn off at 7.6V.

Other features include low start-up current, pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads, such as gate of a power MOSFET. The output is low in the off state, consistent with N-channel devices.

## Absolute Maximum Ratings

Supply Voltage ( $I_{CC} < 30\text{mA}$ ) .....	Self Limiting
Supply Voltage (Low Impedance Source) .....	30V
Output Current .....	$\pm 1\text{A}$
Output Energy (Capacitive Load) .....	5 $\mu\text{J}$
Analog Inputs ( $V_{FB}$ , $V_{SENSE}$ ) .....	-0.3V to 5.5V
Error Amp Output Sink Current .....	10mA
Lead Temperature Soldering	
Reflow (SMD styles only) .....	60 sec. max above 183°C, 230°C peak

## Block Diagram

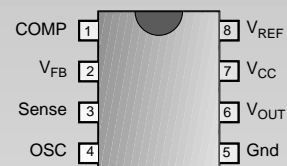


## Features

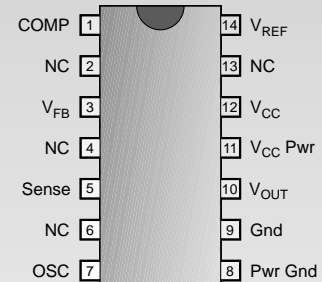
- Optimized for Off-line Control
- Temperature Compensated Oscillator
- 50% Maximum Duty-cycle Clamp
- $V_{REF}$  Stabilized before Output Stage is Enabled
- Low Start-up Current
- Pulse-by-pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 1% Trimmed Bandgap Reference
- High Current Totem Pole Output

## Package Options

### 8L SO Narrow



### 14L SO Narrow



Electrical Characteristics:  $-40 \leq T_A \leq 85^\circ\text{C}$ ;  $V_{CC} = 15\text{V}$  (Note 1);  $R_T = 10\text{k}\Omega$ ;  $C_T = 3.3\text{nF}$  for sawtooth mode unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Reference Section</b>					
Output Voltage	$T_J=25^\circ\text{C}$ , $I_{REF}=1\text{mA}$	4.95	5.00	5.05	V
Line Regulation	$12 \leq V_{CC} \leq 25\text{V}$		6	20	mV
Load Regulation	$1 \leq I_{REF} \leq 20\text{mA}$		6	25	mV
Temperature Stability	(Note 2)		0.2	0.4	mV/ $^\circ\text{C}$
Total Output Variation	Line, Load, Temp. (Note 2)	4.90		5.10	V
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}$ , $T_J=25^\circ\text{C}$ (Note 2)		50		$\mu\text{V}$
Long Term Stability	$T_A=125^\circ\text{C}$ , 1000 Hrs. (Note 2)		5	25	mV
Output Short Circuit	$T_A=25^\circ\text{C}$	-30	-100	-180	mA
<b>Oscillator Section</b>					
Initial Accuracy	Sawtooth Mode, $T_J=25^\circ\text{C}$	47	52	57	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25\text{V}$		0.2	1.0	%
Temperature Stability	Sawtooth Mode $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		5		%
Amplitude	$V_{OSC}$ (peak to peak)		1.7		V
<b>Error Amp Section</b>					
Input Voltage	$V_{COMP}=2.5\text{V}$	2.45	2.50	2.55	V
Input Bias Current	$V_{FB}=0\text{V}$		-0.3	-1.0	$\mu\text{A}$
$A_{VOL}$	$2 \leq V_{OUT} \leq 4\text{V}$	65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1.0		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{V}$	60	70		dB
Output Sink Current	$V_{FB}=2.7\text{V}$ , $V_{COMP}=1.1\text{V}$	2	6		mA
Output Source Current	$V_{FB}=2.3\text{V}$ , $V_{COMP}=5\text{V}$	-0.5	-0.8		mA
$V_{OUT\ HIGH}$	$V_{FB}=2.3\text{V}$ , $R_L=15\text{k}\Omega$ to Gnd	5	6		V
$V_{OUT\ LOW}$	$V_{FB}=2.7\text{V}$ , $R_L=15\text{k}\Omega$ to $V_{REF}$		0.7	1.1	V
<b>Current Sense Section</b>					
Gain	(Notes 3 & 4)	2.85	3.00	3.15	V/V
Maximum Input Signal	$V_{COMP}=5\text{V}$ (Note 3)	0.9	1.0	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{V}$ (Note 3)		70		dB
Input Bias Current	$V_{sense}=0\text{V}$		-2	-10	$\mu\text{A}$
Delay to Output	$T_J=25^\circ\text{C}$ (Note 2)		150	300	ns
<b>Output Section</b>					
Output Low Level	$I_{SINK}=20\text{mA}$		0.1	0.4	V
$I_{SINK}=200\text{mA}$			1.5	2.2	V
Output High Level	$I_{SOURCE}=20\text{mA}$	13.0	13.5		V
	$I_{SOURCE}=200\text{mA}$	12.0	13.5		V
Rise Time	$T_J=25^\circ\text{C}$ , $C_L=1\text{nF}$ (Note 2)		50	150	ns
Fall Time	$T_J=25^\circ\text{C}$ , $C_L=1\text{nF}$ (Note 2)		50	150	ns

Electrical Characteristics: Unless otherwise stated, specifications apply for  $-40 \leq T_A \leq 85^\circ\text{C}$ ;  $V_{CC} = 15\text{V}$  (Note 1);  $R_T = 10\text{k}\Omega$ ;  $C_T = 3.3\text{nF}$  for sawtooth mode.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>■ Total Standby Current</b>					
Start-Up Current			0.5	1.0	mA
Operating Supply Current	$V_{FB}=V_{Sense}=0\text{V}$ $R_T=10\text{k}\Omega$ , $C_T=3.3\text{nF}$		11	17	mA
$V_{CC}$ Zener Voltage	$I_{CC}=25\text{mA}$		34		V
<b>■ PWM Section</b>					
Maximum Duty Cycle		46	48	50	%
Minimum Duty Cycle		0			%
<b>■ Undervoltage Lockout Section</b>					
Start Threshold		7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	7.0	7.6	8.2	V

Notes: 1. Adjust  $V_{CC}$  above the start threshold before setting at 15V.

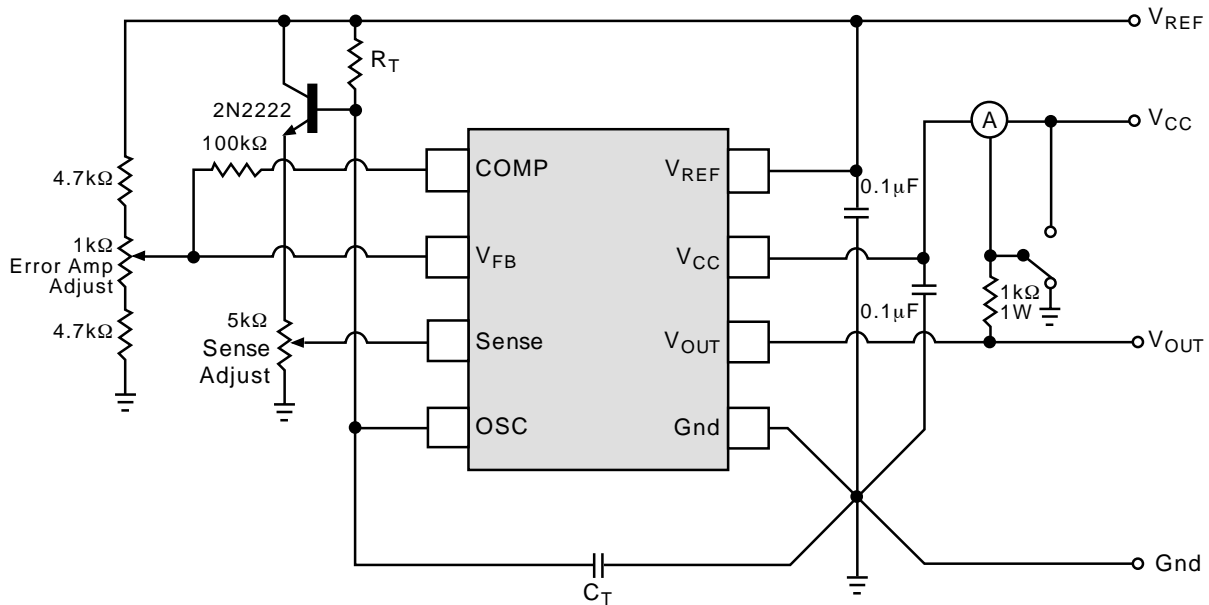
2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at trip point of latch with  $V_{FB}=0$ .

4. Gain defined as:  $A = \frac{\Delta V_{COMP}}{\Delta V_{Sense}}$ ;  $0 \leq V_{Sense} \leq 0.8\text{V}$ .

### Package Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
8L SO Narrow	14L SO Narrow		
1	1	COMP	Error amp output, used to compensate error amplifier.
2	3	$V_{FB}$	Error amp inverting input.
3	5	Sense	Noninverting input to Current Sense Comparator.
4	7	OSC	Oscillator timing network with Capacitor to Ground, resistor to $V_{REF}$ .
5	9	Gnd	Ground.
5	8	Pwr Gnd	Output driver Ground.
6	10	$V_{OUT}$	Output drive pin.
7	11	$V_{CCPWR}$	Output driver positive supply.
7	12	$V_{CC}$	Positive power supply.
8	14	$V_{REF}$	Output of 5V internal reference.
	2,4,6,13	NC	No Connection.



Circuit Description

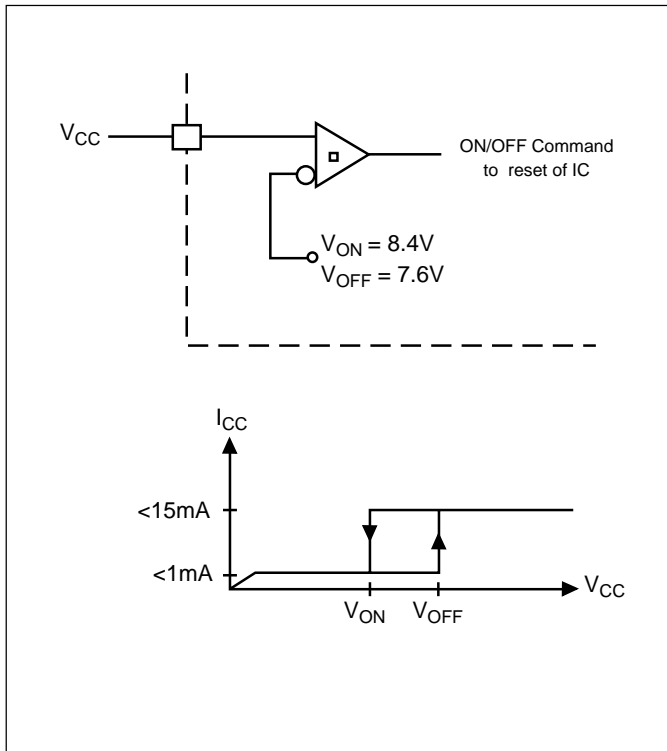


Figure 1: Startup voltage for the CS52845.

Undervoltage Lockout

During Undervoltage Lockout (Figure 1), the output driver is biased to sink minor amounts of current. The output should be shunted to ground with a resistor to prevent activating the power switch with extraneous leakage currents.

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 2). An increase in  $V_{CC}$  causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of OSC components.

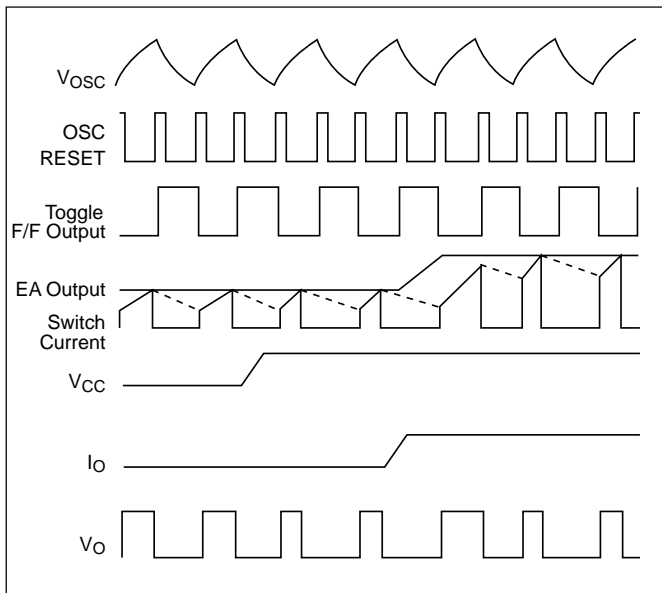


Figure 2: Timing Diagram

### Setting the Oscillator

The times  $T_c$  and  $T_d$  can be determined as follows:

$$t_c = R_T C_T \ln \left( \frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}} \right)$$

$$t_d = R_T C_T \ln \left( \frac{V_{REF} - I_d R_T - V_{lower}}{V_{REF} - I_d R_T - V_{upper}} \right)$$

Substituting in typical values for the parameters in the above formulas:

$$V_{REF} = 5.0V, V_{upper} = 2.7V, V_{lower} = 1.0V, I_d = 8.3mA,$$

then

$$t_c \approx 0.5534 R_T C_T$$

$$t_d = R_T C_T \ln \left( \frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T} \right)$$

For better accuracy  $R_T$  should be  $\geq 10k\Omega$ .

### Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Gnd in a single point ground.

The transistor and  $5k\Omega$  potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

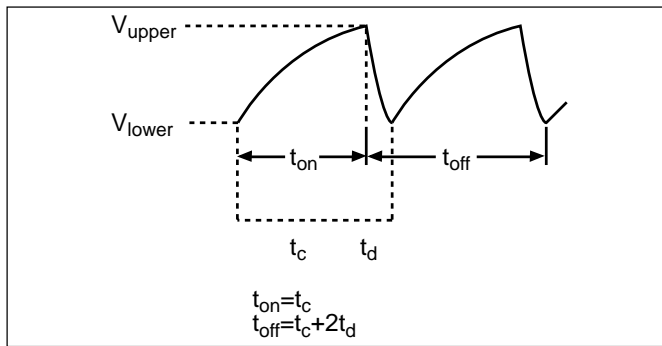


Figure 3: Duty Cycle parameters.

## Package Specification

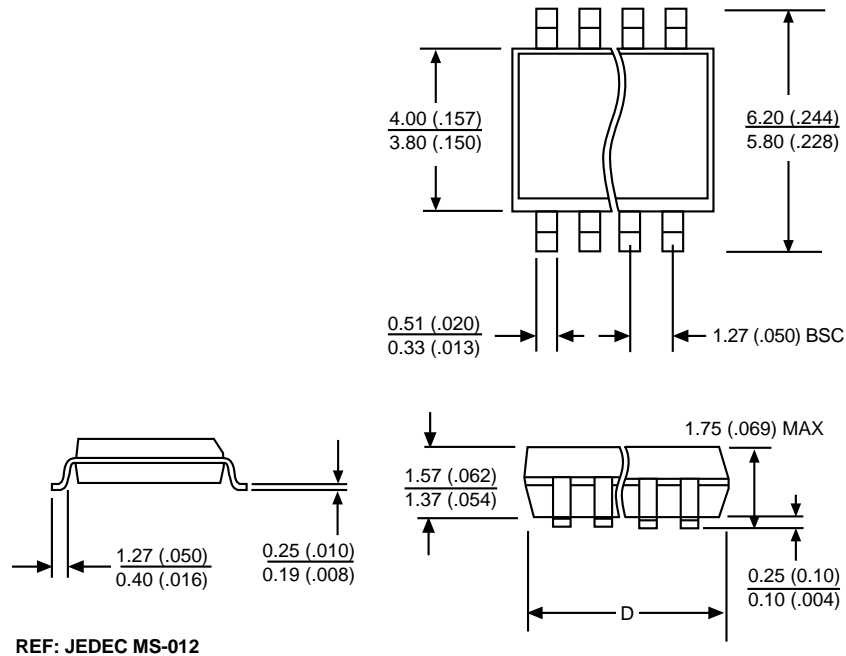
## PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8L SO Narrow	5.00	4.80	.197	.189
14L SO Narrow	8.75	8.55	.344	.337

## PACKAGE THERMAL DATA

Thermal Data		8L SO Narrow	14L SO Narrow	
$R_{\theta JC}$	typ	45	30	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	typ	165	125	$^{\circ}\text{C}/\text{W}$

## Surface Mount Narrow Body (D); 150 mil wide



## Ordering Information

Part Number	Description
CS52845ED8	8L SO Narrow
CS52845EDR8	8L SO Narrow ( <i>tape &amp; reel</i> )
CS52845ED14	14L SO Narrow
CS52845EDR14	14L SO Narrow ( <i>tape &amp; reel</i> )

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.