CS4351

192 kHz Stereo DAC with 2 Vrms Line Out

Features

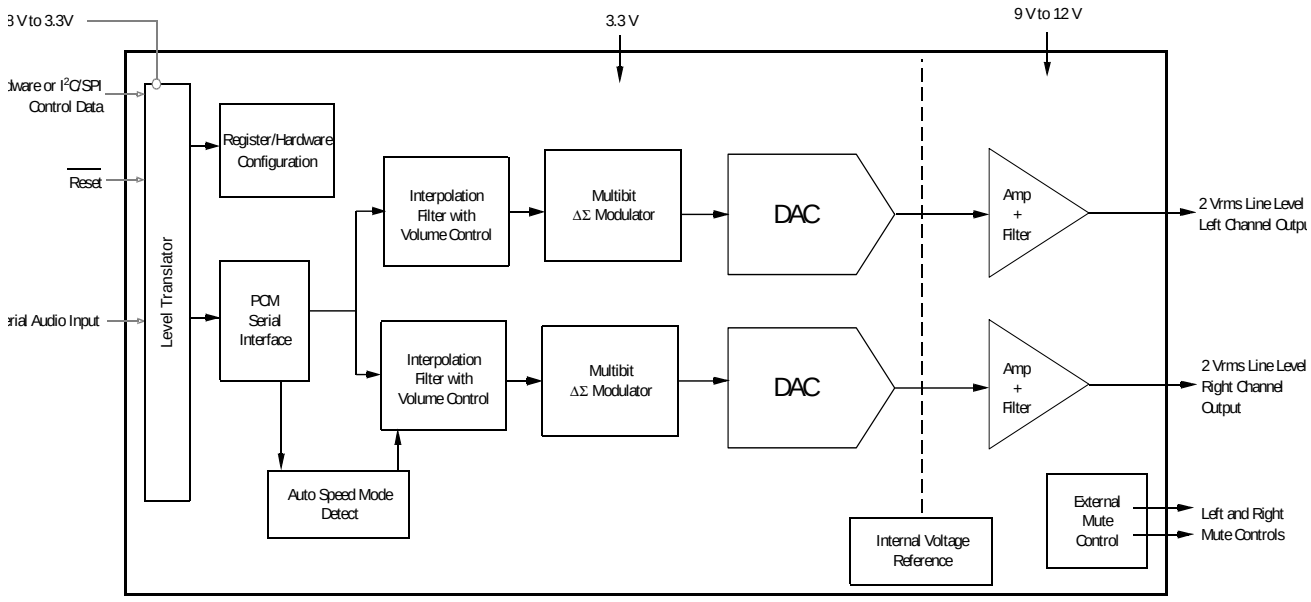
- Multi-Bit Delta-Sigma Modulator
- 24-Bit Conversion
- Up to 192 kHz Sample Rates
- 112 dB Dynamic Range
- -100 dB THD+N
- +3.3 V, +9 to 12 V, and VL Power Supplies
- 2 Vrms Output into 5 kΩ AC Load
- Digital Volume Control with Soft Ramp
  - 119 dB Attenuation
  - 1/2 dB Step Size
  - Zero Crossing Click-Free Transitions
- ATAPI Mixing
- Low Clock Jitter Sensitivity
- Popguard® Technology for Control of Clicks and Pops

Description

The CS4351 is a complete stereo digital-to-analog system including digital interpolation, fifth-order multi-bit delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing, analog filtering, and on-chip 2 Vrms line-level driver. The advantages of this architecture include ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, high tolerance to clock jitter, and a minimal set of external components.

The CS4351 is available in a 20-pin TSSOP package in both Commercial (-10°C - +70°C) and Automotive grades (-40°C to +85°C). The CDB4351 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 37 for complete details.

These features are ideal for cost-sensitive, 2-channel audio systems including DVD players, A/V receivers, set-top boxes, digital TVs and VCRs, mini-component systems, and mixing consoles.



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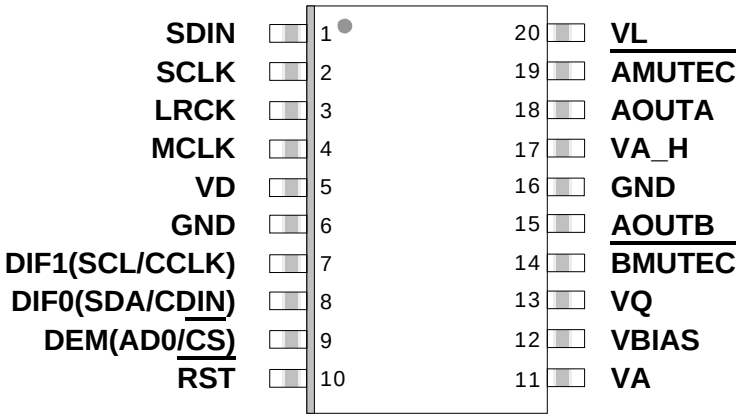
1. PIN DESCRIPTION



Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK	2	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
LRCK	3	**Left / Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	4	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	5	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	6 16	**Ground** (*Input*) - Ground reference.
$\overline{\text{RST}}$	10	**Reset** (*Input*) - Powers down device and resets all internal resisters to their default settings when enabled.
VA	11	**Low Voltage Analog Power** (*Input*) **-** Positive power supply for the analog section.
VBIAS	12	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal DAC.
VQ	13	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VA_H	17	**High Voltage Analog Power** (*Input*) **-** Positive power supply for the analog section.
VL	20	**Serial Audio Interface Power** (*Input*) **-** Positive power for the serial audio interface
$\overline{\text{BMUTEC}}$ $\overline{\text{AMUTEC}}$	14 19	**Mute Control** (*Output*) - Control signal for optional mute circuit.
AOUTB AOUTA	15 18	**Analog Outputs** (*Output*) - The full scale analog line output level is specified in the *Analog Characteristics* table.
Control Port Definitions		
SCL/CCLK	7	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDIN	8	**Serial Control Data** (*Input/Output*) - Input/Output for I²C data. Input for SPI data.
AD0/$\overline{\text{CS}}$	9	**Address Bit 0 / Chip Select** (*Input*) - Chip address bit in I²C Mode. Control Port enable in SPI Mode.
Stand-Alone Definitions		
DIF0 DIF1	8 7	**Digital Interface Format** (*Input*) - Defines the required relationship between the Left Right Clock, Serial Clock, and Serial Audio Data.
DEM	9	**De-emphasis** (*Input*) - Selects the standard 15 µs/50 µs digital de-emphasis filter response for 44.1 kHz sample rates

2. CHARACTERISTICS AND SPECIFICATIONS

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical specifications are derived from performance measurements at T_A = 25 °C, VA_H = 12 V, VA = 3.3 V, VD = 3.3 V.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply	High Voltage Analog power	V_{A_H}	8.55	12	12.6	V
	Low Voltage Analog power	V_A	3.13	3.3	3.47	V
	Digital power	V_D	3.13	3.3	3.47	V
	Interface power	V_L	1.7	3.3	3.47	V
Specified Temperature Range	-CZZ	T_A	-10	-	70	°C
	-DZZ	T_A	-40	-	85	°C

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	High Voltage Analog power	V_{A_H}	-0.3	14	V
	Low Voltage Analog power	V_A	-0.3	3.63	V
	Digital power	V_D	-0.3	3.63	V
	Interface power	V_L	-0.3	3.63	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage	Digital Interface	V_{IN-L}	-0.3	V_L+ 0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS

(Test conditions (unless otherwise specified): input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth 10 Hz to 20 kHz)

Parameter			Symbol	Min	Typ	Max	Unit
All Speed Modes	***Fs = 48, 96, and 192 kHz***						
Dynamic Range (Note 1)	24-bit	unweighted		99	109	-	dB
		A-Weighted		102	112	-	dB
	16-bit	unweighted		-	95	-	dB
		A-Weighted		-	98	-	dB
Total Harmonic Distortion + Noise		(Note 1)	THD+N	-			
	24-bit	0 dB		-	-100	-90	dB
		-20 dB		-	-89	-79	dB
		-60 dB		-	-49	-39	dB
	16-bit	0 dB		-	-92	-	dB
		-20 dB		-	-75	-	dB
		-60 dB		-	-35	-	dB
All Speed Modes							
Idle Channel Noise / Signal-to-noise ratio				-	109	-	dB
Interchannel Isolation		(1 kHz)		-	100	-	dB
Analog Output - All Modes							
Full Scale Output Voltage				1.85	2.00	2.15	Vrms
Common Mode Voltage			V_Q	-	4	-	Vdc
Max DC Current draw from an AOUT pin			I_{OUTmax}	-	10	-	µA
Max Current draw from VQ			I_{Qmax}	-	1	-	µA
Interchannel Gain Mismatch				-	0.1	-	dB
Gain Drift				-	-100	-	ppm/°C
Output Impedance			Z_{OUT}	-	50	-	Ω
AC-Load Resistance			R_L	5	-	-	kΩ
Load Capacitance			C_L	-	-	100	pF

Notes:

1. One-half LSB of triangular PDF dither is added to data.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. See (Note 6)

Parameter		Fast Roll-Off Min	Fast Roll-Off Typ	Fast Roll-Off Max	Unit
Combined Digital and On-Chip Analog Filter Response - Single-Speed Mode - 48 kHz					
Passband (Note 3)	to -0.01 dB corner	0	-	.454	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
StopBand		0.547	-	-	Fs
StopBand Attenuation	(Note 4)	102	-	-	dB
Total Group Delay (Fs = Output Sample Rate)		-	9.4/Fs	-	s
Intra-channel Phase Deviation		-	-	±0.56/Fs	s
Inter-channel Phase Deviation		-	-	0	s
De-emphasis Error (Note 5)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Combined Digital and On-Chip Analog Filter Response - Double-Speed Mode - 96 kHz					
Passband (Note 3)	to -0.01 dB corner	0	-	.430	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 4)	80	-	-	dB
Total Group Delay (Fs = Output Sample Rate)		-	4.6/Fs	-	s
Intra-channel Phase Deviation		-	-	±0.03/Fs	s
Inter-channel Phase Deviation		-	-	0	s
Combined Digital and On-Chip Analog Filter Response - Quad-Speed Mode - 192 kHz					
Passband (Note 3)	to -0.01 dB corner	0	-	.105	Fs
	to -3 dB corner	0	-	.490	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.635	-	-	Fs
StopBand Attenuation	(Note 4)	90	-	-	dB
Total Group Delay (Fs = Output Sample Rate)		-	4.7/Fs	-	s
Intra-channel Phase Deviation		-	-	±0.01/Fs	s
Inter-channel Phase Deviation		-	-	0	s

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(Continued)

Parameter		Slow Roll-Off (Note 2) Min	Typ	Max	Unit
Single-Speed Mode - 48 kHz					
Passband (Note 3)	to -0.01 dB corner	0	-	0.417	Fs
	to -3 dB corner	0	-	0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 4)	64	-	-	dB
Total Group Delay (Fs = Output Sample Rate)		-	6.5/Fs	-	s
Intra-channel Phase Deviation		-	-	±0.14/Fs	s
Inter-channel Phase Deviation		-	-	0	s
De-emphasis Error (Note 5)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Double-Speed Mode - 96 kHz					
Passband (Note 3))	to -0.01 dB corner	0	-	.296	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.792	-	-	Fs
StopBand Attenuation	(Note 4)	70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)		-	3.9/Fs	-	s
Intra-channel Phase Deviation		-	-	±0.01/Fs	s
Inter-channel Phase Deviation		-	-	0	s
Quad-Speed Mode - 192 kHz					
Passband (Note 3))	to -0.01 dB corner	0	-	.104	Fs
	to -3 dB corner	0	-	.481	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.868	-	-	Fs
StopBand Attenuation	(Note 4)	75	-	-	dB
Group Delay		-	4.2/Fs	-	s
Intra-channel Phase Deviation			-	±0.01/Fs	s
Inter-channel Phase Deviation		-	-	0	s

Notes:

2. Slow Roll-off interpolation filter is only available in Control Port mode.
3. Response is clock dependent and will scale with Fs.
4. For Single-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
   For Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
   For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 Fs.
5. De-emphasis is available only in Single-Speed Mode; Only 44.1 kHz De-emphasis is available in Stand-Alone Mode.
6. Amplitude vs. Frequency plots of this data are available in the “Digital Filter Response Plots” on page 31.

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

Parameters		Symbol	Min	Max	Units
MCLK Frequency			1.024	51.2	MHz
MCLK Duty Cycle			45	55	%
Input Sample Rate (Manual selection)	Single-Speed Mode	Fs	4	50	kHz
	Double-Speed Mode	Fs	50	100	kHz
Quad-Speed Mode		Fs	100	200	kHz
Input Sample Rate (Auto selection)	Single-Speed Mode	Fs	4	50	kHz
	Double-Speed Mode	Fs	84	100	kHz
Quad-Speed Mode		Fs	170	200	kHz
LRCK Duty Cycle			40	60	%
SCLK Pulse Width Low		t_{sclkl}	20	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	ns
SCLK Period	Single-Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-
	Double-Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-
	Quad-Speed Mode	t_{sclkw}	$\frac{2}{MCLK}$	-	-
SCLK rising to LRCK edge delay		t_{slrd}	23	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	ns
SDIN valid to SCLK rising setup time		t_{sdlrs}	20	-	ns
SCLK rising to SDIN hold time		t_{sdh}	20	-	ns

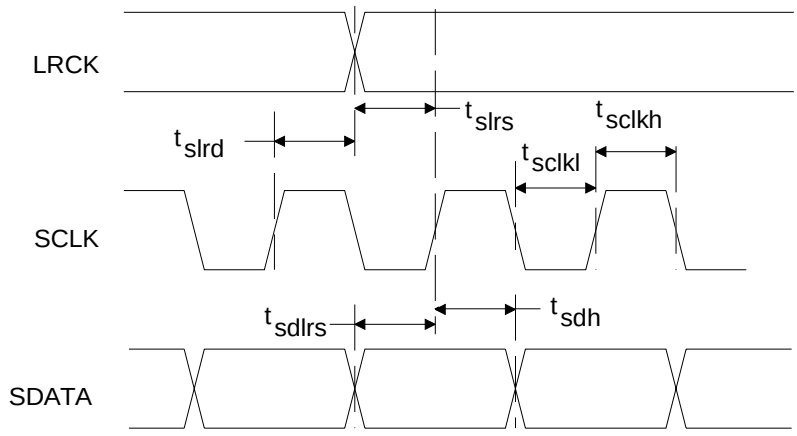


Figure 1. Serial Input Timing

Switching Characteristics - Control Port - I²C® Format

(Inputs: Logic 0 = GND, Logic 1 = VL, C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 7)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

7. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

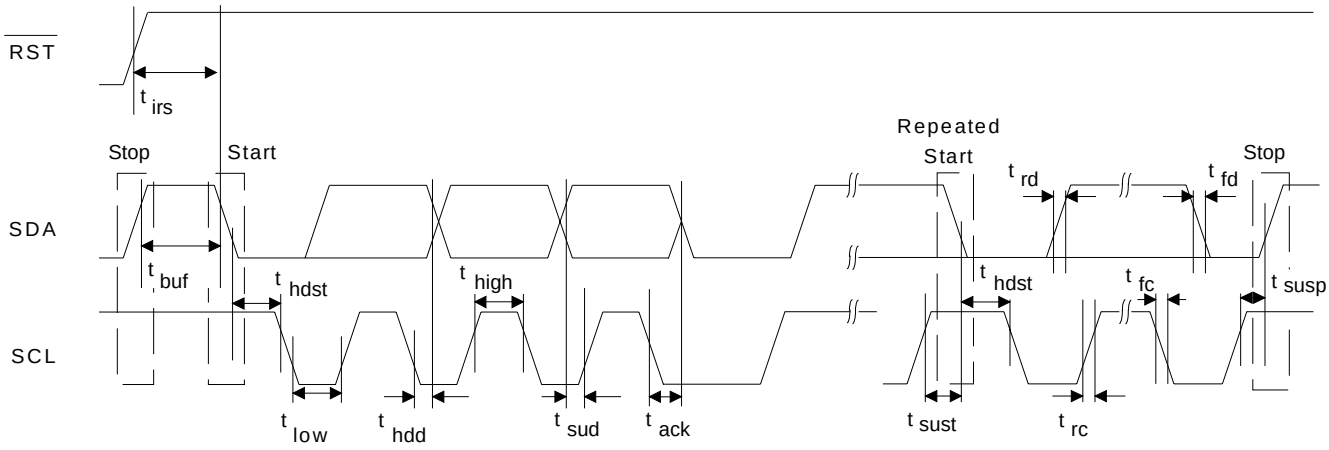


Figure 2. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI™ FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VL, C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 8)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 9)	t_{dh}	17	-	ns
Rise Time of CCLK and CDIN	(Note 10)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 10)	t_{f2}	-	100	ns

Notes:

8. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.
9. Data must be held for sufficient time to bridge the transition time of CCLK.
10. For F_{SCK} < 1 MHz.

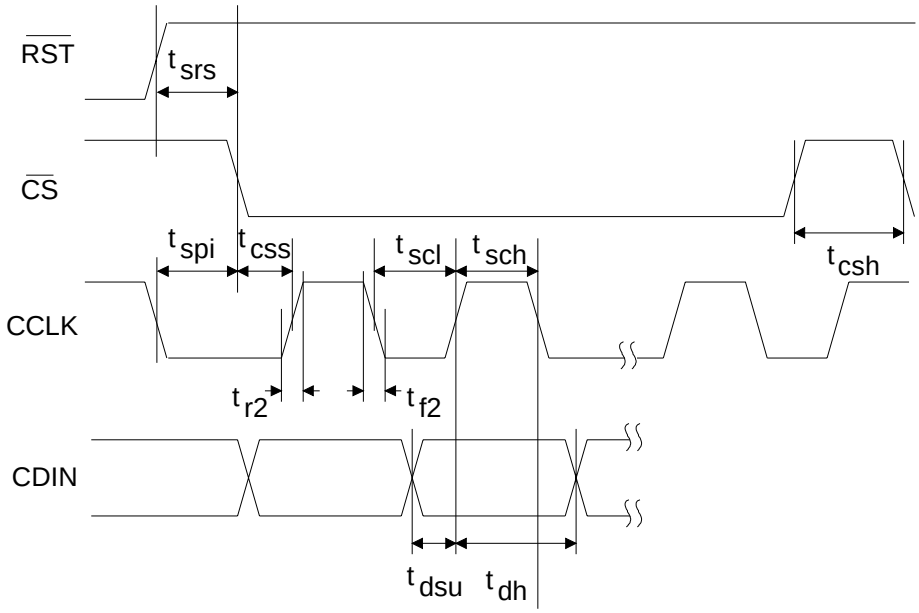


Figure 3. Control Port Timing - SPI Format (Write)

DIGITAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	VL = 3.3 V	V_{IH}	2.0	-	-	V
	VL = 2.5 V	V_{IH}	1.7	-	-	V
	VL = 1.8 V	V_{IH}	0.65•V_L	-	-	V
Low-Level Input Voltage	VL = 3.3 V	V_{IL}	-	-	0.8	V
	VL = 2.5 V	V_{IL}	-	-	0.7	V
	VL = 1.8 V	V_{IL}	-	-	0.33•V_L	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
Maximum MUTEC Drive Current			-	2	-	mA
MUTEC High-Level Output Voltage		V_{OH}	-	VA_H	-	V
MUTEC Low-Level Output Voltage		V_{OL}	-	0	-	V

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current	normal operation, V_{A_H} = 12 V	I_{A_H}	-	15	20	mA
(Note 11)	V_{A_H} = 9 V	I_{A_H}	-	14	19	mA
	V_A= 3.3 V	I_A	-	6	8	mA
	V_D= 3.3 V	I_D	-	21	26	mA
	Interface current (Note 12) V_L= 3.3 V	I_L	-	100	400	µA
	power-down state, all supplies (Note 13)	I_{pd}	-	200	-	µA
Power Dissipation (all supplies)	(Note 11)					
VA_H = 12 V	normal operation		-	270	354	mW
	power-down (Note 13)		-	1	-	mW
VA_H = 9 V	normal operation		-	216	285	mW
	power-down (Note 13)		-	1	-	mW
Power Supply Rejection Ratio (Note 14)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	60	-	dB

Notes:

11. Current consumption increases with increasing FS and increasing MCLK. Typ and Max values are based on highest FS and highest MCLK. Variance between speed modes is small.
12. I_L measured with no external loading on pin 8 (SDA).
13. Power-Down Mode is defined as $\overline{RES}$ pin = Low with all clock and data lines held static.
14. Valid with the recommended capacitor values on VQ and V_{BIAS} as shown in the typical connection diagram in Section 3.

3. TYPICAL CONNECTION DIAGRAM

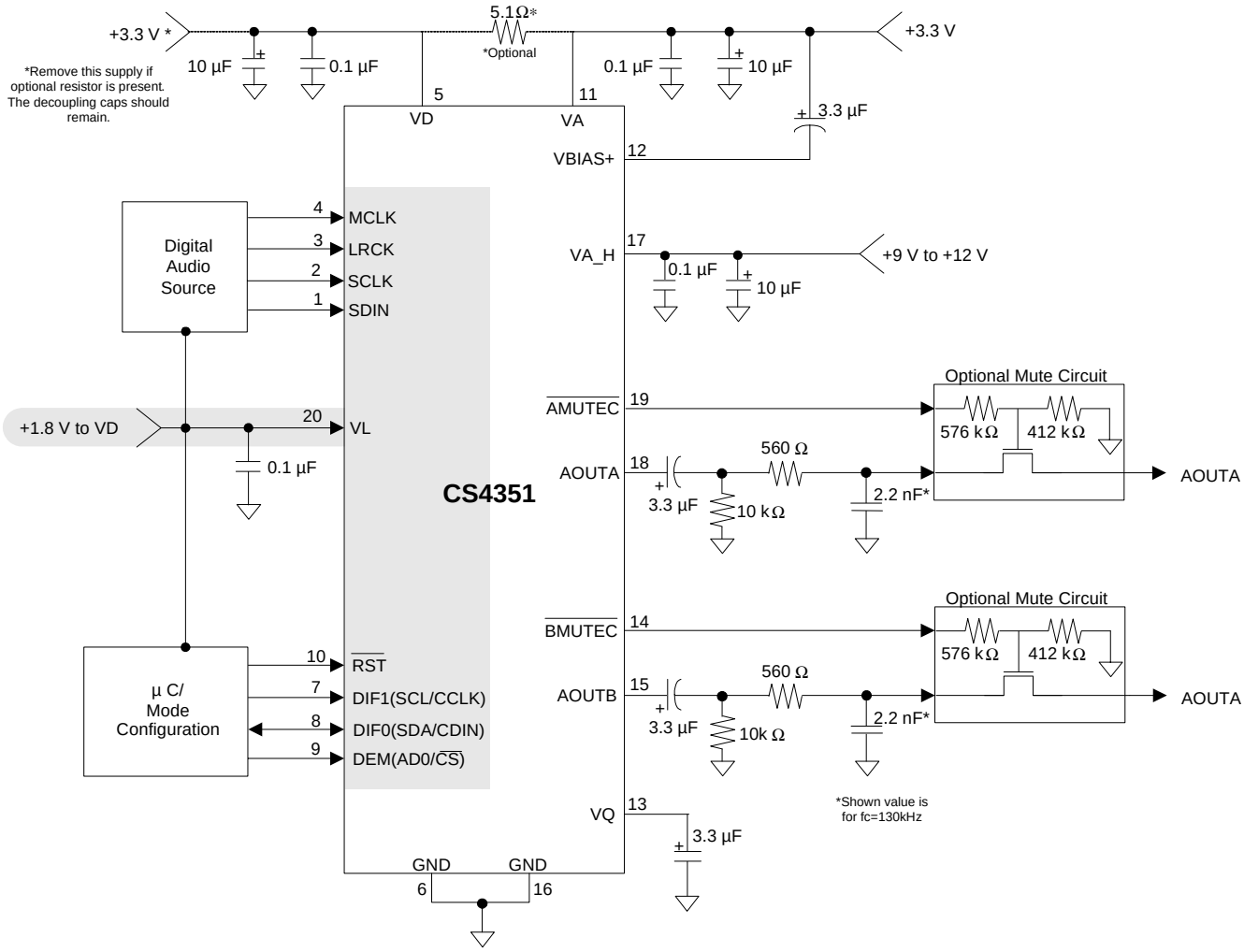


Figure 4. Typical Connection Diagram

4. APPLICATIONS

4.1 Sample Rate Range/Operational Mode Detect

The device operates in one of three operational modes. The allowed sample rate range in each mode will depend on whether the Auto-Detect Defeat bit is enabled/disabled.

4.1.1 Auto-Detect Enabled

The Auto-Detect feature is enabled by default. In this state, the CS4351 will auto-detect the correct mode when the input sample rate (F_S), defined by the LRCK frequency, falls within one of the ranges illustrated in Table 1. Sample rates outside the specified range for each mode are not supported.

Input Sample Rate (F_S)	MODE
4 kHz - 50 kHz	Single-Speed Mode
84 kHz - 100 kHz	Double-Speed Mode
170 kHz - 200 kHz	Quad-Speed Mode

Table 1. CS4351 Auto-Detect

4.1.2 Auto-Detect Disabled

The Auto-Detect feature can be defeated only by the format bits in the control port register 02h. In this state, the CS4351 will not auto-detect the correct mode based on the input sample rate (F_S). The operational mode must then be set manually according to one of the ranges illustrated in Table 2. Please refer to Section 6.2.3 for implementation details. Sample rates outside the specified range for each mode are not supported. In stand-alone mode it is not possible to disable auto-detect of sample rates.

FM1	FM0	Input Sample Rate (F_S)	MODE
0	0	Auto speed mode detect	Auto
0	1	4 kHz - 50 kHz	Single-Speed Mode
1	0	50 kHz - 100 kHz	Double-Speed Mode
1	1	100 kHz - 200 kHz	Quad-Speed Mode

Table 2. CS4351 Mode Select

4.2 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The left/right clock, defined also as the input sample rate (F_S), must be synchronously derived from the MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 3 through 5.

Refer to Section 4.3 for the required SCLK timing associated with the selected Digital Interface Format and to the “Switching Specifications - Serial Audio Interface” section on page 10 for the maximum allowed clock frequencies.

Sample Rate (kHz)	MCLK (MHz)					
	256x	384x	512x	768x	1024x	1152x
32	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640
44.1	11.2896	16.9344	22.5792	33.8688	45.1584	
48	12.2880	18.4320	24.5760	36.8640	49.1520	

Table 3. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 4. Double-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	64x	96x	128x	192x	256x
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 5. Quad-Speed Mode Standard Frequencies

= Denotes clock modes which are NOT auto detected

4.3 Digital Interface Format

The device will accept audio samples in 1 of 4 digital interface formats in Stand-Alone mode, as illustrated in Table 6, and 1 of 6 formats in Control Port mode, as illustrated in Table 7.

4.3.1 Stand-Alone Mode

The desired format is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between the LRCK, SCLK and SDIN, see Figures 5 through 7. For all formats, SDIN is valid on the rising edge of SCLK. Also, SCLK must have at least 32 cycles per LRCK period in format 2, and 48 cycles per LRCK period in format 3.

DIF0	DIF1	DESCRIPTION	FORMAT	FIGURE
0	0	I^2S, up to 24-bit Data	0	6
0	1	Left Justified, up to 24-bit Data	1	5
1	0	Right Justified, 24-bit Data	2	7
1	1	Right Justified, 16-bit Data	3	7

Table 6. Digital Interface Format - Stand-Alone Mode

4.3.2 Control Port Mode

The desired format is selected via the DIF2, DIF1 and DIF0 bits in the Mode Control 2 register (see section Section 6.2.1). For an illustration of the required relationship between LRCK, SCLK and SDIN, see Figures 5 through 7. For all formats, SDIN is valid on the rising edge of SCLK. Also, SCLK must have at

least 32 cycles per LRCK period in format 2, 48 cycles in format 3, 40 cycles in format 4, and 36 cycles in format 5.

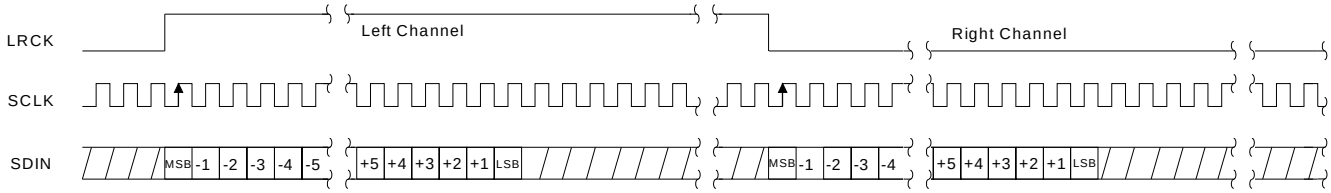


Figure 5. Left-Justified up to 24-Bit Data

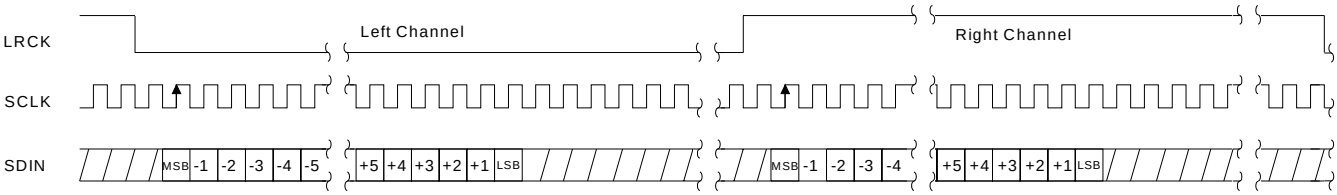


Figure 6. I²S, up to 24-Bit Data

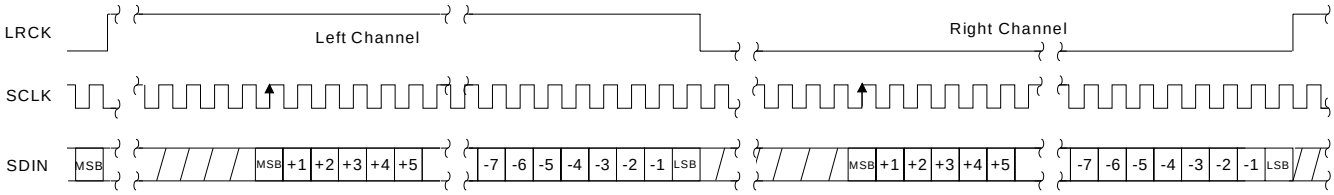


Figure 7. Right-Justified Data

4.4 De-Emphasis Control

The device includes on-chip digital de-emphasis. Figure 8 shows the de-emphasis curve for F_S equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

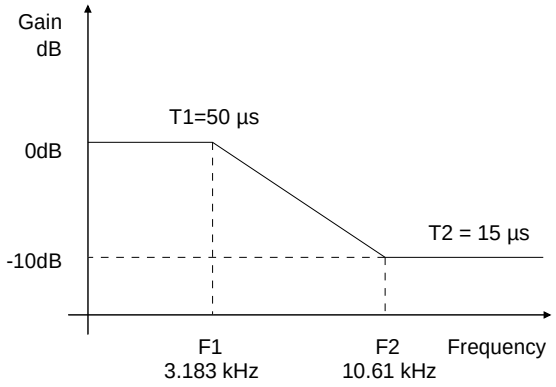


Figure 8. De-Emphasis Curve

Note: De-emphasis is only available in Single-Speed Mode.

4.4.1 Stand-Alone Mode

When pulled to VL the DEM pin activates the 44.1 kHz de-emphasis filter. When pulled to GND the DEM pin turns off the de-emphasis filter.

4.4.2 Control Port Mode

The Mode Control bits selects either the 32, 44.1, or 48 kHz de-emphasis filter. Please see Section 6.2.2 for the desired de-emphasis control.

4.5 Recommended Power-Up Sequence

4.5.1 Stand-Alone Mode

1. Hold $\overline{\text{RST}}$ low until the power supplies and configuration pins are stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in Section 4.2. In this state, the control port is reset to its default settings, VQ will remain low, and VBIAS will be connected to VA.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low and will initiate the Stand-Alone power-up sequence after approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode).

4.5.2 Control Port Mode

1. Hold $\overline{\text{RST}}$ low until the power supply is stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in Section 4.2. In this state, the control port is reset to its default settings, VQ will remain low, and VBIAS will be connected to VA.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low.
3. Perform a control port write to the CP_EN bit prior to the completion of approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode). The desired register settings can be loaded while keeping the PDN bit set to 1.
4. Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximately 50 µs when the POPG bit is set to 0. If the POPG bit is set to 1, see Section 4.6 for a complete description of power-up timing.

4.6 Popguard® Transient Control

The CS4351 uses a novel technique to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when the $\overline{\text{RST}}$ pin is toggled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

4.6.1 Power-Up

When the device is initially powered-up, the audio outputs, AOUTA and AOUTB, are clamped to GND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing audible power-up transients.

4.6.2 Power-Down

To prevent audible transients at power-down, the device must first enter its power-down state. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTA and AOUTB. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

4.6.3 Discharge Time

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning on the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

4.7 Mute Control

The Mute Control pins go active during power-up initialization, reset, muting (see Section 6.4.3), or if the MCLK to LRCK ratio is incorrect. These pins are intended to be used as control for external mute circuits to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. Please see the "Typical Connection Diagram" on page 14 for a suggested mute circuit for single supply systems. This FET circuit must be placed in series after the RC filter, otherwise noise may occur during muting conditions. Further ESD protection will need to be taken into consideration for the FET used. If dual supplies are available, the BJT mute circuit from Figure 12 in the CS4398 datasheet (active Low) may be used.

4.8 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4351 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 4 shows the recommended power arrangements, with VA_H, VA, VD, and VL connected to clean supplies. If the ground planes are split between digital ground and analog ground, the GND pins of the CS4351 should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the VBIAS and VQ pins in order to avoid unwanted coupling into the DAC.

4.8.1 Capacitor Placement

Decoupling capacitors should be placed as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin.

Note: All decoupling capacitors should be referenced to analog ground.

The CDB4351 evaluation board demonstrates the optimum layout and power supply arrangements.

4.9 Control Port Interface

The control port is used to load all the internal register settings (see Section 6). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in one of two modes: I²C or SPI.

4.9.1 MAP Auto Increment

The device has MAP (memory address pointer) auto increment capability enabled by the INCR bit (also the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

4.9.2 I²C Mode

In the I²C mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL (see Figure 9 for the clock to data relationship). There is no $\overline{CS}$ pin. Pin AD0 enables the user to alter the chip address (100110[AD0][R/$\overline{W}$]) and should be tied to VL or GND as required, before powering up the device. If the device ever detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected.

4.9.2.1 I²C Write

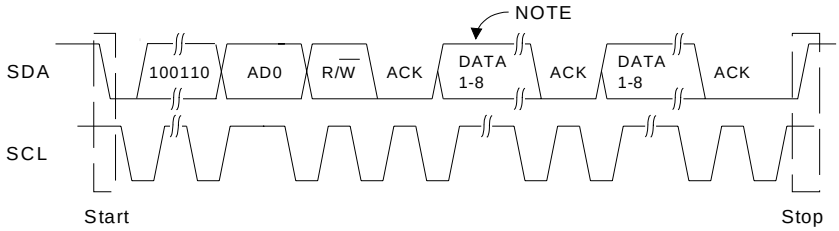
To write to the device, follow the procedure below while adhering to the control port Switching Specifications in Section 8.

1. Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 100110. The seventh bit must match the setting of the AD0 pin, and the eighth must be 0. The eighth bit of the address byte is the R/$\overline{W}$ bit.
2. Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.
3. Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.
4. If the INCR bit (see Section 4.9.1) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I²C writes to other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

4.9.2.2 I²C Read

To read from the device, follow the procedure below while adhering to the control port Switching Specifications.

1. Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 100110. The seventh bit must match the setting of the AD0 pin, and the eighth must be 1. The eighth bit of the address byte is the R/$\overline{W}$ bit.
2. After transmitting an acknowledge (ACK), the device will then transmit the contents of the register pointed to by the MAP. The MAP register will contain the address of the last register written to the MAP, or the default address (see Section 4.10.2) if an I²C read is the first operation performed on the device.
3. Once the device has transmitted the contents of the register pointed to by the MAP, issue an ACK.
4. If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock and issue an ACK after each byte until all the desired registers are read, then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from steps 1 and 2 from the I²C Write instructions followed by step 1 of the I²C Read section. If no further reads from other registers are desired, initiate a STOP condition to the bus.



NOTE: If operation is a write, this byte contains the Memory Address Pointer, MAP. If operation is a read, this byte contains the data of the register pointed to by the MAP.

Figure 9. Control Port Timing, I²C Mode

4.9.3 SPI Mode

In SPI mode, data is clocked into the serial control data line, CDIN, by the serial control port clock, CCLK (see Figure 10 for the clock to data relationship). There is no AD0 pin. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the control port. When the device detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

4.9.3.1 SPI Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in Section 8.

1. Bring $\overline{CS}$ low.
2. The address byte on the CDIN pin must then be 10011000.
3. Write to the memory address pointer, MAP. This byte points to the register to be written.

4. Write the desired data to the register pointed to by the MAP.
5. If the INCR bit (see Section 4.9.1) is set to 1, repeat the previous step until all the desired registers are written, then bring CS high.
6. If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring CS high, and follow the procedure detailed from step 1. If no further writes to other registers are desired, bring CS high.

)

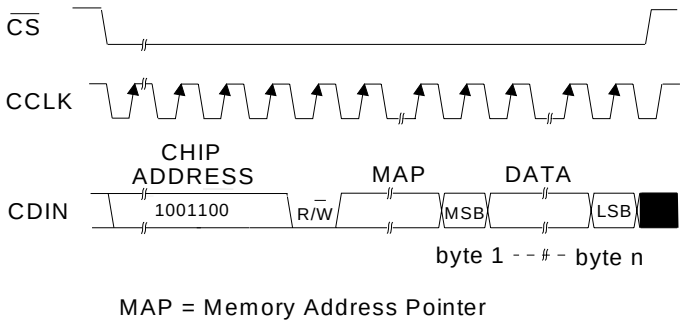


Figure 10. Control Port Timing, SPI mode

4.10 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

4.10.1 INCR (AUTO MAP INCREMENT ENABLE)

Default = '0'
0 - Disabled
1 - Enabled

4.10.2 MAP (MEMORY ADDRESS POINTER)

Default = '0000'

5. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
1h	Chip ID	PART4	PART3	PART2	PART1	PART0	REV2	REV1	REV0
	default	1	1	1	1	1	-	-	-
2h	Mode Control	Reserved	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
	default	0	0	0	0	0	0	0	0
3h	Volume, Mixing, and Inversion Control	VOLB=A	INVERTA	INVERTB	Reserved	ATAPI3	ATAPI2	ATAPI1	ATAPI0
	default	0	0	0	0	1	0	0	1
4h	Mute Control	AMUTE	Reserved	MUTEC A=B	MUTE_A	MUTE_B	Reserved	Reserved	Reserved
	default	1	0	0	0	0	0	0	0
5h	Channel A Volume Control	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
	default	0	0	0	0	0	0	0	0
6h	Channel B Volume Control	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
	default	0	0	0	0	0	0	0	0
7h	Ramp and Filter Control	SZC1	SZC0	RMP_UP	RMP_DN	Reserved	FILT_SEL	Reserved	Reserved
	default	1	0	1	1	0	0	0	1
8h	Misc. Control	PDN	CPEN	FREEZE	Reserved	Reserved	Reserved	Reserved	Reserved
	default	1	0	0	0	0	0	0	0

6. REGISTER DESCRIPTION

** All register access is R/W unless specified otherwise**

6.1 Chip ID - Register 01h

7	6	5	4	3	2	1	0
PART4	PART3	PART2	PART1	PART0	REV2	REV1	REV0
1	1	1	1	1	-	-	-

Function:

This register is Read-Only. Bits 7 through 3 are the part number ID which is 11111b and the remaining Bits (2 through 0) are for the chip revision (Rev. A = 000, Rev. B = 001, ...)

6.2 Mode Control 1 - Register 02h

7	6	5	4	3	2	1	0
Reserved	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
0	0	0	0	0	0	0	0

6.2.1 Digital Interface Format (DIF2:0) Bits 6-4

Function:

These bits select the interface format for the serial audio input.

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 5 through 7.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	**0**	**0**	**Left Justified, up to 24-bit data**	**0 (Default)**	5
0	0	1	I^2S, up to 24-bit data	1	6
0	1	0	Right Justified, 16-bit data	2	7
0	1	1	Right Justified, 24-bit data	3	7
1	0	0	Right Justified, 20-bit data	4	7
1	0	1	Right Justified, 18-bit data	5	7
1	1	0	Reserved		
1	1	1	Reserved		

Table 7. Digital Interface Formats

6.2.2 De-Emphasis Control (DEM1:0) Bits 3-2.

Default = 0
00 - No De-emphasis
01 - 44.1 kHz De-emphasis
10 - 48 kHz De-emphasis
11 - 32 kHz De-emphasis

Function:

Selects the appropriate digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (See Figure 11.)

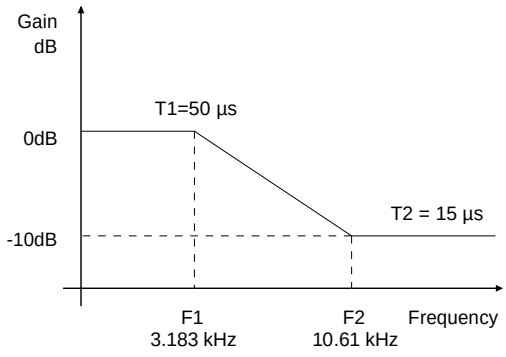


Figure 11. De-Emphasis Curve

Note: De-emphasis is only available in Single-Speed Mode

6.2.3 Functional Mode (FM) Bits 1-0

Default = 00
00 - Auto speed mode detect
01 - Single-Speed Mode (4 to 50 kHz sample rates)
10 - Double-Speed Mode (50 to 100 kHz sample rates)
11 - Quad-Speed Mode (100 to 200 kHz sample rates)

Function:

Selects the required range of input sample rates or DSD Mode.

6.3 Volume Mixing and Inversion Control - Register 03h

B7	B6	B5	B4	B3	B2	B1	B0
VOLB=A	INVERT A	INVERT B	Reserved	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	0	0	0	1	0	0	1

6.3.1 Channel A Volume = Channel B Volume (VOLB=A) Bit 7

Function:

When set to 0 (default) the AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes.

When set to 1 the volume on both AOUTA and AOUTB are determined by the A Channel Attenuation and Volume Control Bytes, and the B Channel Bytes are ignored.

6.3.2 Invert Signal Polarity (Invert_A) Bit 6

Function:

When set to 1, this bit inverts the signal polarity of channel A.

When set to 0 (default), this function is disabled.

6.3.3 Invert Signal Polarity (Invert_B) Bit 5

Function:

When set to 1, this bit inverts the signal polarity of channel B.

When set to 0 (default), this function is disabled.

6.3.4 ATAPI Channel Mixing and Muting (ATAPI3:0) Bits 3-0

Default = 1001 - AOUTA=aL, AOUTB=bR (Stereo)

Function:

The CS4351 implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 8 and Figure 12 for additional information.

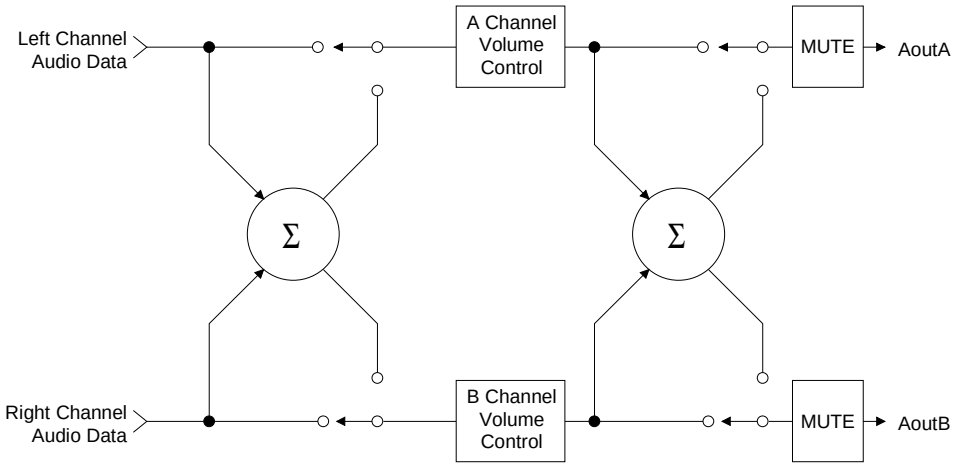


Figure 12. ATAPI Block Diagram

ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA	AOUTB
0	0	0	0	MUTE	MUTE
0	0	0	1	MUTE	bR
0	0	1	0	MUTE	bL
0	0	1	1	MUTE	b[(L+R)/2]
0	1	0	0	aR	MUTE
0	1	0	1	aR	bR
0	1	1	0	aR	bL
0	1	1	1	aR	b[(L+R)/2]
1	0	0	0	aL	MUTE
1	0	0	1	aL	bR
1	0	1	0	aL	bL
1	0	1	1	aL	b[(L+R)/2]
1	1	0	0	a[(L+R)/2]	MUTE
1	1	0	1	a[(L+R)/2]	bR
1	1	1	0	a[(L+R)/2]	bL
1	1	1	1	a[(L+R)/2]	b[(L+R)/2]

Table 8. ATAPI Decode

6.4 Mute Control - Register 04h

7	6	5	4	3	2	1	0
AMUTE	Reserved	MUTEC A=B	MUTE_A	MUTE_B	Reserved	Reserved	Reserved
1	0	0	0	0	0	0	0

6.4.1 Auto-Mute (AMUTE) Bit 7

Function:

When set to 1 (default), the Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period. When set to 0, this function is disabled

6.4.2 AMUTEC = BMUTEC (MUTEC A=B) Bit 5

Function:

When set to 0 (default), the AMUTEC and BMUTEC pins operate independently.

When set to 1, the individual controls for AMUTEC and BMUTEC are internally connected through an AND gate prior to the output pins. Therefore, the external AMUTEC and BMUTEC pins will go active only when the requirements for both AMUTEC and BMUTEC are valid.

6.4.3 A Channel Mute (MUTE_A) Bit 4
B Channel Mute (MUTE_B) Bit 3

Function:

When set to 1, the Digital-to-Analog converter output will mute. The quiescent voltage on the output will be retained. The muting function is effected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register. The corresponding MUTEC pin will go active following any ramping due to the soft and zero cross function.

When set to 0 (default), this function is disabled.

6.5 Channel A Volume Control - Register 05h
Channel B Volume Control - Register 06h

7	6	5	4	3	2	1	0
VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0	0	0	0	0	0	0	0

6.5.1 Digital Volume Control (VOL7:0) Bits 7-0

Default = 00h (0 dB)

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1/2 dB increments from 0 to -127.5 dB. Volume settings are decoded as shown in Table 9. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Power and Muting Control register.

The actual attenuation is determined by taking the decimal value of the volume register and multiplying by 6.02/12.

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
00000001	1	-0.5 dB
00000110	6	-3.0 dB
11111111	255	-127.5 dB

Table 9. Example Digital Volume Settings

6.6 Ramp and Filter Control - Register 07h

7	6	5	4	3	2	1	0
SZC1	SZC0	RMP_UP	RMP_DN	Reserved	FILT_SEL	Reserved	Reserved
1	0	1	1	0	0	0	1

6.6.1 Soft Ramp and Zero Cross Control (SZC1:0) Bits 7-6

Default = 10

SZC1	SZC0	Description
0	0	Immediate Change
0	1	Zero Cross
1	0	Soft Ramp
1	1	Soft Ramp on Zero Crossings

Function:

Immediate Change

When Immediate Change is selected all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp PCM

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp and Zero Cross

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

6.6.2 Soft Volume Ramp-Up After Error (RMP_UP) Bit 5

Function:

When set to 1 (default), an un-mute will be performed after executing a filter mode change, after a LRCK/MCLK ratio change or error, and after changing the Functional Mode. This un-mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

When set to 0, an immediate un-mute is performed in these instances.

Note: For best results, it is recommended this feature be used in conjunction with the RMP_DN bit.

6.6.3 Soft Ramp-Down Before Filter Mode Change (RMP_DN) Bit 4

Function:

When set to 1 (default), a mute will be performed prior to executing a filter mode change. This mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

When set to 0, an immediate mute is performed prior to executing a filter mode change.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_UP bit.

6.6.4 Interpolation Filter Select (FILT_SEL) Bit 2

Function:

When set to 0 (default), the Interpolation Filter has a fast roll off.

When set to 1, the Interpolation Filter has a slow roll off.

The specifications for each filter can be found in the "Combined Interpolation & On-Chip Analog Filter Response" section on page 8, and response plots can be found in Figures 15 to 36.

6.7 Misc Control - Register 08h

7	6	5	4	3	2	1	0
PDN	CPEN	FREEZE	Reserved	Reserved	Reserved	Reserved	Reserved
1	0	0	0	0	0	0	0

6.7.1 Power Down (PDN) Bit 7

Function:

When set to 1 (default), the entire device will enter a low-power state and the contents of the control registers will be retained. The power-down bit defaults to '1' on power-up and must be disabled before normal operation in Control Port mode can occur. This bit is ignored if CPEN is not set.

6.7.2 Control Port Enable (CPEN) Bit 6

Function:

This bit is set to 0 by default, allowing the device to power-up in Stand-Alone Mode. Control Port Mode can be accessed by setting this bit to 1. This will allow operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode.

6.7.3 Freeze Controls (Freeze) Bit 5

Function:

When set to 1, this function allows modifications to be made to the registers without the changes taking effect until FREEZE is set back to 0. To make multiple changes in the Control Port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

When set to 0 (default), register changes take effect immediately.

7. DIGITAL FILTER RESPONSE PLOTS

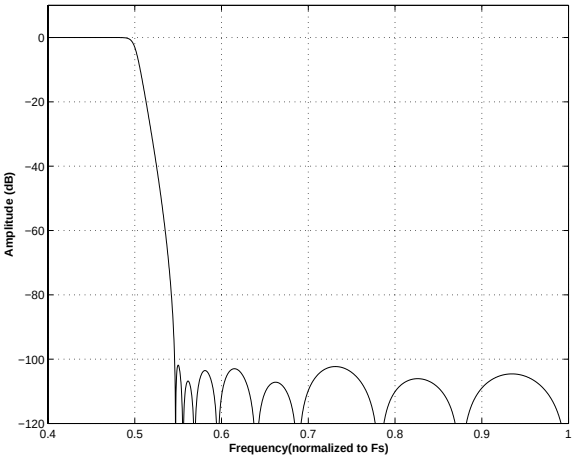


Figure 13. Single-Speed (fast) Stopband Rejection

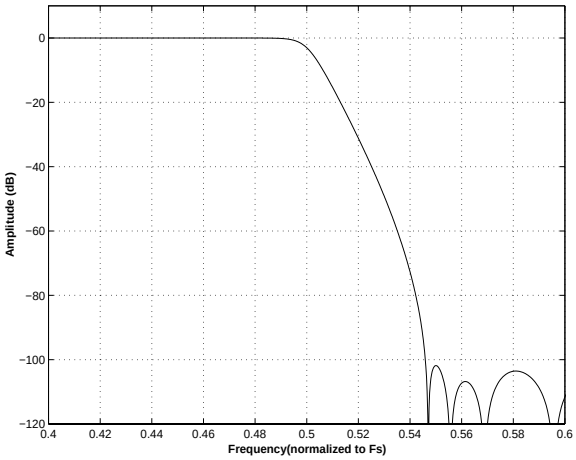


Figure 14. Single-Speed (fast) Transition Band

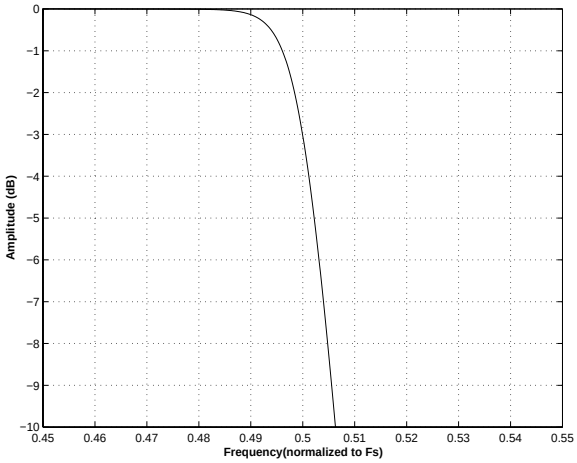


Figure 15. Single-Speed (fast) Transition Band (detail)

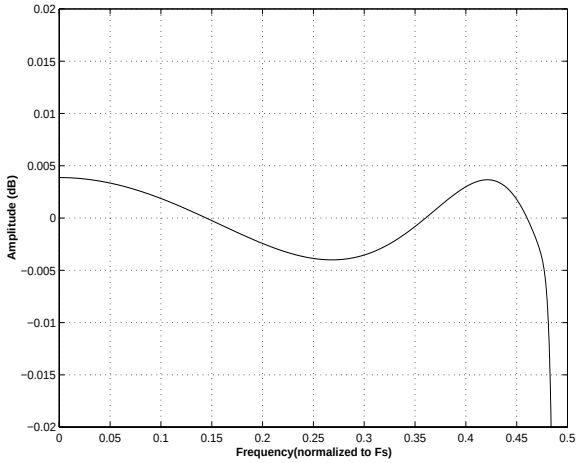


Figure 16. Single-Speed (fast) Passband Ripple

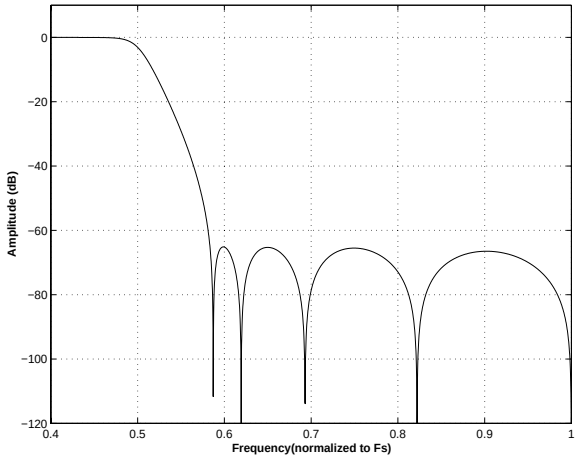


Figure 17. Single-Speed (slow) Stopband Rejection

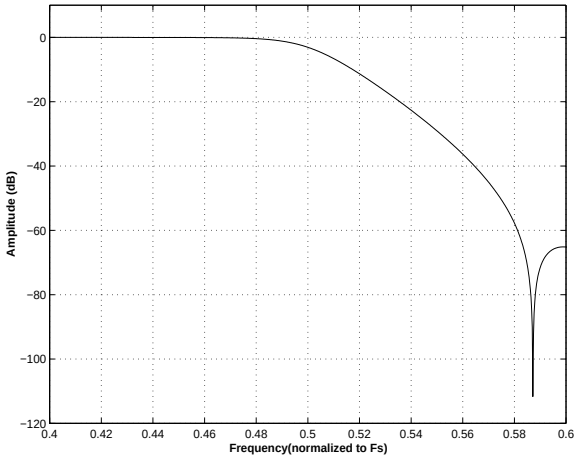


Figure 18. Single-Speed (slow) Transition Band

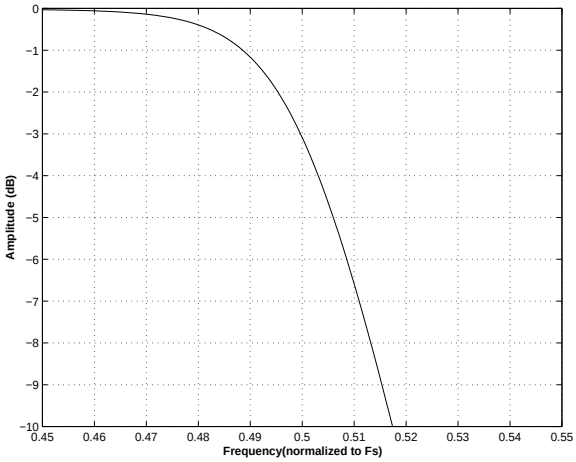


Figure 19. Single-Speed (slow) Transition Band (detail)

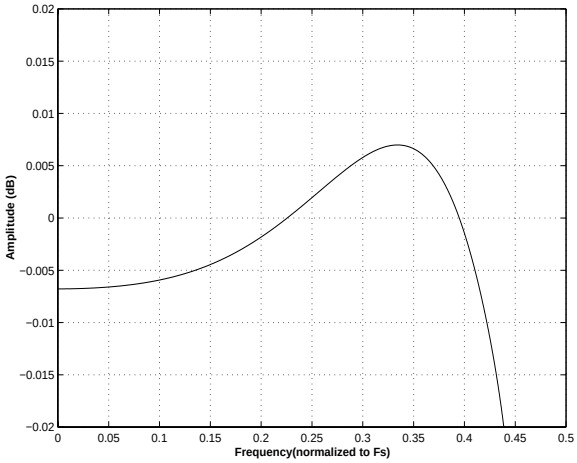


Figure 20. Single-Speed (slow) Passband Ripple

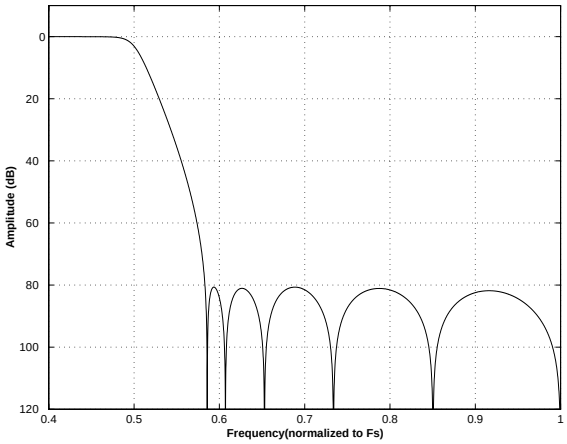


Figure 21. Double-Speed (fast) Stopband Rejection

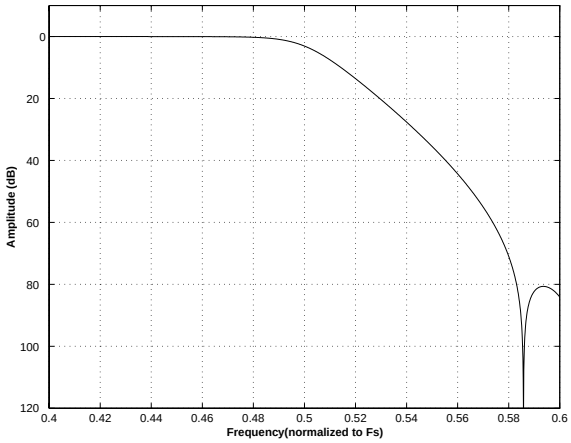


Figure 22. Double-Speed (fast) Transition Band

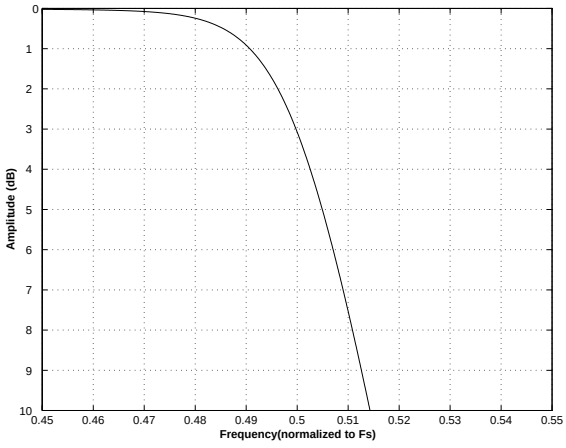


Figure 23. Double-Speed (fast) Transition Band (detail)

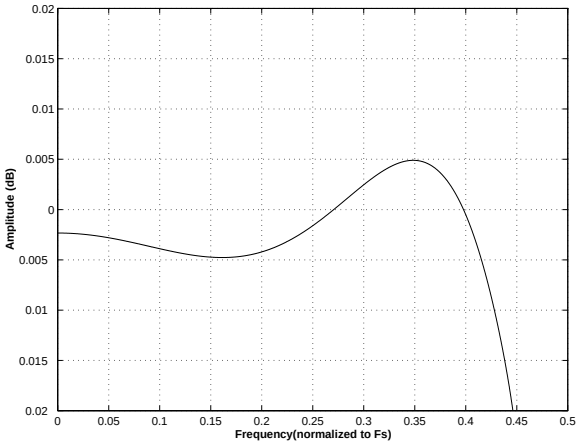


Figure 24. Double-Speed (fast) Passband Ripple

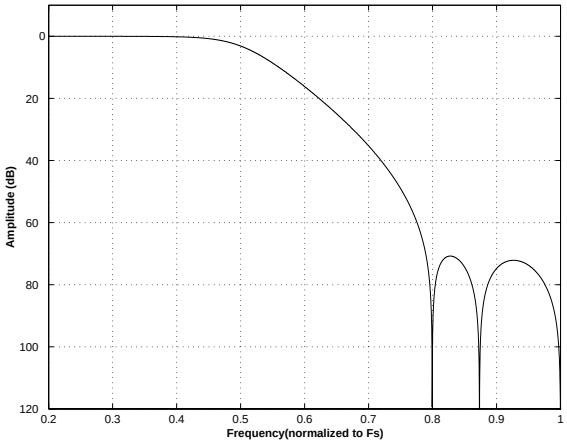


Figure 25. Double-Speed (slow) Stopband Rejection

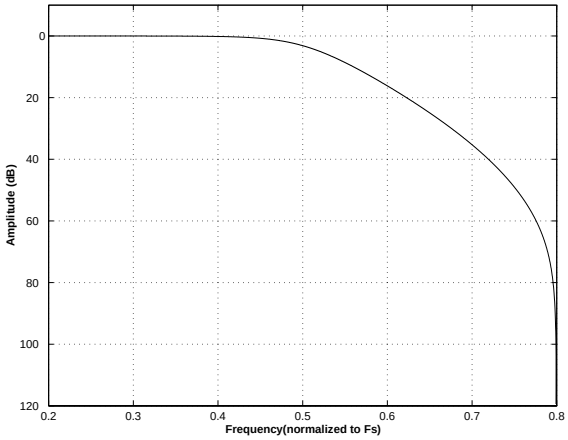


Figure 26. Double-Speed (slow) Transition Band

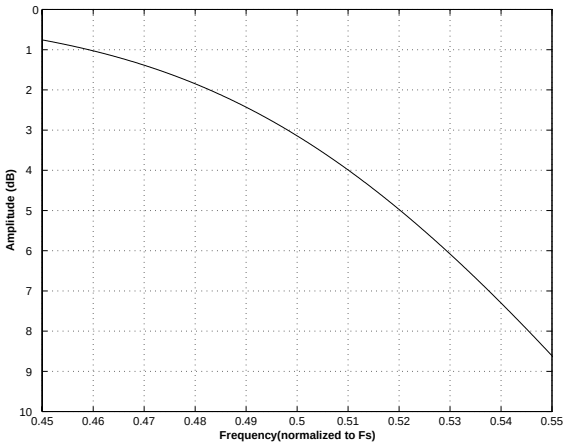


Figure 27. Double-Speed (slow) Transition Band (detail)

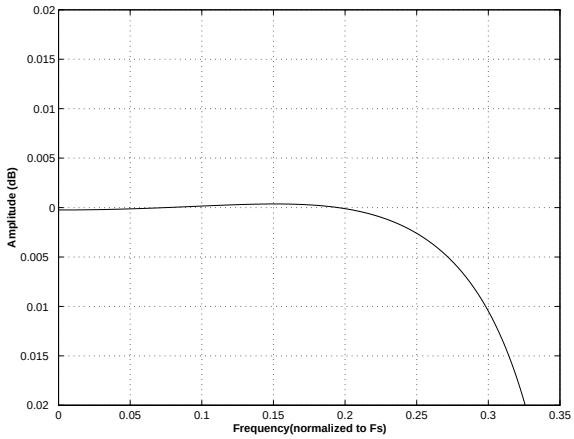


Figure 28. Double-Speed (slow) Passband Ripple

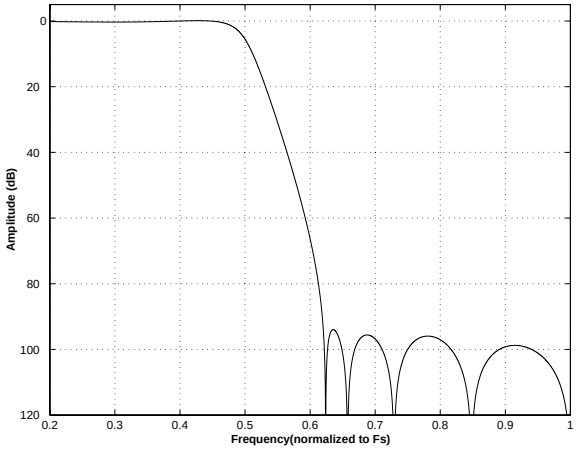


Figure 29. Quad-Speed (fast) Stopband Rejection

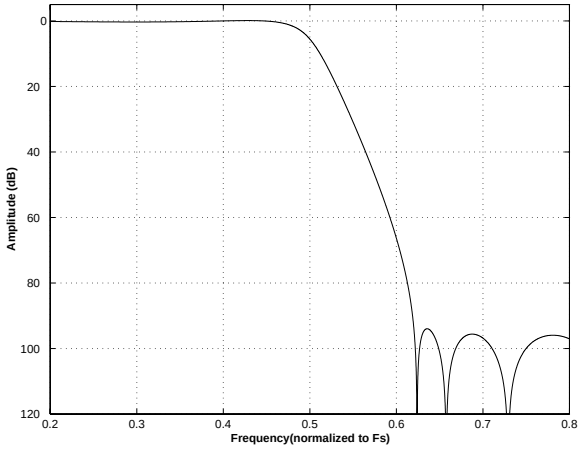


Figure 30. Quad-Speed (fast) Transition Band

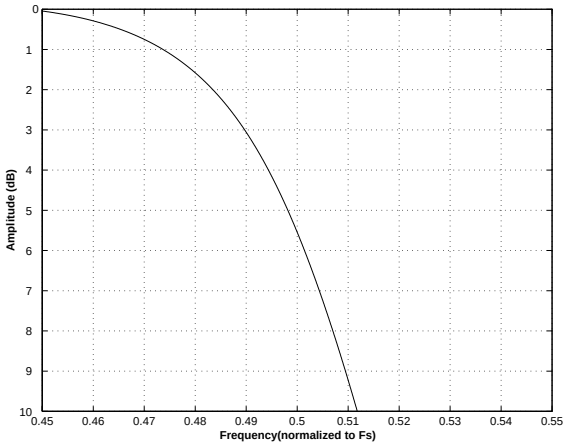


Figure 31. Quad-Speed (fast) Transition Band (detail)

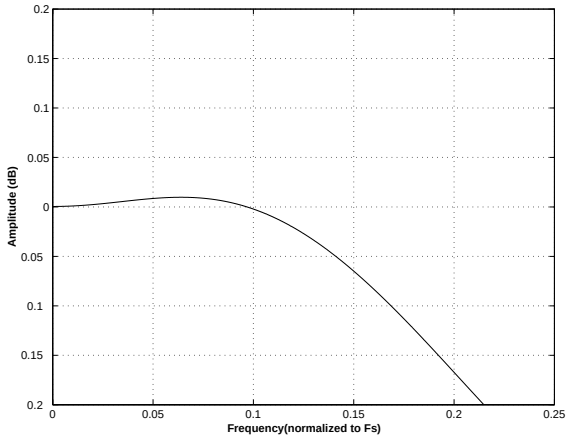


Figure 32. Quad-Speed (fast) Passband Ripple

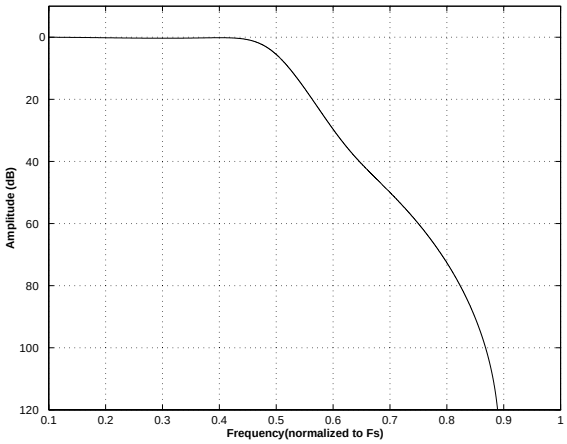


Figure 33. Quad-Speed (slow) Stopband Rejection

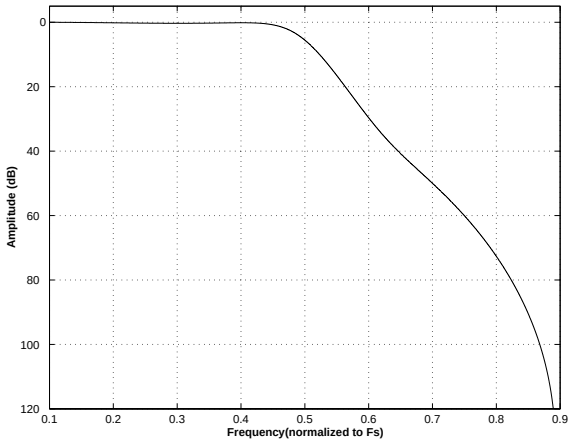


Figure 34. Quad-Speed (slow) Transition Band

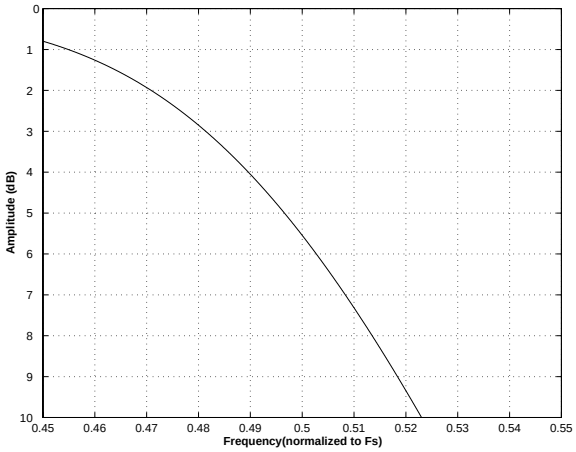


Figure 35. Quad-Speed (slow) Transition Band (detail)

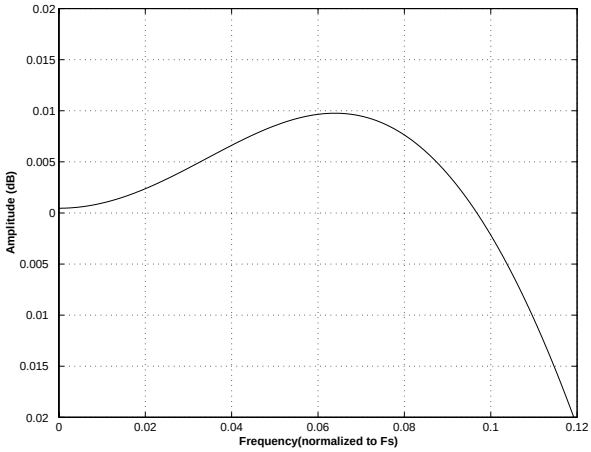


Figure 36. Quad-Speed (slow) Passband Ripple

8. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Intra-Channel Phase Deviation

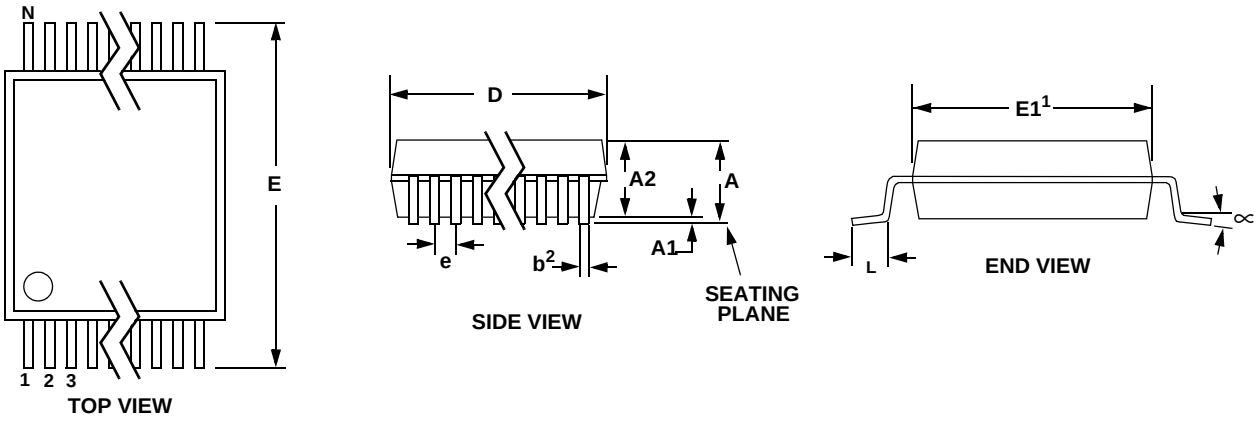
The deviation from linear phase within a given channel.

Inter-Channel Phase Deviation

The difference in phase between channels.

9. PACKAGE DIMENSIONS

20L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.252	0.256	0.259	6.40	6.50	6.60	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	--	0.026	--	--	0.65	
L	0.020	0.024	0.028	0.50	0.60	0.70	
µ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes:

1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance	20L TSSOP	θ_{JA}	-	72	-	°C/Watt

10.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4351	192 kHz Stereo DAC with 2 Vrms Line Out	20-pin TSSOP	YES	Commercial	-10° to +70° C	Rail	CS4351-CZZ
						Tape & Reel	CS4351-CZZR
				Automotive	-40° to +85° C	Rail	CS4351-DZZ
						Tape & Reel	CS4351-DZZR
CDB4351	CS4351 Evaluation Board		-	-	-	-	CDB4351

11.REVISION HISTORY

Release	Date	Changes
PP3	March 2005	Removed CS4351-CZ ordering option. Added CS4351-DZZ ordering option. Updated Tslrd spec on page 10. Updated Tdh spec on page 12. Updated VIL specification on page 13. Updated legal text.
PP4	July 2005	Updated full-scale output specification on page 7. Updated gain drift on page 7 Updated ordering information.
F1	December 2005	Updated status to final Updated legal text

Table 10. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com/corporate/contacts/sales.cfm