



# High Performance Dual Channel Current Mode Controller with ENABLE

## Description

The CS3865C is a high performance, fixed frequency, dual current mode controller. It is used in Off-Line and DC to DC converter applications and require a minimum number of external components. This integrated circuit features a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, and two high current totem pole outputs ideally suited

for driving power MOSFETs. One of the outputs  $V_{OUT2}$  is swappable via the  $ENABLE_2$  pin.

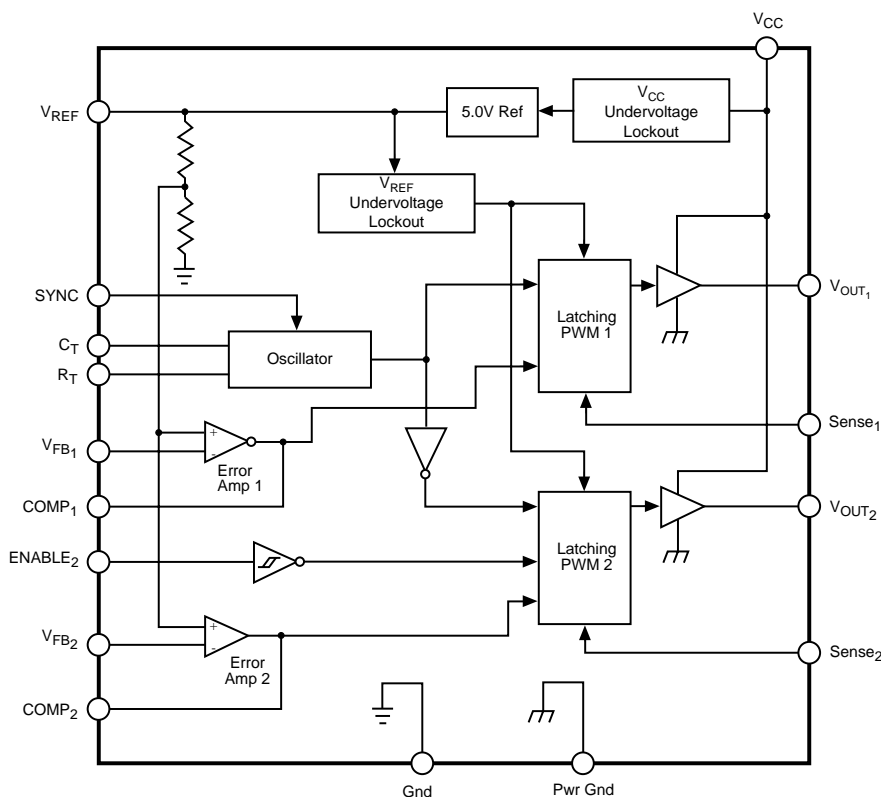
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering of each output.

The CS3865C has a 14V start voltage and is pin compatible with the MC34065H.

## Features

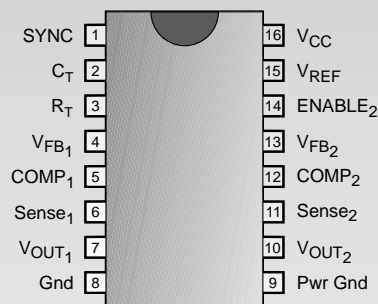
- Oscillator has Precise Duty Cycle Limit and Frequency Control
- 500kHz Current Mode Operation
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Switchable Second Output
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current

## Block Diagram



## Package Options

16L PDIP & SO Wide



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## Absolute Maximum Ratings

Total Power Supply and Zener Current .....	50mA
Output Current, Source or Sink (Note 1).....	1.0A
Output Energy (capacitive load per cycle) .....	5.0 $\mu$ J
Current Sense, Enable and Voltage .....	-0.3 to +5.5V
Feedback Inputs	
High State (Voltage).....	5.5V
Low State (Reverse Current) .....	-5.0mA
Error Amp Output Sink Current.....	10mA
Storage Temperature Range .....	-65 to +150°C
Operating Junction Temperature.....	+150°C
Operating Ambient Temperature.....	0 to +70°C
Lead Temperature Soldering	
Wave Solder (through hole styles only) .....	10 sec. max, 260°C peak
Reflow (SMD styles only) .....	60 sec. max above 183°C, 230°C peak

**Electrical Characteristics:**  $V_{CC} = 15V$ ,  $R_T = 8.2k\Omega$ ,  $C_T = 3.3nF$ , for typical values  $T_A = 25^\circ C$ , for min/max values  $T_A$  is the operating ambient temperature range that applies [Note 3].

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>■ Reference Section</b>					
Reference Output Voltage, $V_{REF}$	$I_{OUT} = 1.0mA$ , $T_J = 25^\circ C$	4.9	5.0	5.1	V
Line Regulation	$11V \leq V_{CC} \leq 15V$		2.0	20.0	mV
Load Regulation	$1.0mA \leq I_{OUT} \leq 10mA$		3.0	25.0	mV
Total Output Variation over Line, Load and Temperature		4.85		5.15	V
Output Short Circuit Current		30	100		mA
<b>■ Oscillator and PWM Sections</b>					
Total Frequency Variation over Line and Temperature	$11V \leq V_{CC} \leq 15V$ , $T_{low} \leq T_A \leq T_{high}$	46.5	49.0	51.5	kHz
Frequency Change with Voltage	$11V \leq V_{CC} \leq 15V$		0.2	1.0	%
Duty Cycle at each Output	Maximum	46.0	49.5	52.0	%
Sync Input Current	High State $V_{IN} = 2.4V$ Low State $V_{IN} = 0.8V$		170 80	250 160	$\mu A$
<b>■ Error Amplifiers</b>					
Voltage Feedback Input	$V_{OUT} = 2.5V$	2.42	2.50	2.58	V
Input Bias Current	$V_{FB} = 5.0V$		-0.1	-1.0	$\mu A$
Open-Loop Voltage Gain	$V_{OUT} = 2.0$ to $4.0V$	65	100		dB
Unity Gain Bandwidth	$T_J = 25^\circ C$ (note 6)	0.7	1.0		MHz
Power Supply Rejection Ratio	$V_{CC} = 11V$ to $15V$	60	90		dB
Output Current	Source $V_{OUT} = 3.0V$ , $V_{FB} = 2.3V$ Sink $V_{OUT} = 1.2V$ , $V_{FB} = 2.7V$	-0.45 2.00	-1.00 12.00		mA mA
Output Voltage Swing	High State, $R_L = 15k$ to ground, $V_{FB} = 2.3V$ Low State, $R_L = 15k$ to $V_{REF}$ , $V_{FB} = 2.7V$	5.0	6.2 0.8	1.1	V

**Electrical Characteristics:**  $V_{CC} = 15V$ ,  $R_T = 8.2k\Omega$ ,  $C_T = 3.3nF$ , for typical values  $T_A = 25^\circ C$ , for min/max values  $T_A$  is the operating ambient temperature range that applies [Note 3].

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>■ Current Sense Section</b>					
Current Sense Input Voltage Gain	(Notes 4 and 5)	2.75	3.00	3.25	V/V
Maximum Current Sense Input Threshold	(Note 4)	430	480	530	mV
Input Bias Current			-2.0	-10.0	$\mu A$
Propagation Delay	Current Sense Input to Output (Note 6)		150	300	ns
<b>■ Output 2 Enable Pin</b>					
Enable Pin Voltage High State	Output 2 enabled	3.5		$V_{REF}$	V
Low State	Output 2 disabled	0.0		1.5	V
Low State Input Current	$V_{IL} = 0V$	100	250	400	$\mu A$
<b>■ Drive Outputs</b>					
Output Voltage Low State	$I_{SINK} = 20mA$		0.1	0.4	V
	$I_{SINK} = 200mA$		1.6	2.5	V
Output Voltage High State	$I_{SOURCE} = 20mA$	13.0	13.5		V
	$I_{SOURCE} = 200mA$	12.0	13.4		V
Output Voltage with UVLO Activated	$V_{CC} = 6.0V$ , $I_{SINK} = 1.0mA$		0.1	1.1	V
Output Voltage Rise Time	$C_L = 1.0nF$ (Note 6)		28	150	ns
Output Voltage Fall Time	$C_L = 1.0nF$ (Note 6)		25	150	ns
<b>■ Undervoltage Lockout Section</b>					
Start-Up Threshold	CS3865C	13	14	15	V
Minimum Operating Voltage After Turn-On		9.0	10.0	11.0	V
Hysteresis			4		V
<b>■ Total Device</b>					
Start-Up Current	$V_{CC} = 12V$		0.6	1.0	mA
Operating Current	(Note 7)		20	25	mA
Power Supply Zener Voltage	$I_{CC} = 30mA$	15.5	17.0	19.0	V

Note 1: Maximum package power dissipation limits must be observed.

Note 3: Adjust  $V_{CC}$  above the Start-Up threshold before setting to 15V.

Note 4: This parameter is measured at latch trip point with  $V_{FB} = 0V$ .

Note 5: Comparator gain is defined as:

$$A_V = \frac{\Delta V_{\text{Compensation}}}{\Delta V_{\text{Current Sense}}}$$

Note 6: These parameters are guaranteed by design but not 100% tested in production.

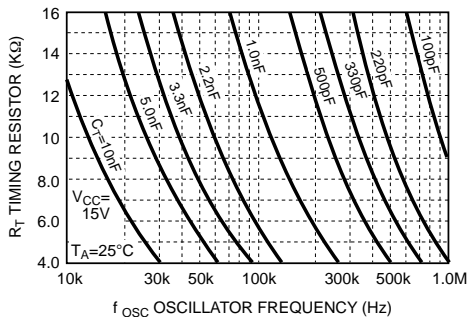
Note 7: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:  $T_{low} = 0^\circ C$ ;  $T_{high} = +70^\circ C$

## Package Pin Description

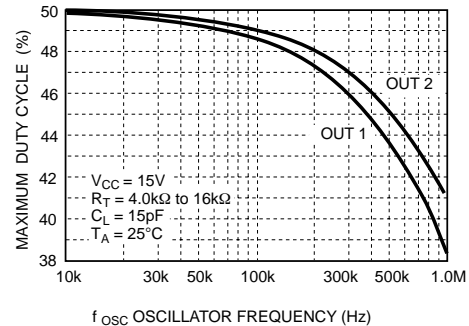
PACKAGE PIN #	PIN SYMBOL	FUNCTION
<b>16 L PDIP &amp; SO Wide</b>		
1	SYNC	A positive going pulse applied to this input will synchronize the oscillator. A DC voltage within the range of 2.4V to 5.5V will inhibit the oscillator.
2	$C_T$	Timing capacitor $C_T$ connects pin to ground setting oscillator frequency.
3	$R_T$	Resistor $R_T$ connects to ground setting the charge current for $C_T$ . Its value must be between 4.0k and 16k.
4	$V_{FB1}$	The inverting input of error amplifier 1. Normally it is connected to the switching power supply output.
5	COMP <sub>1</sub>	The output of error amplifier 1, for loop compensation.
6	Sense <sub>1</sub>	Output 1 pulse by pulse current limit.
7	$V_{OUT1}$	Drives the power switch at output 1.
8	Gnd	Logic ground
9	Pwr Gnd	Power ground. Power device return is connected to this pin.
10	$V_{OUT2}$	Drives the power switch at output 2.
11	Sense <sub>2</sub>	Output 2 pulse by pulse current limit.
12	COMP <sub>2</sub>	Output of error amplifier 2, for loop compensation.
13	$V_{FB2}$	Inverting input of error amplifier 2. Normally it is connected to the switching power supply output.
14	ENABLE <sub>2</sub>	Output 2 disable. A logic low at this pin disables $V_{OUT2}$ .
15	$V_{REF}$	5.0V reference output. It can source current in excess of 30mA.
16	$V_{CC}$	The positive supply of the IC.

## Typical Performance Characteristics

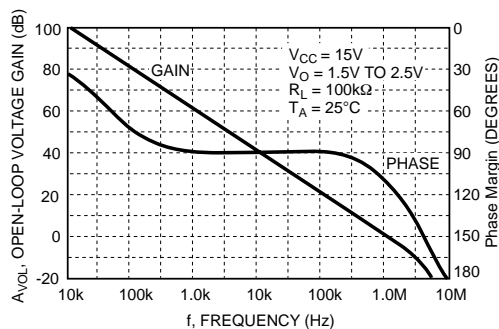
Timing Resistor vs. Oscillator Frequency



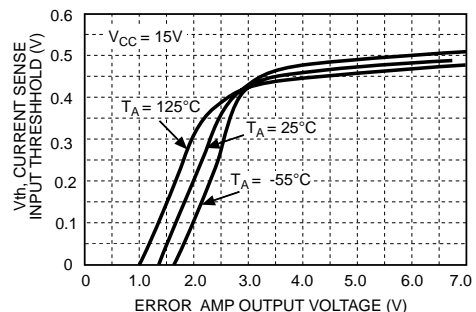
Max. Output Duty Cycle vs. Oscillator Frequency



Error Amp Open-Loop Gain &amp; Phase vs. Frequency

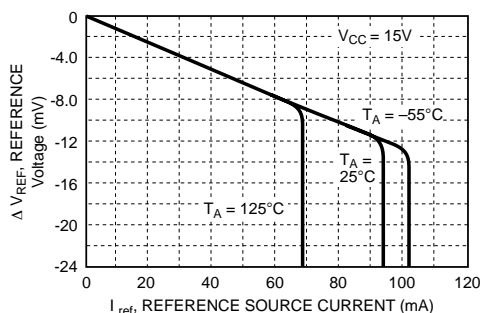


Current Sense Input Threshold vs. Error Amp Output Voltage

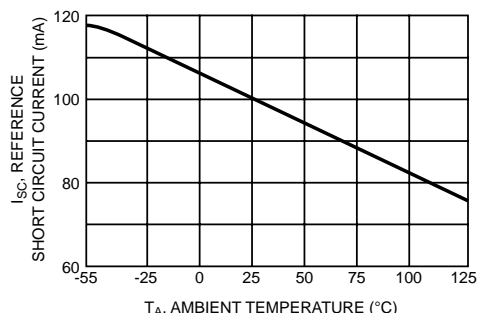


## Typical Performance Characteristics: continued

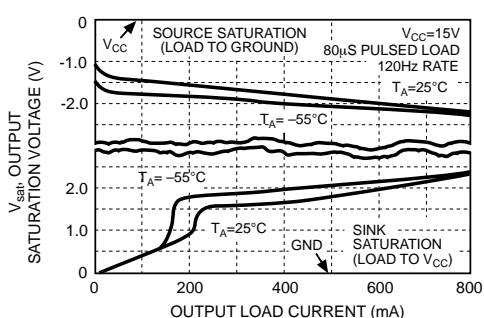
### Reference Voltage Change vs. Source Current



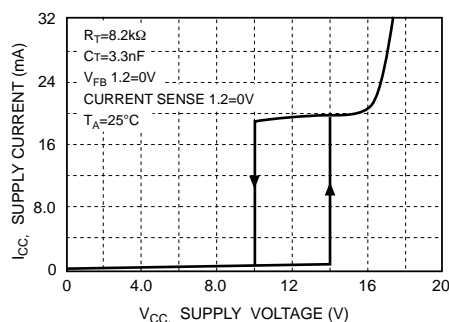
### Reference Short Circuit Current vs. Temperature



### Output Saturation Voltage vs. Load Current



### Supply Current vs. Supply Voltage CS3865C



## Operating Description

The CS3865C is a high performance, fixed frequency, dual channel current mode PWM controller specifically designed for off-line and DC to DC converter applications. It offers the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference, and undervoltage lockout circuits are common to both channels.

### Oscillator

The oscillator uses precise frequency and duty cycle control. The frequency is programmed by the values  $R_T$  and  $C_T$ . Capacitor,  $C_T$ , is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at  $C_T$ . The oscillator peak and valley thresholds are 3.5V and 1.6V respectively. The source/sink current magnitude is controlled by resistor  $R_T$ . For proper operation over temperature range, its value should be between 4.0k $\Omega$  and 16k $\Omega$ .

As  $C_T$  charges and discharges, an internal blanking pulse is generated that alternately drives the inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non-overlapping output duty cycles. The second output,  $V_{OUT2}$  is enabled while  $C_T$  is

charging, and the primary is enabled during the discharge. Even at 500kHz, each output is capable of approximately 44% duty cycle, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications, it may be necessary to synchronize the converter with an external system clock. This can be accomplished by applying an external clock signal. For reliable synchronization, the oscillator frequency should be set about 10% slower than the clock frequency. The rising edge of the clock signal applied to SYNC, terminates  $C_T$ 's charging and  $V_{OUT2}$ 's conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved.

### Error Amplifier

Each channel contains a fully-compensated error amplifier. The output and inverting input nodes are accessible. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71 degrees of phase margin. The non-inverting input is internally biased at 2.5V. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is -1.0 $\mu$ A which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider resistance.

The error amp is compensated externally thru the  $V_{FB}$  and COMP pins. Its output voltage is offset by two diode drops ( $\approx 1.4V$ ) and divided by three before it connects to the inverting input of the current sense comparator. This guarantees that both outputs are disabled when the error amplifier output is at its lowest state which occurs when the power supply is operating at light or no-load conditions, or at the beginning of a soft-start interval.

The minimum allowable error amplifier feedback resistance is limited by the amplifier's source current capability (0.5 mA) and the output voltage ( $V_{OH}$ ) required to reach the current sense comparator 0.5V clamp level with the error amplifier inverting input at ground. This condition happens during initial system start up or when the sensed output is shorted:

$$R_{F(\min)} \approx \frac{3 \times 0.5V + 1.4V}{0.5mA} = 5800\Omega$$

### Current Sense Comparator and PWM Latch

The CS3865C operates as a current mode controller. Output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the error amplifier output. Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The current sense comparator-PWM Latch combination ensures that only a single pulse appears at the drive output ( $V_{OUT}$ ) during any given oscillator cycle. The current is converted to a voltage by connecting a sense resistor  $R_{Sense}$  in series with the source of output switch Q1 and ground. This voltage is monitored through the Sense<sub>1,2</sub> pins and compared to a voltage derived from the error amp output. The peak current under normal operating conditions is controlled by the voltage at COMP where:

$$I_{pk} = \frac{V(\text{COMP}) - 1.4V}{3R_{Sense}}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage is too high. Under these conditions, the current sense comparator threshold will be internally clamped to 0.5V. Therefore the maximum peak switch current is:

$$I_{pk(\max)} = \frac{0.5V}{R_{Sense}}$$

Erratic operation due to noise pickup can result if there is an excessive reduction of the  $I_{pk}(\max)$  clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. The addition of an  $R_C$  filter on the current sense input reduces this spike to an acceptable level.

### Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. Power supply terminal ( $V_{CC}$ ) and the reference output ( $V_{REF}$ ) are monitored by separate comparator. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The upper and lower thresholds of the  $V_{CC}$  comparator are 14V and 10V respectively.

The  $V_{REF}$  comparator disables the drive outputs until the internal circuitry is functional. This comparator has upper and lower thresholds of 3.6V and 3.4V. A 17V zener is connected as a shunt regulator from  $V_{CC}$  to ground to protect the IC and power MOSFET gate from excessive voltage. The guaranteed minimum operating voltage after turn-on is 11V.

### Outputs and Power Ground

Each channel contains a single totem-pole output stage that is specifically designed for direct drive of power MOSFET's. The outputs have up to  $\pm 1.0A$  peak current capability and have a typical rise and fall time of 28 ns with a 1.0nF load. Internal circuitry has been added to keep the outputs in active pull-down mode whenever an undervoltage lockout is active, eliminating the need for an external pull-down resistor.

Although the outputs are optimized for MOSFET's, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn-off. Since the outputs do not contain internal current limits an external series resistor will be required to prevent the peak output current from exceeding the  $\pm 1.0A$  maximum rating. The sink saturation ( $V_{OL}$ ) is less than 0.4V at 100mA.

A separate ground pin, Pwr Gnd, is provided. Properly implemented, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes important when the  $I_{pk(\max)}$  clamp level is reduced.

### ENABLE<sub>2</sub>

This input is used to switch  $V_{OUT2}$ .  $V_{OUT1}$  is used to control circuitry that runs continuously, e.g. volatile memory, the system clock, or a remote controlled receiver.  $V_{OUT2}$  output can control the high power circuitry that is turned off when not needed.

### Voltage Reference

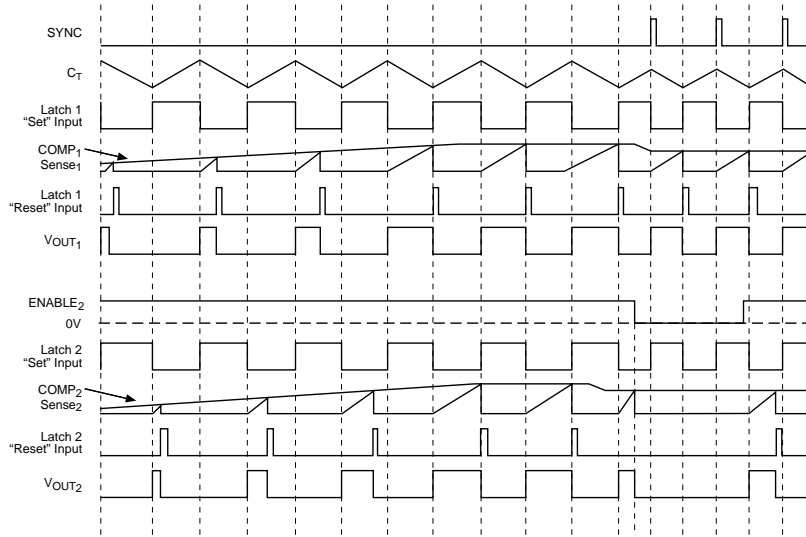
The 5.0V bandgap reference is trimmed to  $\pm 2.0\%$  tolerance. The reference has short circuit protection and is capable of sourcing 30mA for powering any additional external circuitry.

Design Considerations

High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the current sense and voltage feed-back inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit board layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input fil-

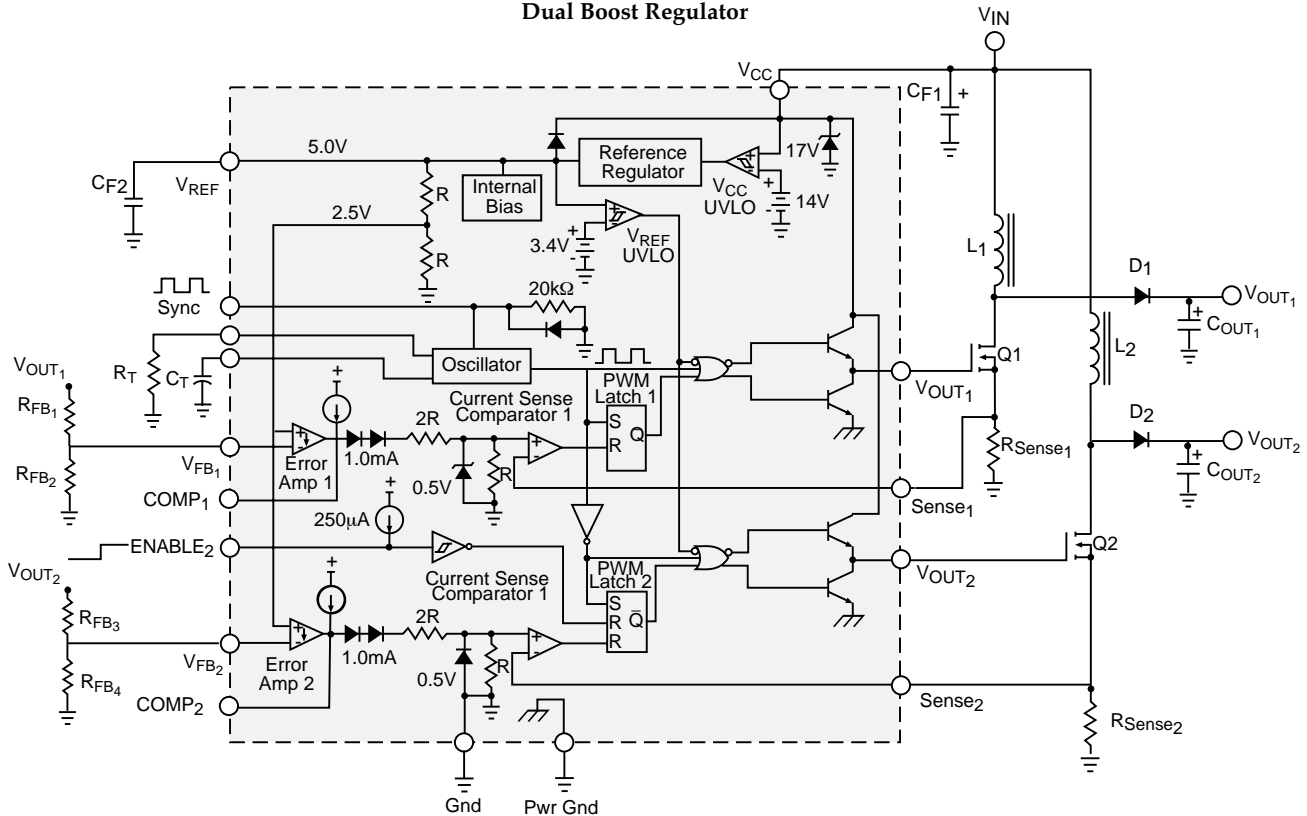
ter capacitor. Ceramic bypass capacitors (0.1 $\mu$ F) connected directly to  $V_{CC}$  and  $V_{REF}$  may be required to improve noise filtering. They provide a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs. The error amp compensation circuitry and the converter output voltage-divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Timing Diagram



Applications Diagram

Dual Boost Regulator



Package Specification

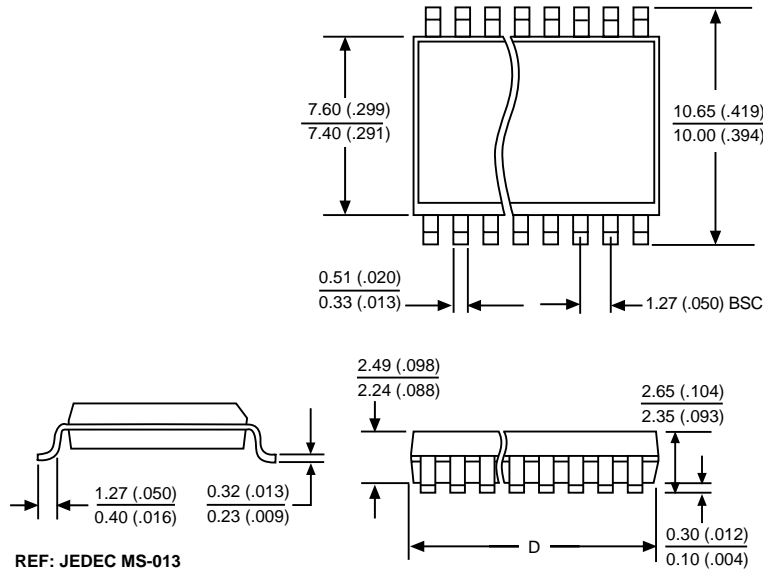
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L PDIP	19.69	18.67	.775	.735
16L SO	10.50	10.10	.413	.398

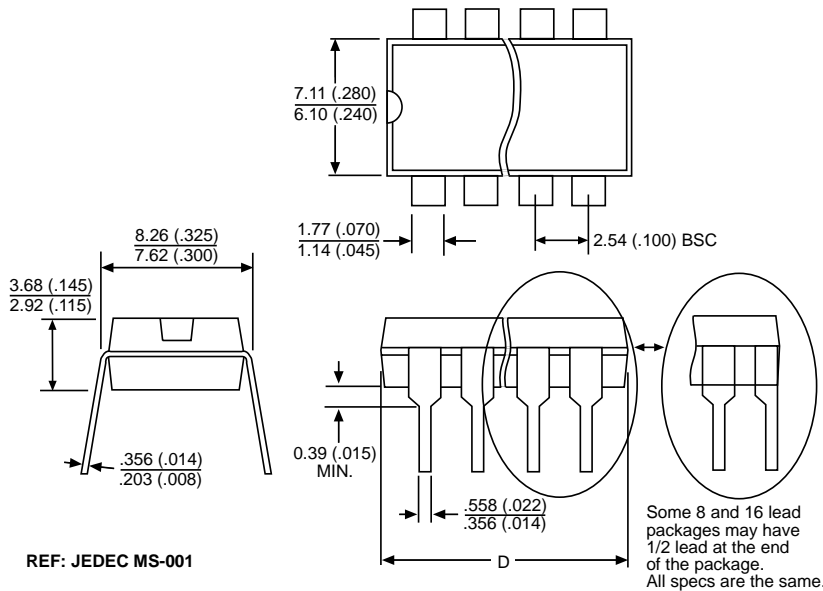
PACKAGE THERMAL DATA

Thermal Data		16 Lead PDIP	16 Lead SO	
$R\theta_{JC}$	typ	42	23	$^{\circ}\text{C}/\text{W}$
$R\theta_{JA}$	typ	80	105	$^{\circ}\text{C}/\text{W}$

Surface Mount Wide Body (DW); 300 mil wide



Plastic DIP (N); 300 mil wide



Ordering Information

Part Number	Description
CS3865CGN16	16L PDIP
CS3865CGDW16	16L SO Wide
CS3865CGDWR16	16L SO Wide (tape & reel)

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