CS1601
CS1601H

Digital PFC Controller for Electronic Ballasts

Features

- ☐ Low PFC System Cost
- ☐ Best-in-class THD
- ☐ Digital EMI Noise Shaping Reduces Conducted EMI
- ☐ Adaptive Switching Frequency Control Minimizes Boost Inductor Size
- ☐ High Efficiency Due to Zero-current Switching
- ☐ Integrated Feedback Compensation Simplifies System Design
- ☐ Comprehensive Safety Features
    - Undervoltage Lockout (UVLO)
    - Output Overvoltage Protection
    - Cycle-by-cycle Current Limiting
    - Input Voltage Brownout Protection
    - Open/Short Loop Protection for IAC & IFB Pins
    - Thermal Shutdown
- ☐ Pin Placement Similar to Traditional Boundary Mode (CRM) Controllers

Applications

- ☐ LED Power Supply/Driver
- ☐ Fluorescent Ballasts
- ☐ HID Ballasts

Overview

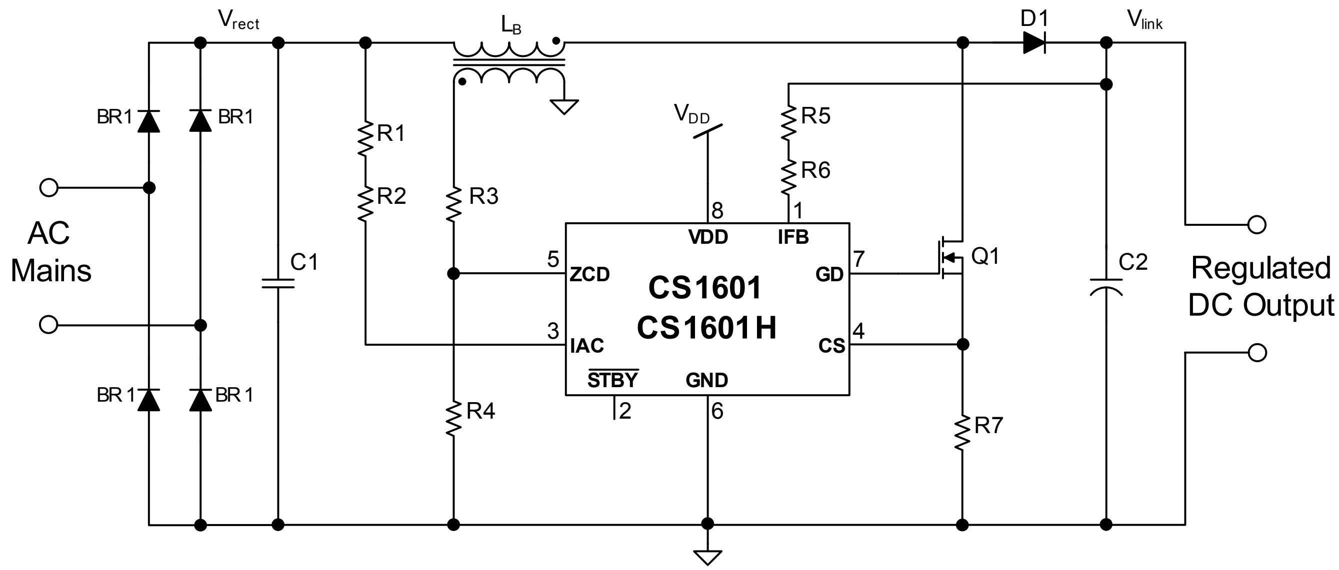
The CS1601 and CS1601H are digital power factor correction (PFC) controllers designed to deliver the lowest PFC system cost in electronic ballast applications. The controller operates in a variable frequency discontinuous conduction mode (VF-DCM) with zero-current switching optimized to deliver best-in-class THD and minimize the size and cost of magnetic components. The CS1601 operates at switching frequencies of up to 70kHz, and the CS1601H operates at frequencies of up to 100kHz.

The VF-DCM control algorithm varies both duty cycle and frequency. This spreads the EMI frequency spectrum, thus reducing conducted EMI filtering requirements. In addition, the maximum switching frequency is reached at the peak of the AC input, which allows the use of a smaller, more cost-effective boost inductor.

The feedback loop is closed through an integrated compensation network within the controller, eliminating the need for additional external components. Protection features such as overvoltage, overcurrent, open and short-circuit protection, overtemperature, and brownout protect the system during abnormal transient conditions.

Ordering Information

See **page 16.**



1. INTRODUCTION

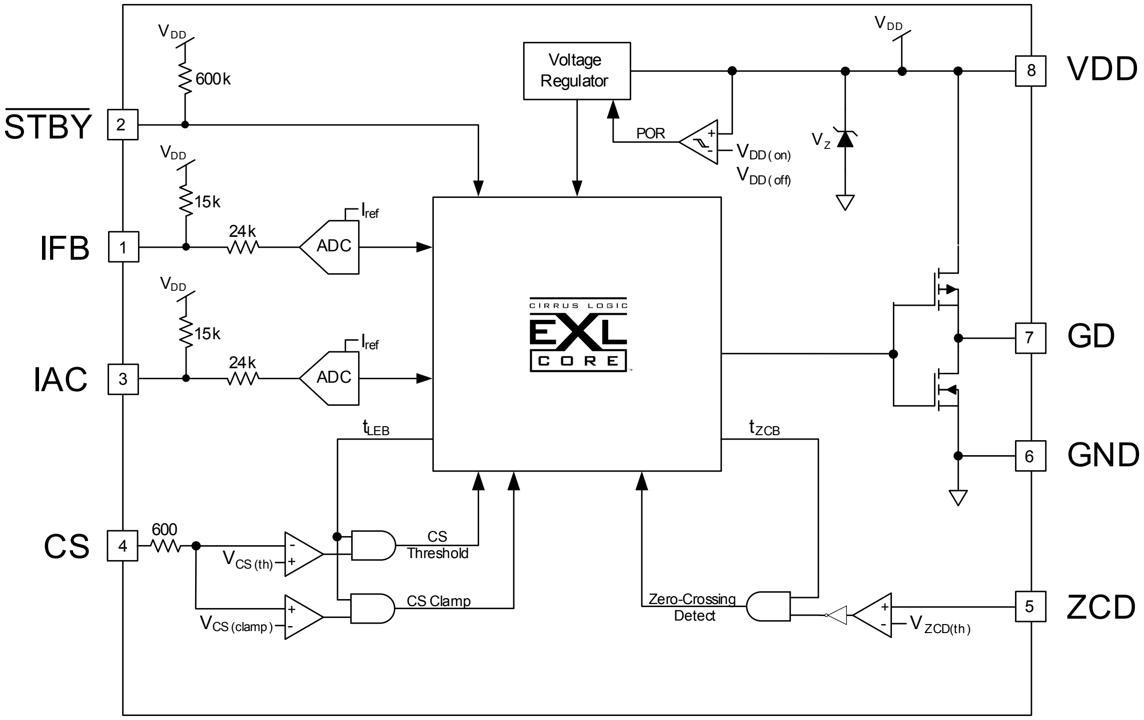


Figure 1. CS1601 Block Diagram

The CS1601 digital power factor correction (PFC) control IC is designed to deliver the lowest system cost by reducing the total number of system components and optimizing the EMI noise signature, which reduces the conducted EMI filter requirements. The CS1601 digital algorithm determines the behavior of the boost converter during startup, normal operation, and under fault conditions (overvoltage, overcurrent, and overtemperature).

Figure 1 illustrates a high-level block diagram of the CS1601. The PFC processor logic regulates the power transfer by using an adaptive digital algorithm to optimize the PFC active-switch (MOSFET) drive signal duty cycle and switching frequency. The adaptive controller uses independent analog-to-digital converter (ADC) channels when sensing the feedback and feedforward analog signals required to implement the digital PFC control algorithm.

The AC mains rectified voltage (on pin IAC) and PFC output link voltage (on pin IFB) are transformed by the PFC processor logic and used to generate the optimum PFC active-switch drive signal (GD) by calculating the optimal switching frequency and t_{ON} time on a cycle-by-cycle basis.

An auxiliary winding is typically added to the PFC boost inductor to provide zero-current detection (ZCD) information. The ZCD acts as a demagnetization sensor used to monitor the PFC active-switching behavior and efficiency. The auxiliary voltage is normalized using an external attenuator and is connected to the ZCD pin, providing the CS1601 a mechanism to detect the valley/zero crossings. The ZCD comparator looks for the zero crossing on the auxiliary winding and switches when the auxiliary voltage is below zero. Switching in the valley of the oscillation minimizes the switching losses and reduces EMI noise.

The PFC controller uses a current sensor for overcurrent protection. The boost inductor peak current is measured across an external resistor in the switching circuit on a cycle-by-cycle basis. An overcurrent fault is generated when the sense voltage applied to the CS pin exceeds a predefined reference voltage.

The CS1601 includes a supervisor and protection circuit to manage startup, shutdown, and fault conditions. The protection circuit is designed to prevent output overvoltage as a result of load and AC mains transients. The PFC power converter main rectified voltage (V_{rect}) and output link voltage (V_{link}) are monitored for overvoltage faults that would lead to shutdown of the PFC controller. The PFC overvoltage protection is designed for auto-recovery; operation resumes once the fault clears.

2. PIN DESCRIPTION

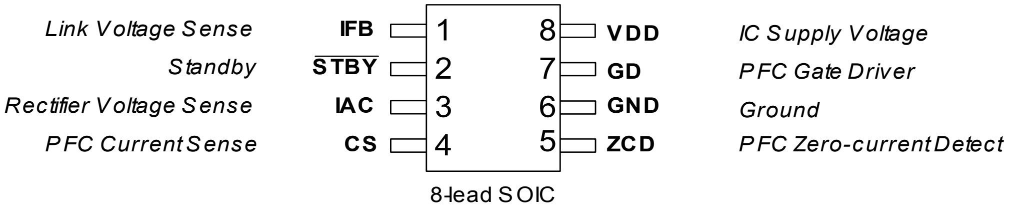


Figure 2. CS1601 Pin Assignments

Pin Name	Pin #	I/O	Description
IFB	1	IN	**Link Voltage Sense** — A current proportional to the output link voltage of the PFC is input here. The current is measured with an ADC.
$\overline{\text{STBY}}$	2	IN	**Standby** — A voltage below 0.8V puts the IC into a non-operating, low-power state. The input has an internal 600kΩ pull-up resistor to the V_{DD} pin.
IAC	3	IN	**Rectifier Voltage Sense** — A current proportional to the rectified line voltage is input here. The current is measured with an ADC.
CS	4	IN	**PFC Current Sense** — The current flowing in the PFC MOSFET is sensed through a resistor. The resulting voltage is applied to this pin and digitized for use by the PFC computational logic to limit the maximum current through the power FET.
ZCD	5	IN	**PFC Zero-current Detect** — Boost Inductor demagnetization sensing input for zero-current detection (ZCD) information. The pin is externally connected to the PFC boost inductor auxiliary winding through an external resistor divider.
GND	6	PWR	**Ground** — Common reference. Current return for both the input signal portion of the IC and the gate driver.
GD	7	OUT	**PFC Gate Driver** — The totem pole stage is able to drive the power MOSFET with a peak current of 0.5A source and 1.0A sink.
V_{DD}	8	PWR	**IC Supply Voltage** — Supply voltage of both the input signal portion of the IC and the gate driver. A storage capacitor is connected on this pin to serve as a reservoir for operating current for the device, including the gate drive current to the power transistor. This pin is clamped to a maximum voltage (V_Z) by an internal zener function.

3. CHARACTERISTICS AND SPECIFICATIONS

3.1 Electrical Characteristics

Typical characteristics conditions:

$T_A = 25°C$, $V_{DD} = 13V$, GND = 0V

All voltages are measured with respect to GND.

Unless otherwise specified, all currents are positive when flowing into the IC.

Minimum/Maximum characteristics conditions:

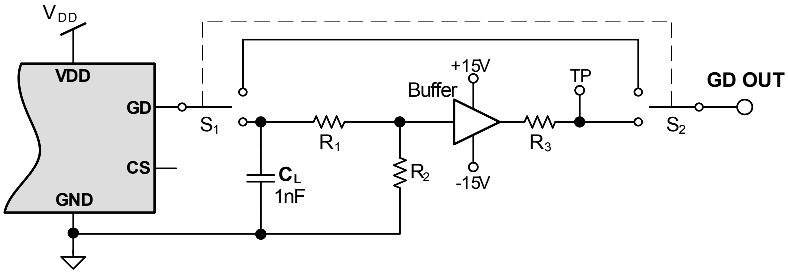
$T_J = -40°$ to $+125°C$, $V_{DD} = 10V$ to $15V$, GND = 0V

Parameter	Condition	Symbol	Min	Typ	Max	Unit
V_{DD} Supply Voltage						
Operating Range	After Turn-on	V_{DD}	7.9	-	17.0	V
Turn-on Threshold Voltage	V_{DD} Increasing	$V_{DD(on)}$	9.8	10.2	10.5	V
Turn-off Threshold Voltage (UVLO)	V_{DD} Decreasing	$V_{DD(off)}$	7.9	8.1	8.3	V
UVLO Hysteresis		V_{Hys}	-	2.1	-	V
Zener Voltage	$I_{DD} = 20mA$	V_Z	17.0	17.9	19.0	V
V_{DD} Supply Current						
Startup Supply Current	$V_{DD} = V_{DD(on)}$	I_{ST}	-	68	95	µA
Operating Supply Current[4] CS1601 CS1601H	 $C_L = 1nF$, fsw = 70kHz $C_L = 1nF$, fsw = 100kHz	I_{DD}	 - -	 1.5 1.75	 2.1 2.25	 mA mA
Standby Supply Current	$\overline{STBY} < 0.8V$	I_{SB}	-	80	125	µA
Reference						
Reference Current		I_{ref}	-	129	-	µA
PFC Gate Drive						
Output Source Resistance	$I_{GD} = 100mA$, $V_{DD} = 13V$	R_{OH}	-	9	-	Ω
Output Sink Resistance	$I_{GD} = -200mA$, $V_{DD} = 13V$	R_{OL}	-	6	-	Ω
Rise Time[4]	$C_L = 1nF$, $V_{DD} = 13V$	t_r	-	32	50	ns
Fall Time[4]	$C_L = 1nF$, $V_{DD} = 13V$	t_f	-	15	27	ns
Output Voltage Low State	$I_{GD} = -200mA$, $V_{DD} = 13V$	Vol	-	0.9	1.3	V
Output Voltage High State	$I_{GD} = 100mA$, $V_{DD} = 13V$	Voh	11.3	11.8	-	V
Zero-current Detection (ZCD)						
ZCD Threshold		$V_{ZCD(th)}$	-	50	-	mV
ZCD Blanking		t_{ZCB}	-	200	-	ns
ZCD Sink Current[1]		I_{ZCD}	-2	-	-	mA
Upper Voltage Clamp	$I_{ZCD} = 1mA$	V_{CLP}	-	V_{DD}	-	V
Overvoltage Protection (OVP)						
IFB Current at Startup Mode		$I_{IFB(startup)}$	-	116	-	µA
IFB Current at Normal Mode		$I_{IFB(norm)}$	-	129	-	µA
OVP Threshold	$I_{ref} = 129µA$	I_{OVP}	-	139	-	µA
OVP Hysteresis	$I_{ref} = 129µA$	$I_{OVP(Hy)}$	-	2	-	µA

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Overcurrent Protection (OCP)						
Current Sense Reference Clamp		$V_{CS(clamp)}$	-	1.0	-	V
Threshold on Current Sense		$V_{CS(th)}$	-	0.5	-	V
Leading Edge Blanking		t_{LEB}	-	300	-	ns
Delay to Output		t_{CS}	-	60	350	ns
Brownout Protection (BP)						
Input Brownout Protection Threshold	Gate Drive Turns Off	$I_{BP(lower)}$	-	31.6	-	µA
Input Brownout Recovery Threshold	Gate Drive Turns On	$I_{BP(upper)}$	-	39.6	-	µA
Thermal Protection[2]						
Thermal Shutdown Threshold		T_{SD}	134	147	159	°C
Thermal Shutdown Hysteresis		$T_{SD(Hy)}$	-	9	-	°C
$\overline{\text{STBY}}$ Input[3]						
Logic Threshold Low			-	-	0.8	V
Logic Threshold High			V_{DD}-0.8	-	-	V

Notes:

1. External circuitry should be designed to ensure the ZCD sink current pulled from the internal clamp diode when it is forward biased does not exceed specification.
2. Specifications guaranteed by design and are characterized and correlated using statistical process methods.
3. $\overline{\text{STBY}}$ is designed to be driven by an open collector. The input is internally pulled up with a 600 kΩ resistor.
4. For test purposes, load capacitance (C_L) is 1 nF and is connected as shown in the following diagram.



3.2 Absolute Maximum Ratings

Characteristics conditions:

All voltages are measured with respect to GND.

Pin	Symbol	Parameter		Value	Unit
8	V_{DD}	IC Supply Voltage		19	V
1,2,3,4,5	-	Analog Input Maximum Voltage		-0.5 to (V_{DD}+0.5)	V
1,2,3,4,5	-	Analog Input Maximum Current		50	mA
7	V_{GD}	Gate Drive Output Voltage		-0.3 to (V_{DD}+0.3)	V
7	I_{GD}	Gate Drive Output Current		-1.0 / +0.5	A
-	P_D	Total Power Dissipation @ T_A = 50 °C		600	mW
-	θ_{JA}	Junction-to-Ambient Thermal Impedance		107	°C/W
-	T_A	Operating Ambient Temperature Range		-40 to +125	°C
-	T_J	Junction Temperature Operating Range[5]		-40 to +125	°C
-	T_{Stg}	Storage Temperature Range		-65 to +150	°C
All Pins	ESD	Electrostatic Discharge Capability	Human Body Model Charged Device Model	2000 500	V V

Notes: 5. Long-term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation at the rate of 50 mW/ °C for variation over temperature.

WARNING:
Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

4. TYPICAL ELECTRICAL PERFORMANCE

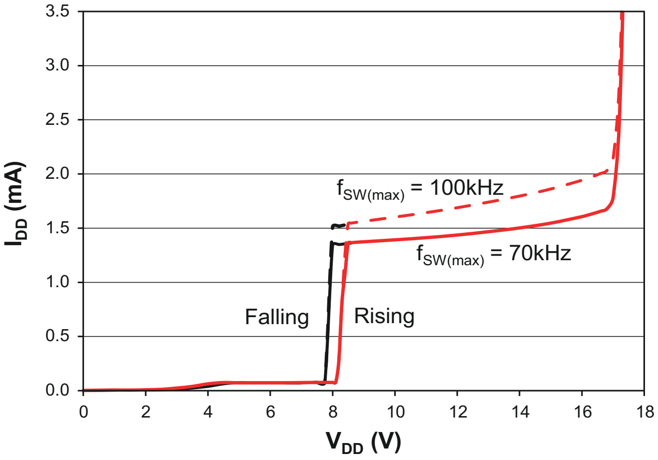


Figure 3. Supply Current vs. Supply Voltage

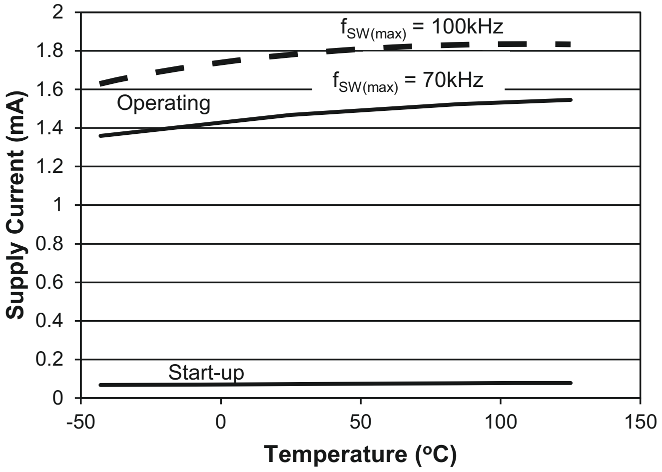


Figure 4. Supply Current (I_{SB}, I_{ST}, I_{DD}) vs. Temp

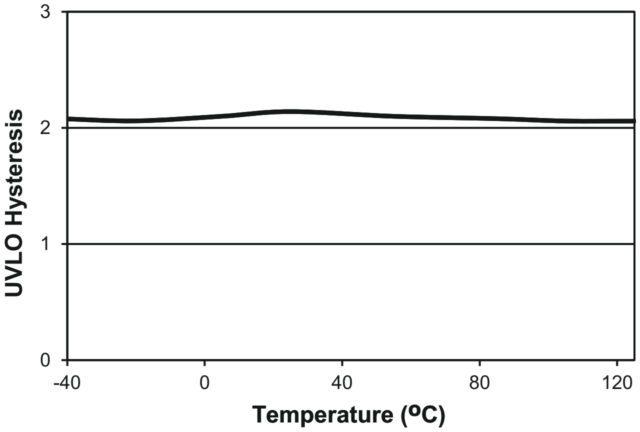


Figure 5. UVLO Hysteresis vs. Temp

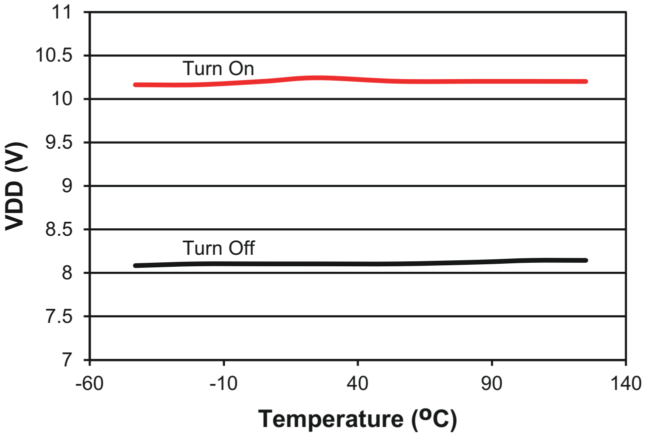


Figure 6. Turn-on & Turn-off Threshold vs. Temp

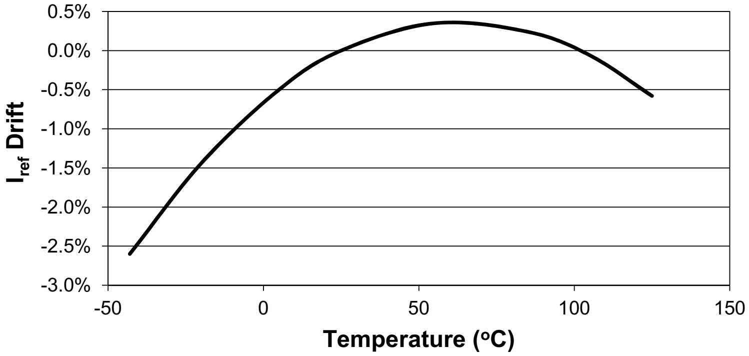


Figure 7. Reference Current (I_{ref}) Drift vs. Temp

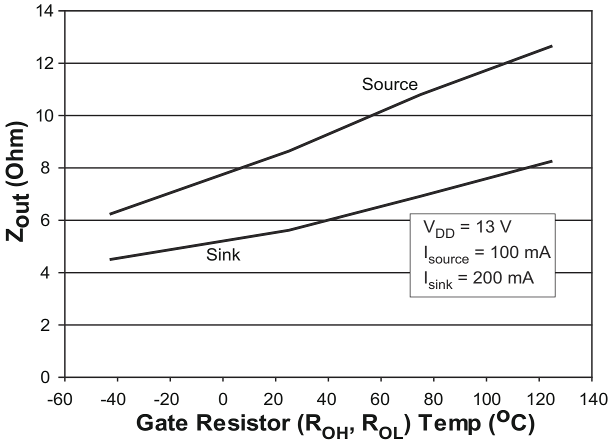


Figure 8. Gate Resistance (R_{OH}, R_{OL}) vs. Temp

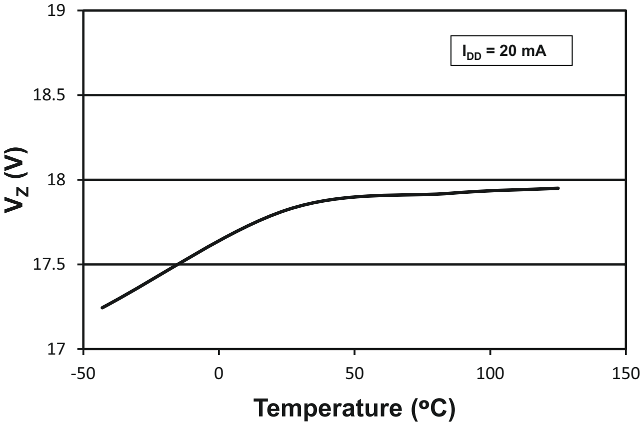


Figure 9. V_{DD} Zener Voltage vs. Temp

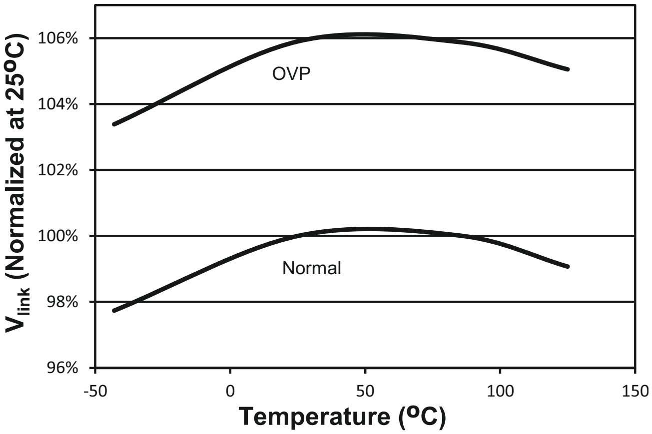


Figure 10. OVP vs. Temp

5. GENERAL DESCRIPTION

The CS1601 offers numerous features, options, and functional capabilities to the electronic product lighting designer. This digital power factor correction (PFC) control IC is designed to replace legacy analog PFC controllers with minimal design effort.

5.1 PFC Operation

One key feature of the CS1601 is its operating frequency profile. Figure 10 illustrates how the frequency varies over a half cycle of the line voltage in steady-state operation. When power is first applied to the CS1601, it examines the line voltage and adapts its operating frequency to the line voltage, as shown in Figure 10. The operating frequency is varied from the peak to the trough of the AC input. During startup, the control algorithm generates maximum power while operating in critical conduction mode (CRM), providing an approximate square-wave current envelope within every half-line cycle.

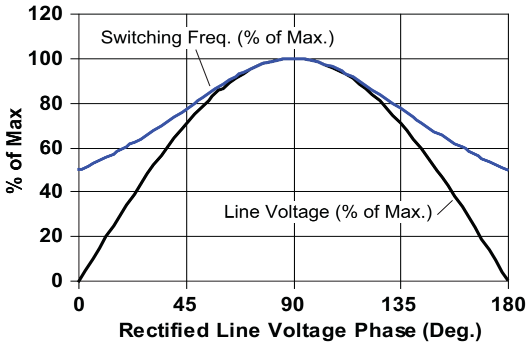


Figure 10. Switching Frequency vs. Phase Angle

Figure 11 illustrates how the operating frequency of the CS1601 (as a percentage of maximum frequency) changes with output power and the peak of the line voltage.

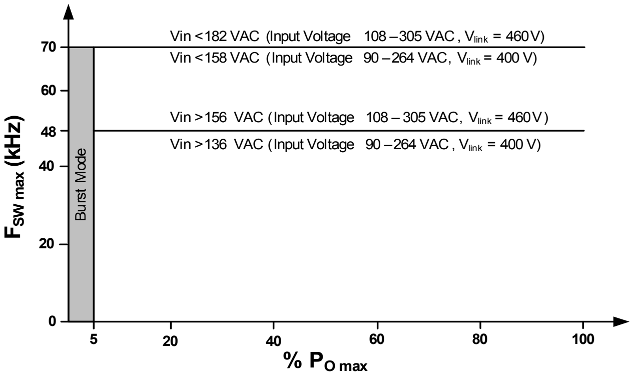


Figure 11. CS1601 Max Switching Freq vs. Output Power

Figure 12 illustrates how the operating frequency of CS1601H changes with output power and the peak of the line voltage.

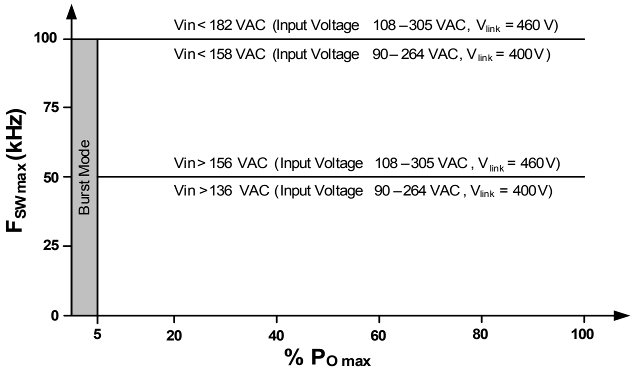


Figure 12. CS1601H Max Switching Freq vs. Output Power

When P_O falls below 5%, the CS1601 changes to Burst Mode. (Refer to 5.3 *Burst Mode* on page 10 for more information.)

The CS1601 is designed to function as a DCM controller. However, during peak periods, the controller may interchange control methods and operate in a quasi-critical-conduction mode (quasi-CRM) at low line. For example, at 108VAC main input under full load, the PFC controller will function as a quasi-CRM controller at the peak of the AC line cycle, as shown in Figure 13.

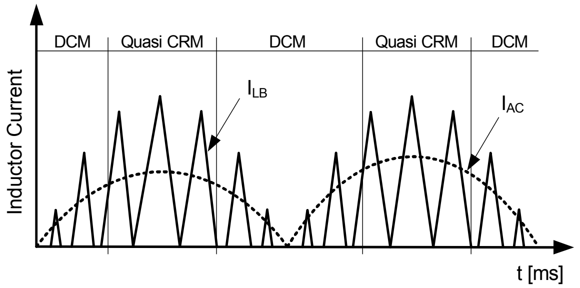


Figure 13. DCM and Quasi-CRM Operation with CS1601

The zero-current detection (ZCD) of the boost inductor is achieved using an auxiliary winding. When the stored energy of the inductor is fully released to the output, the voltage on the ZCD pin decreases, triggering a new switching cycle. This quasi-resonant switching allows the active switch to be turned on with near-zero inductor current, resulting in a nearly lossless switch event. This minimizes turn-on losses and EMI noise created by the switching cycle. PFC control is achieved during light load by using on-time modulation.

5.2 Startup vs. Normal Operation Mode

The CS1601 has two discrete operation modes: startup and normal. Startup mode will be activated when V_{link} is less than 90% of nominal value, $V_{O(startup)}$, and remains active until V_{link} reaches 100% of nominal value, as shown in Figure 14. Startup mode is activated during initial system power-up. Any V_{link} drop to less than $V_{O(startup)}$, such as a load change, can cause the system to enter startup mode until V_{link} is brought back into regulation.

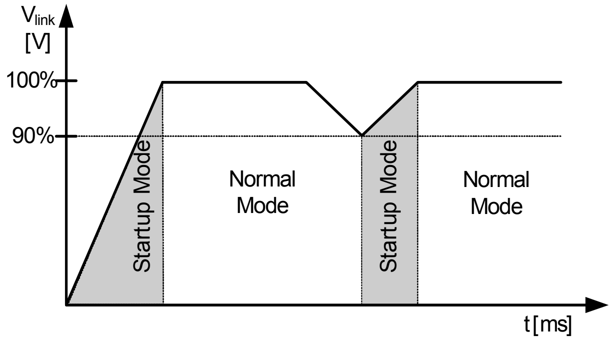


Figure 14. Startup and Normal Modes

Startup mode is defined as a surge of current delivering maximum power to the output regardless of the load. During every active switch cycle, the 'ON' time is calculated to drive a constant peak current over the entire line cycle. However, the 'OFF' time is calculated based on the DCM/CCM boundary equation.

5.3 Burst Mode

Burst mode is used to improve system efficiency when the system output power (P_o) is <5% of nominal. Burst mode is implemented by intermittently disabling the PFC over a full half-line period under light-load conditions, as shown in Figure 15.

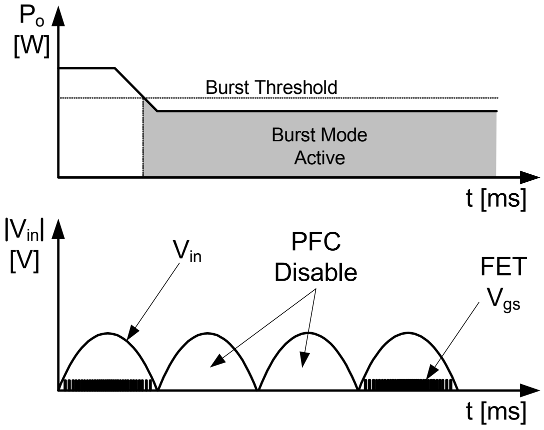


Figure 15. Burst Mode

5.4 Output Power and PFC Boost Inductor

In normal operating mode, the nominal output power is estimated by the following equation:

$$P_o = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times L_B \times V_{link}} \qquad \text{[Eq.1]}$$

where:

P_o	rated output power of the system
η	efficiency of the boost converter (estimated as 100% by the PFC algorithm)
$V_{in(min)}$	minimum RMS line voltage measured after the rectifier and EMI filter. $V_{in(min)}$ is equal to 90Vrms or 108Vrms depending on the AC Line Voltage operating range.
V_{link}	nominal PFC output voltage; V_{link} = 400V when $V_{in(min)}$ = 90Vrms or V_{link} = 460V when $V_{in(min)}$ = 108Vrms
f_{max}	maximum switching frequency; for the CS1601 f_{max} = 70kHz and the CS1601H f_{max} = 100kHz
L_B	boost inductor specified by rated power requirement
$\alpha<1$	margin factor to guarantee rated output power (P_o) against boost inductor tolerances.

Equation 1 is provided for explanation purposes only. Using substituted required design values for V_{link} and f_{max} gives the following equation:

$$P_o = \alpha \times \eta \times (108V)^2 \times \frac{460V - (108V \times \sqrt{2})}{2 \times 70kHz \times L_B \times 460V} \qquad \text{[Eq.2]}$$

Changing the value for the V_{link} voltage is not recommended.

Solving Equation 2 for the PFC boost inductor L_B gives the following equation:

$$L_B = \alpha \times \eta \times (108V)^2 \times \frac{460V - (108V \times \sqrt{2})}{2 \times 70kHz \times P_o \times 460V} \qquad \text{[Eq.3]}$$

If a value of the boost inductor other than that obtained from Equation 3 above is used, the total output power capability and the minimum input voltage threshold will differ according to Equation 2. Note that if the input voltage drops below 108Vrms and the inductance value is <L_B, the link voltage V_{link} will drop below 460V and fall out of regulation.

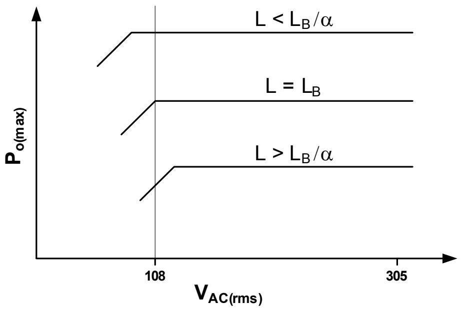


Figure 16. Relative Effects of Varying Boost Inductance

5.5 PFC Output Capacitor

The value of the PFC output capacitor needs to be selected based upon voltage ripple and hold-up requirements. To ensure system stability with the digital controller, the recommended value of the capacitor is within the range of 0.25µF/watt to 0.5µF/watt with a V_{link} voltage of 460V.

5.6 Output IFB Sense and Input IAC Sense

A current proportional to the PFC output voltage, V_{link}, is supplied to the IC on pin IFB and is used as a feedback control signal. This current is compared against an internal fixed-value reference current.

The ADC is used to measure the magnitude of the I_{IFB} current through resistor R_{IFB}. The magnitude of the I_{IFB} current is then compared to an internal reference current of (I_{ref}) 129µA.

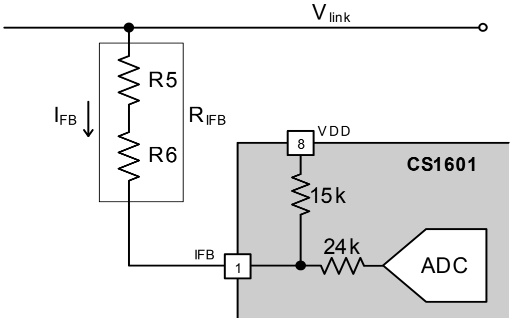


Figure 17. IFB Input Pin Model

Resistor R_{IFB} sets the feedback current and is calculated as follows:

$$R_{IFB} = \frac{V_{link} - V_{DD}}{I_{ref}} = \frac{460V - V_{DD}}{129\mu A} \qquad \text{[Eq.4]}$$

By using digital loop compensation, the voltage feedback signal does not require an external compensation network.

A current proportional to the AC input voltage is supplied to the IC on pin IAC and is used by the PFC control algorithm.

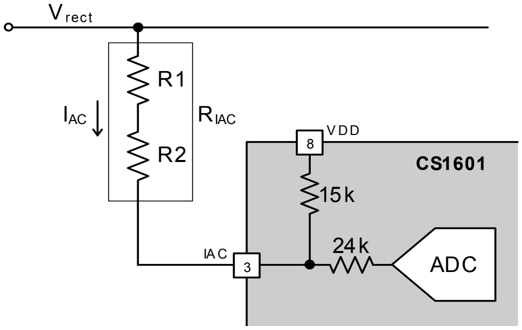


Figure 18. IAC Input Pin Model

Resistor R_{IAC} sets the IAC current and is derived as follows:

$$R_{IAC} = R_{IFB} \qquad \text{[Eq.5]}$$

For optimal performance, resistors R_{IAC} and R_{IFB} should use 1% tolerance or better resistors for best V_{link} voltage accuracy.

5.7 Valley Switching

The zero-current detection (ZCD) pin is monitored for demagnetization in the auxiliary winding of the boost inductor (L_B). The ZCD circuit is designed to detect the V_{Aux} valley/zero crossings by sensing the voltage transformed onto the auxiliary winding of L_B.

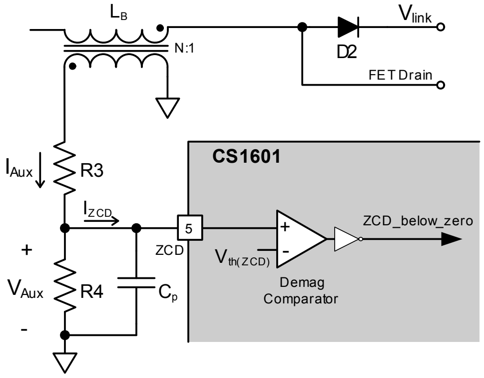


Figure 19. ZCD Input Pin Model

The objective of zero-voltage switching is to initiate each MOSFET switching cycle when its drain-source voltage is at the lowest possible voltage potential, thus reducing switching losses. The CS1601 uses an auxiliary winding on the PFC boost inductor to implement zero-voltage switching.

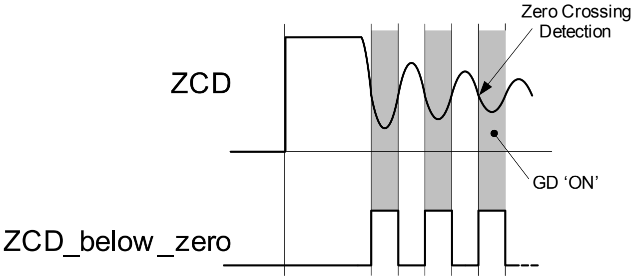


Figure 20. Zero-voltage Switch

During each switching cycle, when the boost diode current reaches zero, the boost MOSFET drain-source voltage begins oscillating at the resonant frequency of the boost inductor and MOSFET parasitic output capacitance. The ZCD_below_zero signal transitions from high to low just prior to a local minimum of the MOSFET drain-source voltage oscillation. The zero-crossing detect circuit ensures that a ZCD_below_zero pulse will only be generated when the comparator output is continuously high for a nominal time period (t_{ZCB}) of 200ns. Therefore, any negative edges on the comparator's output due to spurious glitches will not cause a pulse to be generated.

Due to the CS1601's variable-frequency control, the MOSFET switching cycle will not always be initiated at the first resonant valley. The external circuitry should be designed so that the current (I_{ZCD}) at the ZCD pin is approximately ±1.0mA. The table below depicts approximate values for R3 and R4 for a range of boost-to-auxiliary inductor turns ratio, N.

N	~R3	~R4
9	46kΩ	1.75kΩ
10	42kΩ	1.75kΩ
11	37.5kΩ	1.75kΩ
12	35.5kΩ	1.75kΩ
13	32kΩ	1.75kΩ
14	29.5kΩ	1.75kΩ
15	27.5kΩ	1.75kΩ

Table 1. Aux Inductor Turns Ratio vs. R3 and R4

Resistors R3 and R4 were calculated using $V_{link} = 460V$ and $C_p = 10pF$.

Equation 6 is used to calculate the cut-off frequency defined by the RC circuit at the ZCD pin.

$$f_c = 1/(2\pi(R3 \| R4)C_p) \qquad \text{[Eq.6]}$$

where:

f_c	The cut-off frequency, f_c, needs to be 10x the ringing frequency.
C_p	Capacitance at the ZCD pin

5.8 Brownout Protection

The CS1601 brownout detection circuit monitors the peak of the V_{rect} input voltage and disables the PWM switching when it drops below a predetermined threshold. Hysteresis and minimum detection time are provided to avoid brownout detection during short input transients. When brownout is detected, the CS1601 enters standby mode. On recovery from brownout, it re-enters normal operating mode.

Current I_{AC} is proportional to the AC input voltage V_{rect}, where $V_{rect} = R_{IAC} x I_{AC}$ and $R_{IAC} = R1+R2$ (see Figure 18 on page 11). The digitized current applied to the IAC pin is monitored by the brownout protection algorithm. When V_{rect} drops below the brownout detection threshold, the CS1601 triggers a timer. The IC asserts the brownout protection and stops the gate-drive switching only if the timer exceeds 56ms. This is the equivalent of 7 rectified line cycles at 60Hz.

During the brownout state, the device continues monitoring the input line voltage. The device exits the brownout state when I_{AC} exceeds the brownout upper threshold for at least 56ms. Typical values for the lower ($I_{BP(lower)}$) and upper ($I_{BP(upper)}$) brownout thresholds are 31.6µA and 39.6µA, respectively.

The overpower protection may activate prior to brownout protection, depending on the load.

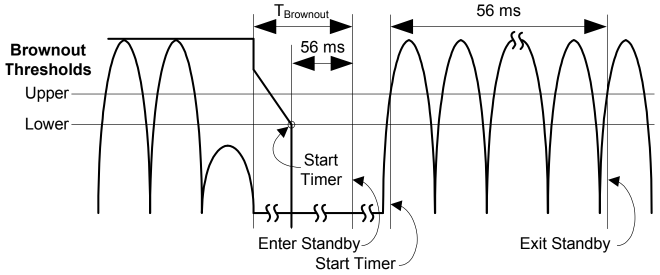


Figure 21. Brownout Sequence

The maximum response time of the brownout protection feature occurs at light-load conditions. It is calculated by Equation 7.

$$T_{Brownout} = 8\,ms + \frac{8\,ms}{5\,V}(128\,V - V_{BP(th)}) + 56\,ms \qquad \text{[Eq.7]}$$

$$= 8 + \frac{8}{5}(128 - 94.8) + 56 = 117ms$$

where:

$V_{BP(th)}$ Brownout threshold voltage, $V_{BP(th)} = I_{BP(lower)} x R_{IAC}$

5.9 Overvoltage Protection

The overvoltage protection (OVP) will trigger immediately and stop the gate drive when the current into the IFB pin (I_{OVP}) exceeds 105% of the reference current (I_{ref}) value. The IC resumes gate drive switching when the measured current at IFB drops below $I_{OVP} - I_{OVP(Hy)}$. Equation 8 is used to calculate the OVP threshold (V_{OVP}).

$$V_{OVP} = R_{IFB} \times I_{OVP} + V_{DD} \qquad \text{[Eq.8]}$$

5.10 Overcurrent Protection

To limit boost inductor current through the FET and to prevent boost inductor saturation conditions, the CS1601 incorporates a cycle-by-cycle peak inductor current limit circuit using an external shunt resistor to 'sense' the FET source current accurately. The overcurrent protection (OCP) circuit is designed to monitor the current when the active switch is turned on. The OCP circuit is enabled after the leading-edge blanking time (t_{LEB}). The shunt voltage is compared to a reference voltage, $V_{cs(th)}$, to determine whether an overcurrent condition exists. The OCP circuit triggers immediately, allowing the OCP algorithm to turn off the gate driver.

The overcurrent protection circuit is also designed to monitor for a catastrophic overcurrent occurrence by sensing sudden and abnormal operating currents. A second OCP threshold, $V_{cs(clamp)}$, determines whether a severe overcurrent condition exists. This immediately turns off the gate drive, and the system enters a restart mode. The CS1601 inhibits all switching operations for approximately 1.6ms and then attempts to restart normal operation.

5.11 Overpower Protection

The CS1601 incorporates an internal overpower protection (OPP) algorithm that provides protection from overload conditions. This algorithm uses the condition that output power is a function of the boost inductor (see section *5.4 Output Power and PFC Boost Inductor* on page 10).

Under moderate overload, V_{link} may droop up to 10% while maintaining rated power and PFC. Further increasing the load current causes V_{link} to drop below the startup threshold (~360V). Below this threshold, the circuit switches the operating mode to startup with more power available to raise V_{link}. As V_{link} reaches its nominal value, startup mode is canceled and power is now limited to the rated value. If the overload is still present, this cycle will repeat.

If a sustained overload, or a repeated cycle of overload events, is detected for greater than 112 ms, the CS1601 shuts down for 2.5 seconds and then attempts to restart.

5.12 Open/Short Loop Protection

If the PFC output sense resistor, R_{IFB}, fails (open or short to GND), the measured output voltage decreases at a slew rate of about 2 V/µs, which is determined by the ADC sampling rate. The IC stops the gate drive when the measured output voltage is lower than the measured line voltage. The IC resumes gate drive switching when the current into the IFB pin becomes larger than or equal to the current into the IAC pin, and V_{link} is greater than the peak of the line voltage ($V_{rect(pk)}$). The maximum response time of open/short loop protection for R_{IFB} is about 150 µs.

If the PFC input sense resistor R_{IAC} fails (open or short to GND), the current reference signal supplied to the IC on pin IAC falls to zero.

5.13 Internal Overtemperature Protection

An internal thermal sensor triggers a shutdown when the temperature exceeds 135°C (nominal) on the silicon. The sensor sends a signal to the core that supplies current to all internal digital logic, cutting off power from them. Once the temperature of the IC has dropped by 9°C (nominal), the sensor resets, allowing power to the logic.

5.14 Standby ($\overline{\text{STBY}}$) Function

The standby ($\overline{\text{STBY}}$) pin provides a means by which an external signal can cause the CS1601 to enter a non-operating, low-power state. The $\overline{\text{STBY}}$ input is intended to be driven by an open-collector/open-drain device. Internal to the pin, there is a pull-up resistor connected to the V_{DD} pin, as shown in Figure 22. Since the pull-up resistor has a high impedance, a filter capacitor (up to 1000pF) may be required on this pin.

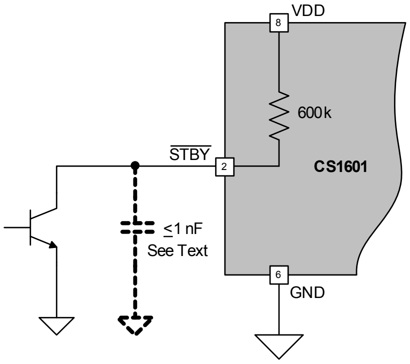


Figure 22. $\overline{\text{STBY}}$ Pin Connection

When the $\overline{\text{STBY}}$ pin is not used, it is recommended that the pin be tied to V_{DD} (pulled high).

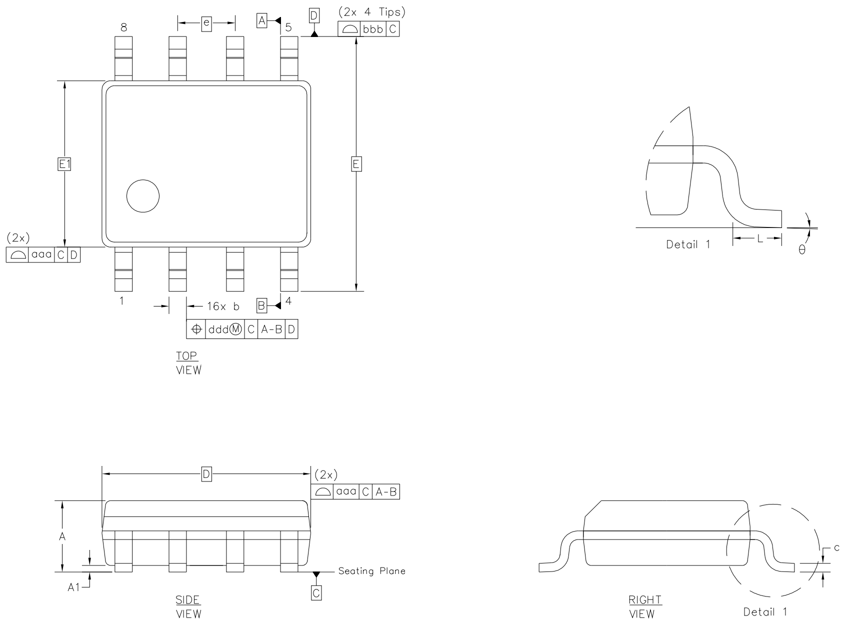
5.15 Summary of Equations

Eq. #	Equation
1	**Output Power** (page 10) $P_o = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times L_B \times V_{link}}$
2	**Output Power with recommended values** (page 10) $P_o = \alpha \times \eta \times (90Vrms)^2 \times \frac{400V - (90Vrms \times \sqrt{2})}{2 \times 70kHz \times L_B \times 400V}$
3	**Boost Inductor** (page 10) $L_B = \alpha \times \eta \times (90Vrms)^2 \times \frac{400V - (90Vrms \times \sqrt{2})}{2 \times 70kHz \times P_o \times 400V}$
4	**Output IFB Sense Resistor** (page 11) $R_{IFB} = \frac{V_{link} - V_{DD}}{I_{ref}} = \frac{400V - V_{DD}}{129\mu A}$
5	**Input IAC Sense Resistor** (page 11) $R_{IAC} = R_{IFB}$
6	**Auxiliary Winding Cut-off Frequency** (page 12) $f_c = 1/(2\pi(R3 \parallel R4)C_p)$
7	**Maximum Response Time for Brownout**: (page 12) $T_{Brownout} = 8\,ms + \frac{8\,ms}{5\,V}(128\,V - V_{BP(th)}) + 56\,ms$
8	**Overvoltage Protection** (page 12) $V_{OVP} = R_{IFB} \times I_{OVP} + V_{DD}$
9	**Boost Inductor Peak Current** $I_{LB(pk)} = \frac{4 \times P_O}{\eta \times V_{in(min)} \times \sqrt{2}}$
10	**Boost Inductor RMS Current** $I_{LB(rms)} = \frac{P_O}{V_{in(min)} \times \eta}$
11	**V_{link} Voltage Ripple** $\Delta V_{link(rip)} = \frac{P_O}{2\pi \times f_{line(min)} \times V_{link} \times C_{out}}$

Variables/Recommended Values	
P_o	Rated output power of the system.
η	Efficiency of the boost converter (estimated as 100% by the PFC algorithm).
$V_{in(min)}$	Minimum RMS line voltage is 90Vrms, measured after the rectifier and EMI filter.
V_{link}	Nominal PFC output voltage must be 400V.
f_{max}	Maximum switching frequency is 70kHz.
L_B	Boost inductor specified by rated power requirement.
α	Margin factor to guarantee rated output power (P_o) against boost inductor tolerances.
R_{IAC}	Value of the IAC pin sense resistor(s).
R_{IFB}	Value of the IFB pin sense resistor(s).
I_{ref}	Value of the fixed, internal reference current.
f_c	The cut-off frequency, f_c, needs to be 10x the ringing frequency or f_c = 10MHz.
C_p	Capacitance at the ZCD pin. C_p<10pF.
$V_{BP(th)}$	Brownout threshold voltage. $V_{BP(th)}$ = 94.8V.
C_{out}	Value of the output capacitor in mF.
$f_{line(min)}$	Minimum line frequency.
V_{DD}	IC Supply Voltage.
V_{OVP}	OVP threshold.
I_{OVP}	Current into the IFB pin.

6. PACKAGE DRAWING

SOIC-8 NARROW (150 MIL BODY) PACKAGE DRAWING



	MILLIMETERS			INCHES		
Dimension	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	- -	- -	1.75	- -	- -	0.069
A1	0.10	- -	0.25	0.004	- -	0.010
b	0.31	- -	0.51	0.012	- -	0.020
c	0.10	- -	0.25	0.004	- -	0.010
D	4.90 BSC			0.193 BSC		
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
L	0.40	- -	1.27	0.016	- -	0.050
Θ	0°	- -	8°	0°	- -	8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ddd	0.25			0.010		

Notes:

1. Controlling dimensions are in millimeters
2. Dimensions and Tolerances per ASME Y14.5M
3. This drawing conforms to JEDEC outline MS-012, variation AA for standard SOIC-8 narrow body
4. Recommended reflow profile is per JEDEC/IPC J-STD-020

7. ORDERING INFORMATION

Part #	Temperature Range	Package Description
CS1601-FSZ	-40°C to +125°C	8-lead SOIC, Lead (Pb) Free
CS1601H-FSZ	-40°C to +125°C	8-lead SOIC, Lead (Pb) Free

8. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating[a]	Max Floor Life[b]
CS1601-FSZ	260°C	2	365 Days
CS1601H-FSZ	260°C	2	365 Days

[a] MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

[b] Stored at 30°C, 60% relative humidity.

9. REVISION HISTORY

Revision	Date	Changes
PP5	MAY 2011	Updated *Typical Electrical Performance* section.
PP6	JUN 2011	Updated *Characteristics and Specifications* section.
F1	SEP 2011	Finalized. Updated *Characteristics and Specifications* section.
F2	JAN 2012	Edited for content and clarity. Corrected typographical errors.
F3	FEB 2012	Revised MSL rating.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to http://www.cirrus.com

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