LANfinity™ CN7221

Home Networking Physical Layer Device with Integrated Analog Front End Circuitry

This document describes the **CN7221** Home Networking Physical Layer (PHY) with Integrated Analog Front End (AFE). It includes device pinouts, signal descriptions, and timing diagrams. The **CN7221** allows home networks to operate over common telephone wires at 1 Mbps. The **CN7221** simplifies system designs and improves their reliability by eliminating the need for a separate AFE comprised of discrete components.

The **CN7221** supports the emerging home phoneline networking standard proposed by the Home Phoneline Networking Alliance (HomePNA). Conexant has announced plans to release a family of multifunction home phoneline networking chipsets. The first products to be announced in this family include the **RS7111A** 1/10/100 PCI/CardBus Multifunction Controller, the **RS7220** Home Networking PHY, the **RS7112** Multifunction Controller with Integrated PHY, and the **CN7221** Home Networking PHY with Integrated AFE (see Ordering Information, page 2).

The HomePNA phoneline network utilizes existing telephone wiring to connect computers and devices without interrupting phone service. Industry-standard home networking products will enable a variety of home computing opportunities including

- shared Internet access using a single phone line
- printer/peripheral sharing
- file and application sharing
- networked gaming

The **CN7221** can be combined with the **RS7112** Multifunction PCI/CardBus Controller and Conexant's host-controlled (HCF) V.90/K56flex modem to provide a variety of home networking plus 56 Kbps modem solutions.

Features

- Supports the HomePNA 1.0 specification for a home phoneline network
- 1 Mbps data rate
- Integrated Analog Front End
- Configurable transmit power level; high- and low-power
- Configurable transmit data rate; low- and high-speed
- 32-pin TQFP package

HomePNA 1.0 Specification Features

- Meets HomePNA certification test requirements
- Uses existing phonelines, no new wires required
- Compatible with existing services
  - Internet access, voice services, and home network coexist on the same wire
- Robust protocol assures performance over poor wiring infrastructure
- FCC Part 15- and Part 68-compliant

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Ordering Information

Product	Package	Device Number
CN7221 HomePNA 1.0 Physical Layer with Integrated Analog Front End	32-pin TQFP	11625-11
Related Products		
RS7112 Multifunction PCI/CardBus Ethernet and HomeLAN Controller with Integrated HomePNA 1.0 Physical Layer and 56 Kbps HCF/HSF Modem Interface	176-pin TQFP	11623-14
RS7112-LAN Multifunction PCI/CardBus Ethernet and HomeLAN Controller with Integrated HomePNA 1.0 Physical Layer Only	176-pin TQFP	11623-12
RS7111A Multifunction PCI/CardBus Ethernet and HomeLAN Controller with V.90 HCF Modem Interface	176-pin TQFP	11617-14
RS7111A-LAN Multifunction PCI/CardBus Ethernet and HomeLAN Controller Only	176-pin TQFP	11617-12
RS7220 HomePNA 1.0 Physical Layer device	64-pin TQFP	R8293-11

Typical Application

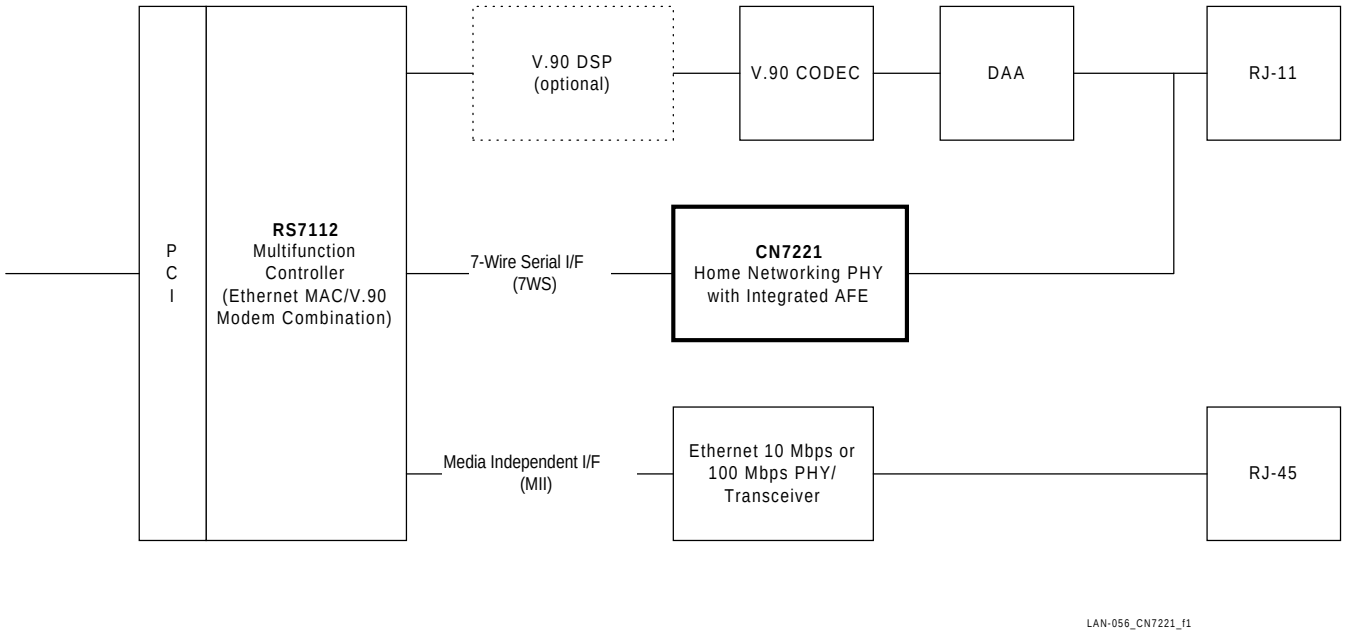


Figure 1. Typical Application

Description

The typical application shown in Figure 1 displays a multifunction PCI Network Interface Card (NIC). The NIC incorporates the **RS7112** Home Networking Controller, the **CN7221** Home Networking PHY with Integrated AFE, and a V.90 56 Kbps host-controlled modem. The **RS7112's** 7-wire serial interface (7WS) is used to support the **CN7221**.

Home Networking

The home phoneline network is an Ethernet-compatible LAN running over the random-tree wiring found in nearly all homes. It does not require any hubs, routers, splitters, filters or terminations. Initial products are PC network interface cards, which will interface home computers directly to the network via an in-home telephone jack. Home phoneline networking will also work with current Internet access technologies, such as cable modems, V.90 and ADSL.

Functional Description

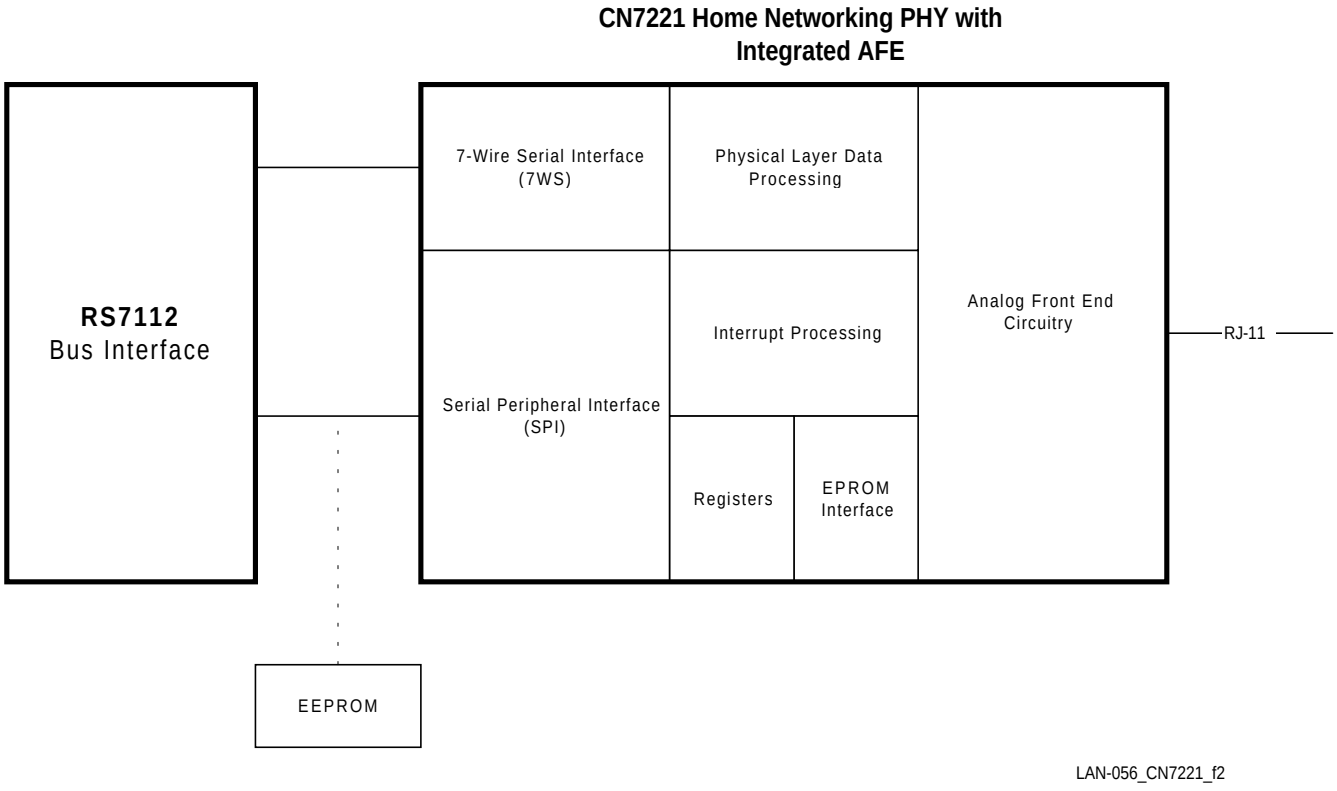


Figure 2. CN7221 Device Block Diagram

Overview

The **CN7221** PHY + AFE resides between the **RS7112** and the physical medium and is responsible for receiving and transmitting data on that physical medium, detecting collisions on the physical medium, and translating data to and from the **RS7112**. For the purpose of this discussion, the interface to the **RS7112** is referred to as the back end.

The discussion of the back end briefly describes the signals involved in that interface as well as some of the operation of those signals. More detailed information may be gathered from the section of this document on the 7-wire serial interface itself (page 5).

Back End (PHY to MAC Interface)

The back end interface is wholly defined by the seven following signals: HLAN_TX_CLK, HLAN_TX_EN, HLAN_TXD, HLAN_RX_CLK, HLAN_CRS, HLAN_RXD, and HLAN_COL. The Tx signals are sampled on the falling edge of HLAN_TX_CLK and the Rx signals are changed on the falling edge of the HLAN_RX_CLK. HLAN_COL may change on either edge of either the HLAN_TX_CLK or the HLAN_RX_CLK. All signals are active high.

Due to the nature of the encoding/decoding algorithm as well as the collision detection algorithm used in the **CN7221**, the resulting variable bit rate forces the PHY to "hold off" the MAC data stream by gating the HLAN_RX_CLK and HLAN_TX_CLK signals. Gating is done in a manner guaranteed to be glitch-free.

System Signals

The system level signals provide hardware level initialization, configuration and status indications from the device. They are shown in Table 1.

The HLAN_OSC pin is the 60 MHz clock input pin.

The HLAN_IRQ signal is an active-low interrupt signal intended for use as a level-sensitive interrupt to an external processor. All interrupt sources are maskable and capable of being stimulated through software via the ISR and IMR programmable registers.

Table 1. System Signals

Signal	Description
HLAN_RESET#	Asynchronous system reset
HLAN_IRQ#	Active low processor interrupt
HLAN_OSC	60 MHz oscillator input

Seven Wire Serial (7WS) Interface Signals

The 7-Wire serial interface provides the digital interface to the Ethernet MAC.

The seven signals that comprise the 7WS are HLAN_TX_CLK, HLAN_TX_EN, HLAN_TXD, HLAN_RX_CLK, HLAN_CRS, HLAN_RXD, and HLAN_COL. Of these, only HLAN_TX_EN and HLAN_TXD are inputs to the PHY; the other five are outputs from the PHY. These signals behave differently depending on which operation is currently happening in the PHY. The operations of the PHY are as follows:

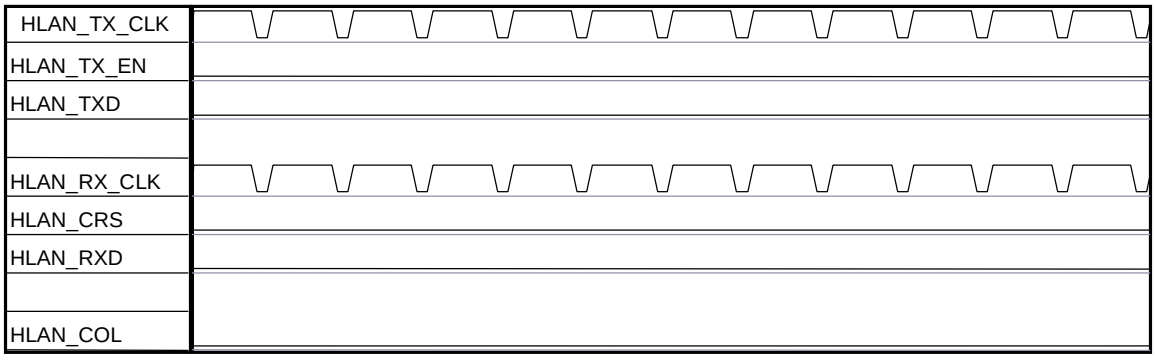
- Idle (no activity in either direction)
- RxPKT (receiving data)
- TxPKT (transmitting data).

The subsequent subsections analyze each 7WS-related state of the PHY in detail.

Table 2. 7WS Interface Signals

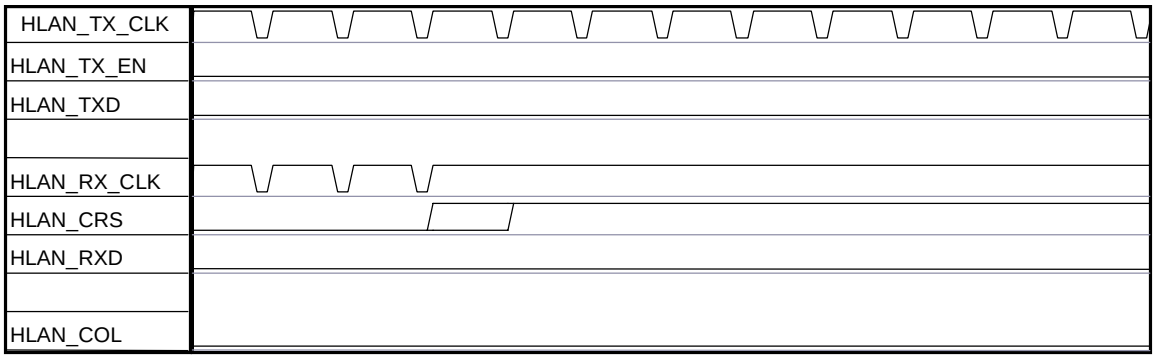
Signal	Description
HLAN_TX_CLK	Transmit clock
HLAN_TX_EN	Transmit enable
HLAN_TXD	Transmit data
HLAN_RX_CLK	Receive clock
HLAN_CRS	Receive carrier sense
HLAN_RXD	Receive data
HLAN_COL	Collision (active high)

Idle State



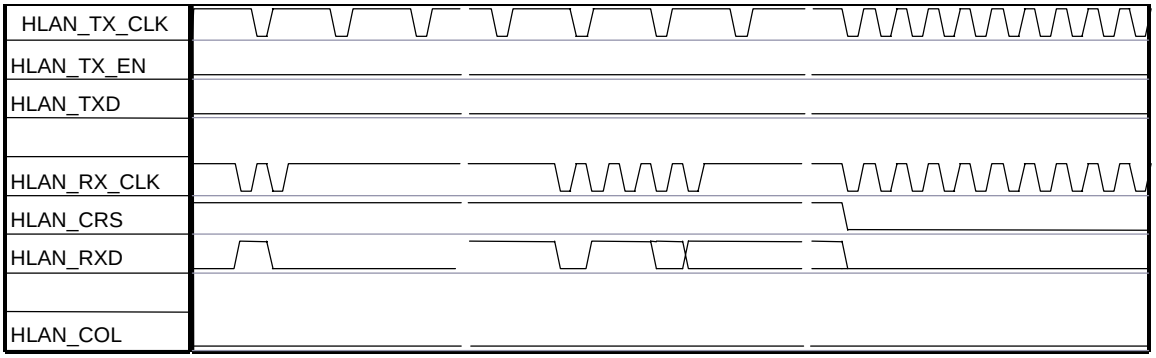
HLAN_RX_CLK and HLAN_TX_CLK are synchronized to the same phase. All other signals are inactive. The two clock signals toggle low for 116.7ns and high for 466.7ns, for an overall period of 583.3ns (about 1.7MHz).

RxPKT — Carrier Sense Asserted



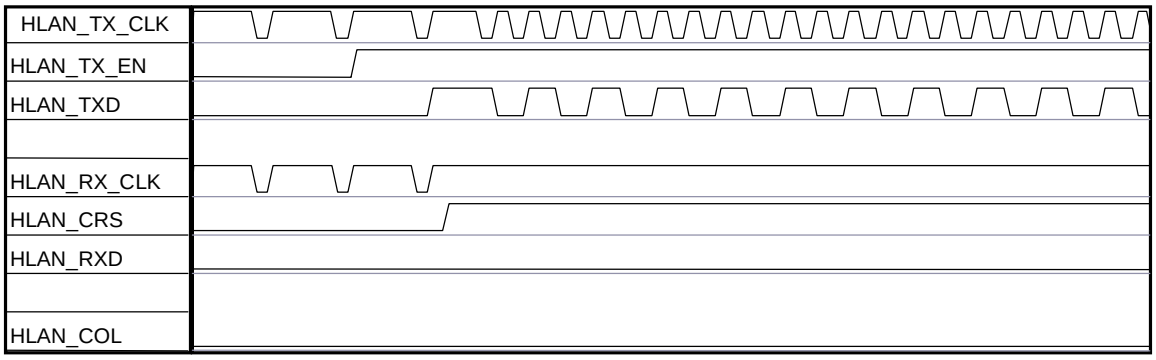
HLAN_RX_CLK becomes disabled (and left in the high state) as soon as HLAN_CRS is asserted. HLAN_CRS may be asserted at a multiple of 116.7ns after the rising edge of HLAN_RX_CLK (that is, 0ns, 116.7ns, 233.3ns, 350.0ns, or 466.7ns). The clock is re-enabled about 135 uS into the packet.

RxPKT — HLAN_RX_CLK Active and HLAN_CRS Cleared



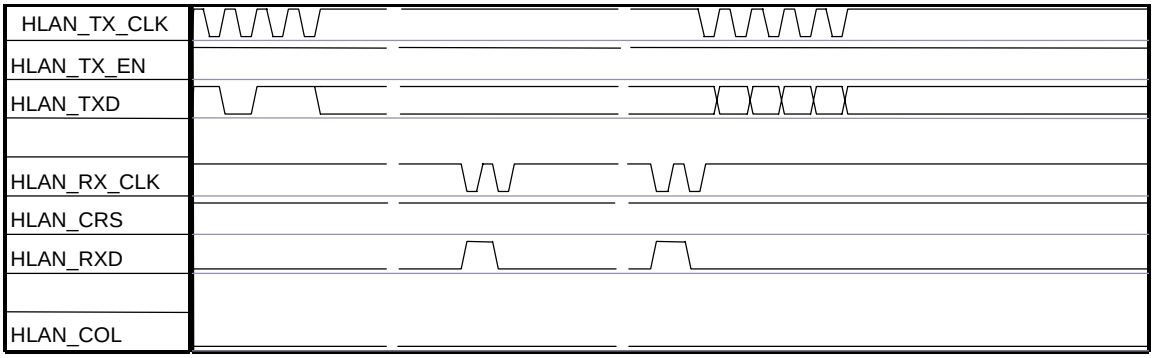
HLAN_RX_CLK and HLAN_TX_CLK are unrelated to each other during this time. When a symbol has been received and decoded, HLAN_RX_CLK toggles at a rate of 233.3ns (full period, 50% duty cycle) in order to shift out the three to six bits encoded in the symbol. The middle portion of this diagram shows the end of the preamble, followed by an SFD and the beginning of the datagram. HLAN_CRS will fall approximately 16us after the last received symbol. Once HLAN_CRS falls, HLAN_RX_CLK and HLAN_TX_CLK are toggled continuously at 233.3ns for 97 cycles, after which the PHY returns to the Idle state.

TxPKT — HLAN_TX_EN Asserted



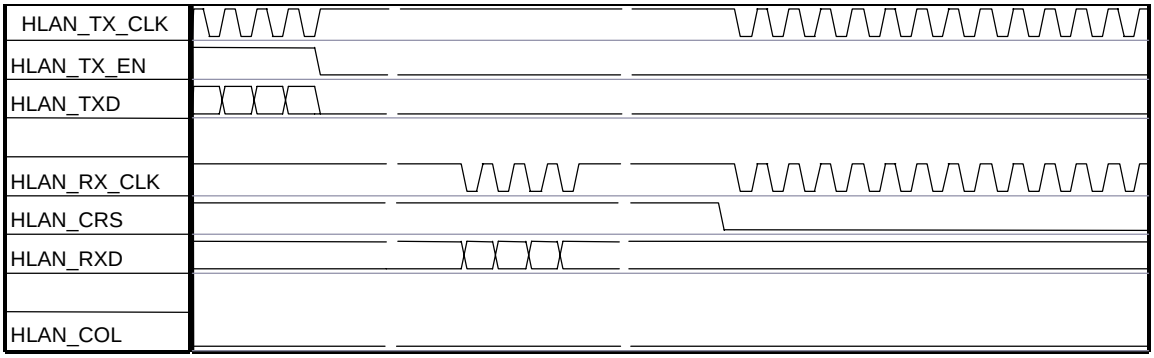
Once HLAN_TX_EN is asserted, the PHY stops HLAN_RX_CLK, asserts HLAN_CRS, and toggles HLAN_TX_CLK at 233.3ns.

TxPKT — HLAN_RX_CLK Active



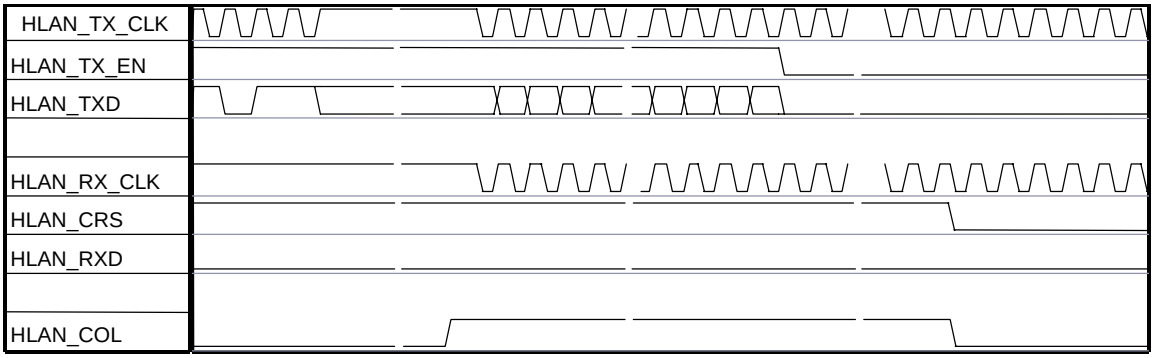
HLAN_TX_CLK continues to toggle at 233.3ns until the SFD is observed, as shown in the first section of the above diagram. At this point, HLAN_TX_CLK is disabled (high) until the AID header has been transmitted on the wire (or until a HLAN_COL has been detected). This takes about 120us, at which time HLAN_RX_CLK starts toggling, thereby shifting 32 bits of preamble and SFD back to the MAC. Sometime later, the HLAN_TX_CLK restarts as symbols get sent onto the wire in an analogous manner as HLAN_RX_CLK during packet reception.

TxPKT — HLAN_TX_EN Cleared



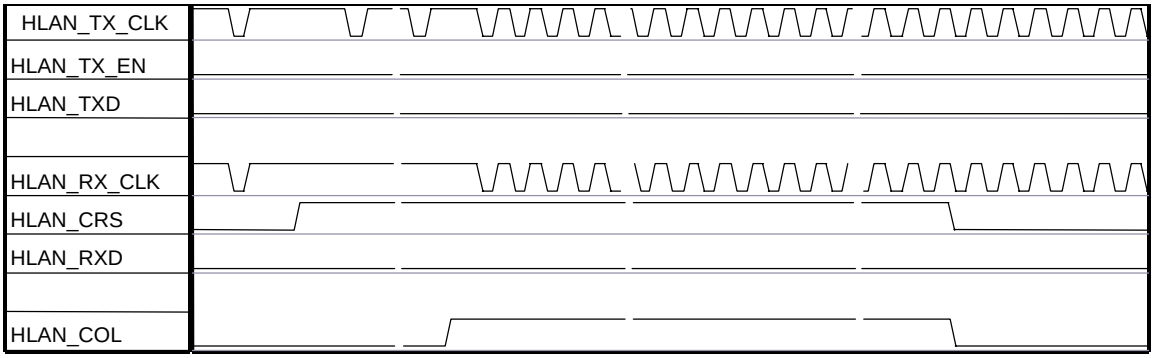
Once HLAN_TX_EN is cleared, the last symbol gets encoded and transmitted, the looped-back data is presented back to the MAC, and about 22us later, HLAN_CRS falls. Once HLAN_CRS falls, HLAN_TX_CLK and HLAN_RX_CLK toggle with a period of 233.3ns for 97 clocks, after which the system returns to the Idle state.

TxPKT — HLAN_COL Asserted



HLAN_COL will be asserted some time after the preamble and SFD have been clocked in. HLAN_TX_CLK and HLAN_RX_CLK are then clocked with a period of 233.3ns until HLAN_CRS drops. HLAN_TX_EN drops about 32 clocks after HLAN_COL was asserted. HLAN_CRS and HLAN_COL are dropped together after more than 500 clocks (about 120us). HLAN_TX_CLK and HLAN_RX_CLK keep toggling at 233.3ns period for roughly another 100 clock cycles, when the system returns to the idle state.

RxPKT — HLAN_COL Asserted



HLAN_COL may be asserted up to 120us after HLAN_CRS has been asserted. Once HLAN_COL has been asserted, HLAN_TX_CLK and HLAN_RX_CLK run at a period of 233.3ns per cycle until 97 cycles after HLAN_COL and HLAN_CRS are cleared. It can take up to about 60us for HLAN_CRS to clear.

Serial Peripheral Interface

The SPI provides a software interface for configuration and status of the **CN7221**.

The SPI signals are composed of: HLAN_SPI_CLK, HLAN_SPI_DOUT, HLAN_SPI_DIN, and HLAN_SPI_CS#.

Commands are issued to the device by asserting the HLAN_SPI_CS# signal (active low), shifting in an eight-bit opcode; if the operation is a read or a write, the opcode is followed by an eight-bit register address. If the operation is a write, the address is followed by an eight-bit data byte. If the operation is a read, the HLAN_SPI_DOUT pin will shift out an eight bit data byte representing the contents of the register referenced by the address field. All commands must be initiated with a high-to-low transition on the HLAN_SPI_CS# pin. The device also may be commanded to set or clear its WE flag. This flag is cleared upon reset, and disables all write operations when in that state.

Opcodes are as follows:

0000 0110 SET WE
0000 0100 CLEAR WE
0000 0011 READ
0000 0010 WRITE

Timing for the various signals in SPI mode is defined in Table 4 and in Figure 3.

The HLAN_SPI_DIN signal should not be changed until at least 100ns after the rising edge of HLAN_SPI_CLK. In other words, the HLAN_SPI_DIN signal has a hold time constraint of 100ns past the rising edge of HLAN_SPI_CLK.

Table 3. SPI Signals

Signal	Description
HLAN_SPI_CLK	Serial interface clock
HLAN_SPI_DOUT	Serial data output
HLAN_SPI_DIN	Serial data input
HLAN_SPI_CS#	Serial interface chip select (active low)

Table 4. SPI Timing

Mnemonic	Description	Min	Max	Units
TWIDTHclkl	Positive half-cycle pulse width	400		ns
TWIDTHclkh	Negative half-cycle pulse width	400		ns
TSETcsl	CSN low to rising clock edge	50		ns
TSETcsh	CSN high to rising clock edge	50		ns
TDLYsov	Falling clock edge to SO valid		50	ns
TDLYsoz	Falling clock edge to SO tri-state		100	ns
TSETsiv	SI valid to rising clock edge	50		ns

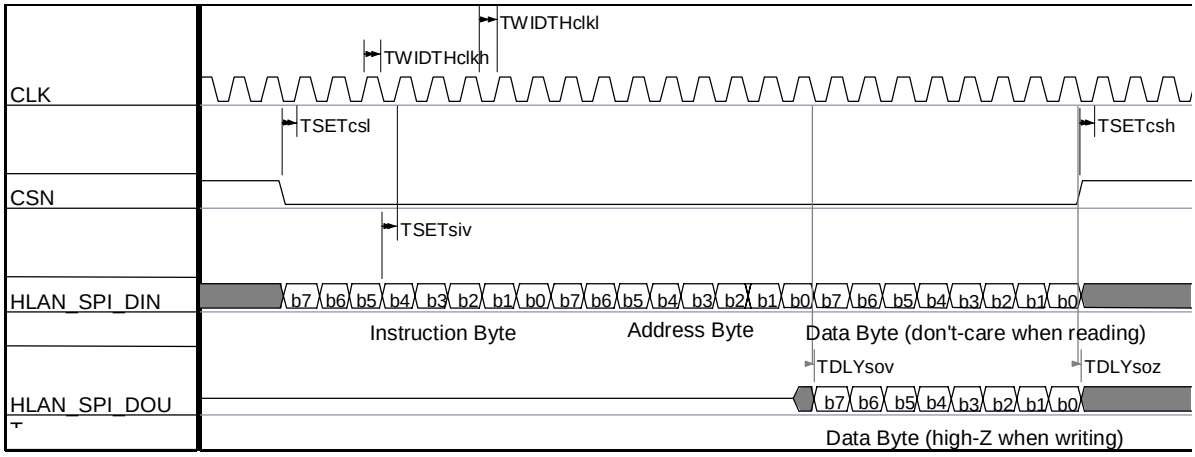


Figure 3. SPI Timing

LANfinity RS7112 Interface

The **RS7112** interface consists of the SPI signals (see page 9), and the HLAN_IRQ# signal.

All SPI registers in the system are readable and writable. The TxSPEED, TxPOWER, and CMDignore bits of the CONTROL register may be set or cleared in two ways: SPI CONTROL register write or remote management command (TxSPEED and TxPOWER only). These methods may overwrite one another. After reset, any change in the state of those pins will update the CONTROL register bits.

Table 5. RS7112 Interface Signals

Signal	Description
HLAN_IRQ#	Active low processor interrupt

Remote Commands

Any node in a home phoneline network may issue remote commands. The effect of a remote command is to set the transmit speed and power of all nodes in the network. A remote command is encoded in the AID header and is identified by having an AID address of 0xFF. The remaining AID header information contains the commanded power and speed. Three identical remote commands must be received before a PHY will respond by changing its' transmit speed and power. Once three identical remote commands have been received, however, the transmit speed and power are updated and bit 1 of the ISTAT register is set.

The PHY will issue three remote commands when any one of bits 8 through 11 of the CONTROL register is set. As soon as these bits are set, the PHY will automatically update it's own transmit speed and power and start issuing the remote command on subsequent packets until three packets have been successfully transmitted (that is, without collision). Once the three remote commands have been sent, bits 8 through 11 of the CONTROL register will be cleared and bit 0 of the ISTAT register will be set.

Pinout Diagram

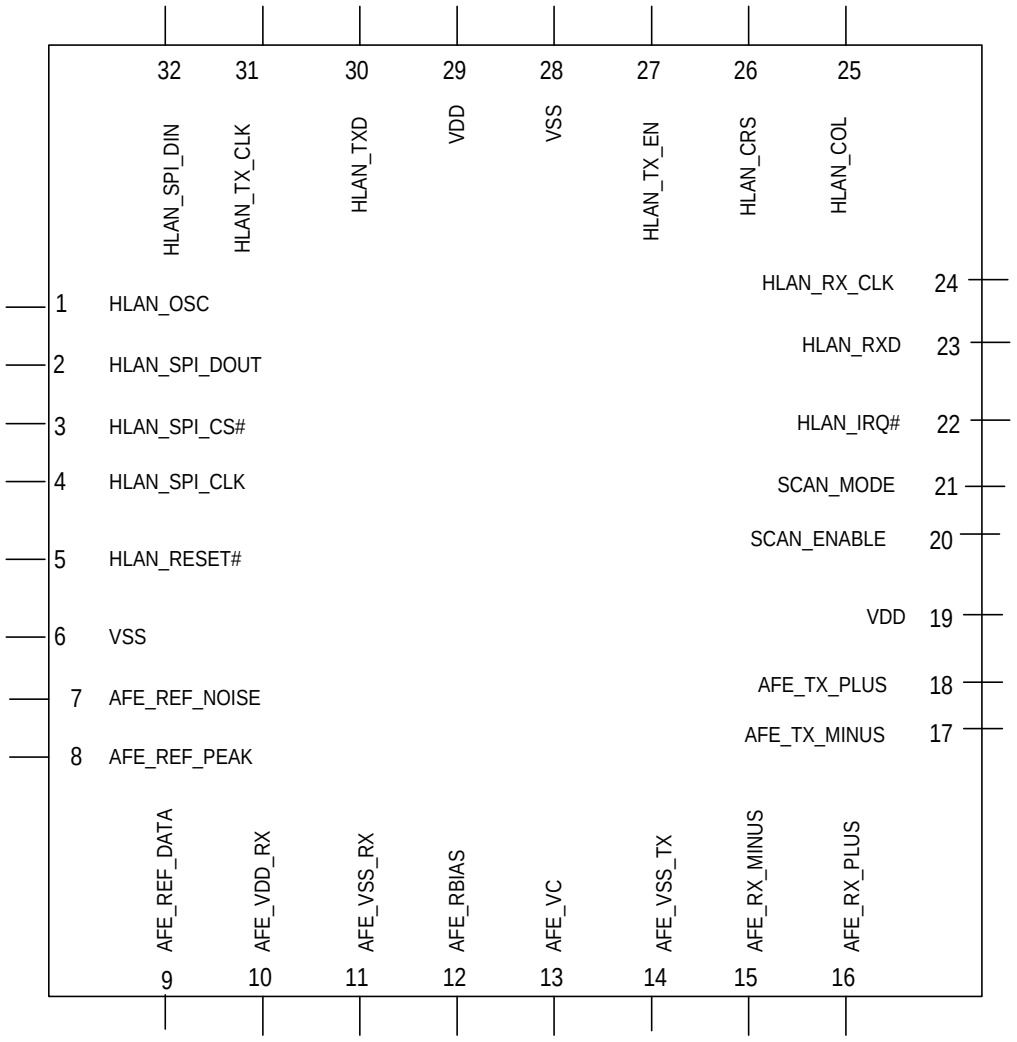


Figure 4. CN7221 32-pin TQFP Pinout Diagram

Pin Designations by Number

Table 6. CN7221 32-pin TQFP Pin Designations by Number

Pin No.	Signal	Pin No.	Signal
1	HLAN_OSC	17	AFE_TX_MINUS
2	HLAN_SPI_DOUT	18	AFE_TX_PLUS
3	HLAN_SPI_CS#	19	VDD
4	HLAN_SPI_CLK	20	SCAN_ENABLE
5	HLAN_RESET#	21	SCAN_MODE
6	VSS	22	HLAN_IRQ#
7	AFE_REF_NOISE	23	HLAN_RXD
8	AFE_REF_PEAK	24	HLAN_RX_CLK
9	AFE_REF_DATA	25	HLAN_COL
10	AFE_VDD_RX	26	HLAN_CRS
11	AFE_VSS_RX	27	HLAN_TX_EN
12	AFE_RBIAS	28	VSS
13	AFE_VC	29	VDD
14	AFE_VSS_TX	30	HLAN_TXD
15	AFE_RX_MINUS	31	HLAN_TX_CLK
16	AFE_RX_PLUS	32	HLAN_SPI_DIN

Pin Designations by Group

Table 7. Pin Designations by Group

Home LAN

Pin Name	Type	Schmitt	Resistive	Drive	Description	Pin Number(s)
HLAN_OSC	I			CMOS	60 MHz oscillator input	1
HLAN_RESET#	I		↓ 25Kohm	CMOS	Active high asynchronous system reset	5
HLAN_IRQ#	O			6mA	Active low processor interrupt	22
HLAN_TX_EN	I		↓ 25Kohm	CMOS	7WS transmit enable	27
HLAN_TXD	I		↓ 25Kohm	CMOS	7WS transmit data	30
HLAN_TX_CLK	O			6mA	7WS transmit clock	31
HLAN_COL	O			6mA	7WS collision (active high)	25
HLAN_CRS	O			6mA	7WS receive carrier sense	26
HLAN_RXD	O			6mA	7WS receive data	23
HLAN_RX_CLK	O			6mA	7WS receive clock	24
HLAN_SPI_CS#	I/O		↑100Kohm	6mA	Serial interface chip select Active low	3
HLAN_SPI_CLK	I/O			6mA	Serial interface clock	4
HLAN_SPI_DOUT	O			6mA	Serial data output	2
HLAN_SPI_DIN	I			CMOS	Serial data input	32

AFE Interface (Reference)

Pin Name	Type	Schmitt	Resistive	Drive	Description	Pin Number(s)
AFE_REF_NOISE					Noise reference filtered with an external 0.0075 uF Cap for data CT comparator.	7
AFE_REF_PEAK					Peak reference filtered with an external 0.0034 uF Cap for peak CT comparator.	8
AFE_REF_DATA					Data reference filtered with an external 0.0134 uF Cap for data CT comparator.	9
AFE_RBIAS					External 1% 2.75kOhm resistor to set reference current.	12
AFE_RX_MINUS					Negative input of the 7.5MHz receive signal	15
AFE_RX_PLUS					Positive input of the 7.5MHz receive signal	16
AFE_TX_MINUS					Negative output of the 7.5MHz TX signal connected to the 50ohm resistor and 1000pF AC coupling Caps.	17
AFE_VDD_RX					RX power supply (3-3.6V or 3.15-3.45)	10
AFE_VSS_RX					RX ground	11
AFE_VSS_TX					TX ground	14
AFE_VC					Middle point of the power supply filtered with an external 10uF Cap.	13
AFE_TX_PLUS					Positive output of the 7.5MHz TX signal connected to the 50ohm resistor and 1000pF AC coupling Caps.	18

Test Signals

Pin Name	Type	Schmitt	Resistive	Drive	Description	Pin Number(s)
SCAN_MODE	I	×	↓	—	Selects different scan modes	21
SCAN_ENABLE	I	×	↓	—	Scan enable (1 = enable scan)	20

Power Pins

Pin Name	Type	Characteristic	Description	Pin Number(s)
VDD	P 5 pins		+3.3V Power	19, 29
VSS	G 7 pins		Ground	6, 28

Electrical Characteristics

Table 8.Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{DD}				V
Input Voltage	V_{IN}				V
Operating Temperature Range	T				^{o}C
Storage Temperature	T_{stg}				^{o}C
Voltage Applied to Outputs in High Z state	V_{hz}				V
DC Input Clamp Current	I_{lk}				mA
DC Input Clamp Current	I_{ok}				mA
Static Discharge Voltage (25 ^{o}C)	ESD				V
Latch-up Current	I_{trig}				mA

Table 9. DC Electrical Characteristics

T_A = 0^{o}C to +70^{o}C, V_{DD} = +3.3V ± 5%, V_{SS} = 0V.

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Low	V_{IL}				V
Input Voltage High	V_{IH}				V
Output Voltage Low @ I_{OL} = 2, 4, 8, 12 mA	V_{OL}				V
Output Voltage High @ I_{OH} = 2, 4, 8, 12 mA	V_{OH}				V

Table 10. AC Electrical Characteristics

TA = 0^{o}C to +70^{o}C, VDD = +3.3V ± 5%, VSS = 0V.

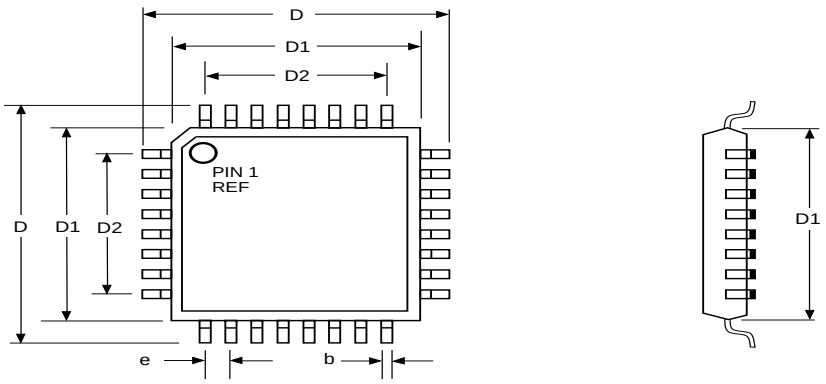
Parameter	Symbol	Min	Typ	Max	Units
Frequency (PCI_CLK)	f_{pck}				MHz
Frequency (8023_MII_TX_CLK) 100 Mbps	f_{xtal}				MHz
Frequency (8023_MII_RX_CLK) 100 Mbps	TBD				MHz
Frequency (8023_MII_TX_CLK) 10 Mbps	TBD				MHz
Frequency (8023_MII_RX_CLK) 10 Mbps	TBD				MHz
Frequency (8023_MII_MDC)	TBD				MHz

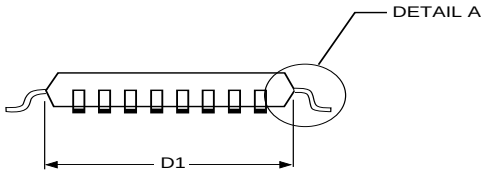
Note: Setup, Hold and Delays are with respect to the rising edge of the respective clock unless specified. PCI Bus signals conform to the PCI Bus Timing Specification.

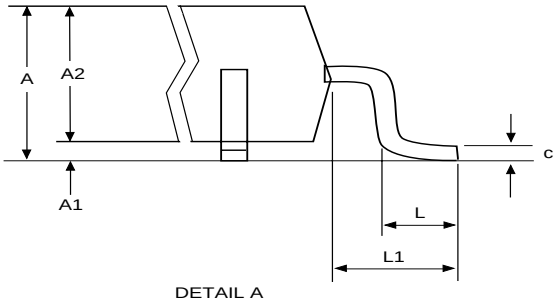
Table 11. Current and Power Characteristics

Mode	Typical Current (mA)	Maximum Current (mA)	Typical Power (W)	Maximum Power (W)	Notes
Active					
Idle					
Power down					

Package Dimensions







Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	8.75	9.25	0.3445	0.3642
D1		7.0 REF		0.2756 REF
D2		5.6 REF		0.2205 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.80 BSC		0.0315 BSC
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity		0.10 MAX		0.004 MAX

Ref: 32-PIN TQFP (GP00-D262)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-TQFP-32 (040395)

Figure 5. 32-pin TQFP Package Dimensions

Further Information
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