Consumer Microcircuits Limited

M-I-X-E-D S-I-G-N-A-L S-O-L-U-T-I-O-N-S

CMX654

V23 Transmit Modulator

D/654/3 June 1998

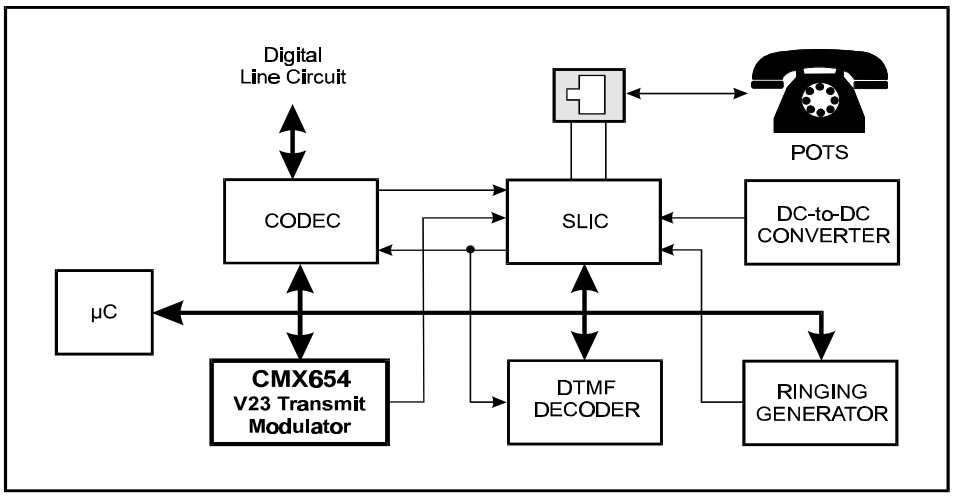
Advance Information

Features

- **1200bits/sec, V23 Transmit Modulator**
- **3.0V to 5.5V Supply: 1mA typical at 3V**
- **Zero Power Mode: 1µA typical**
- **1200bits/sec Tx Data Retiming**
- **3.58MHz Xtal/Clock Rate**
- **Meets ITU and ETSI Specifications**
- **16 Pin SOIC and DIP Packages**

Applications

- **Caller ID generation for:**
  - **ISDN Terminal Adapters**
  - **Wireless Local Loop System**
  - **ISDN PABX Applications**
  - **Pair-Gain Systems**
  - **Public Switched Telephone Networks**
  - **Trunk Exchanges**



1.1 Brief Description

The CMX654 is a low power CMOS integrated circuit for the transmission of asynchronous 1200bits/sec data in accordance with ITU, V.23 and ETSI specifications.

The device incorporates an optional Tx data retiming function. The device can be operated so that only the mark or space tone is produced.
The CMX654 may be used in a wide range of telephone telemetry systems. With a low voltage requirement of 3.0V it is suitable for both portable terminal and line powered applications. A very low current 'sleep' mode (1µA typ.) and operating current of 1mA typ. mean the device is ideal for line powered applications. A 3.58MHz standard Xtal/Clock rate is required and the device operates from a 3.0 to 5.5V supply. Both SOIC (D4) and Plastic DIL (P3) 16-pin package types are available.

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1.2 Block Diagram

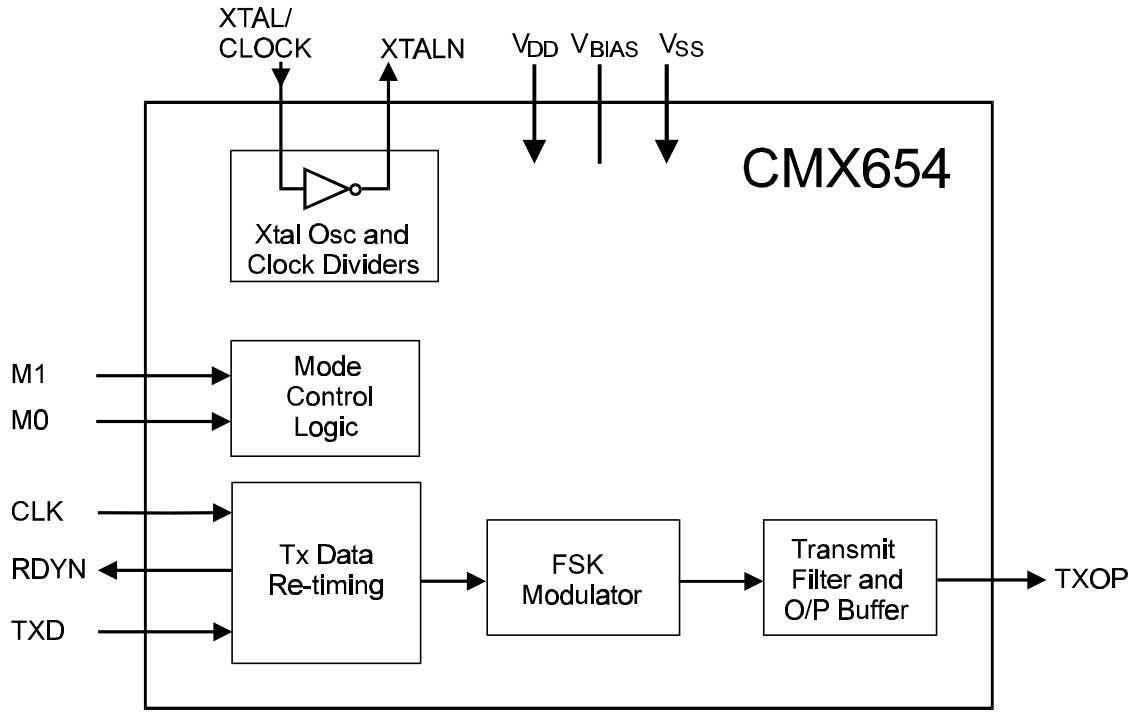


Figure 1 Block Diagram

1.3 Signal List

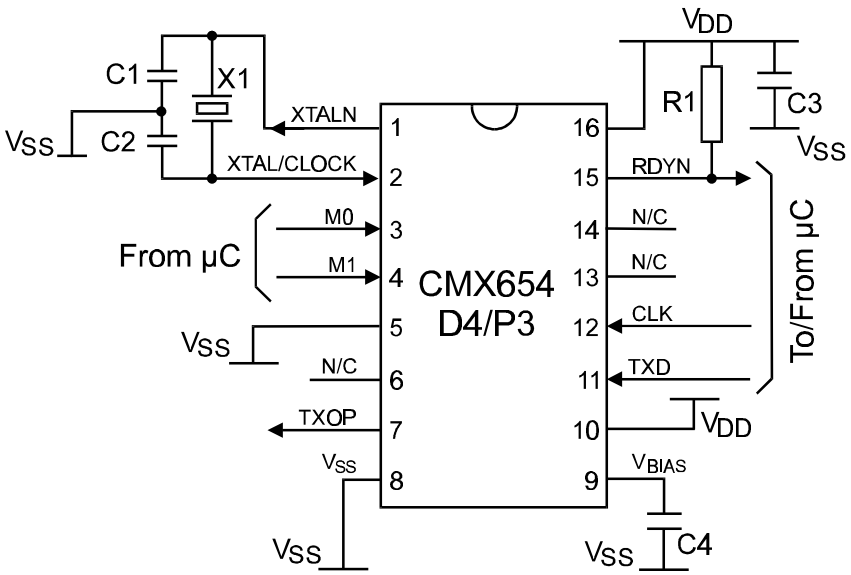
CMX654 D4/P3	Signal		Description
Pin No.	**Name**	**Type**	
1	XTALN	O/P	The output of the on-chip Xtal oscillator inverter.
2	XTAL/CLOCK	I/P	The input to the on-chip Xtal oscillator inverter.
3	M0	I/P	A logic level input for setting the mode of the device. See Section 1.5.2.
4	M1	I/P	A logic level input for setting the mode of the device. See Section 1.5.2.
5	-	-	Connect to V_{SS}
6	-	N/C	No connection, do not connect to this pin.
7	TXOP	O/P	The output of the FSK generator.
8	V_{SS}	Power	The negative supply rail (ground).

CMX654 D4/P3	Signal		Description
Pin No.	**Name**	**Type**	
9	V_{BIAS}	O/P	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
10	-	-	Connect to V_{DD}.
11	TXD	I/P	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See Section 1.5.3.
12	CLK	I/P	A logic level input which may be used to clock data bits into the Tx FSK Data Retiming block.
13	-	N/C	No connection, do not connect to this pin.
14	-	N/C	No connection, do not connect to this pin.
15	RDYN	O/P	"Ready for Tx data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
16	V_{DD}	Power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Notes: I/P = Input
O/P = Output
N/C = No Connection

V_{DD} and V_{BIAS} decoupling are very important. It is recommended that the decoupling capacitors are placed so that connections between them and the device pins are as short as practicable.

1.4 External Components



R1	100kΩ	C1, C2	18pF
X1	3.579545MHz	C3	0.1µF
		C4	0.1µF

Resistors ±5%, capacitors ±10% unless otherwise stated.

Figure 2 Recommended External Components for Typical Application

1.5 General Description

1.5.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the CMX654 is determined by a 3.579545MHz clock present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL/CLOCK input. If supplied from an external source, C1, C2 and X1 should not be fitted.

The on-chip oscillator is turned off in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by CMX654 as well as generating undefined states of the RDYN output.

1.5.2 Mode Control Logic

The CMX654's operating mode is determined by the logic levels applied to the M0 and M1 input pins:

M1	M0	Tx Mode	Data Retime[1]
0	1	1200bits/sec	Tx
1	0	off	-
1	1	'Zero-Power'	-

[1] If enabled.

In the 'Zero-Power' mode, power is removed from all internal circuitry. When leaving 'Zero-Power' mode there must be a delay of 20ms before any Tx data is passed to the device to allow the bias level, filters and oscillator to stabilise. On applying power to the device the mode must be set to 'ZP', i.e. M0=1, M1=1, until V_{DD} has stabilised.

1.5.3 FSK Modulator and Transmit Filter

These blocks produce a tone according to the TXD, M0 and M1 inputs as shown in the table below, assuming data retiming is not being used:

M1	M0	TXD = '0'	TXD = '1'
1	1	-	
1	0	0Hz[1]	
0	1	2100Hz	1300Hz

Note: [1] TXOP held at approx $V_{DD}/2$.

When modulated at the appropriate baud rates, the Transmit Filter and associated external components (see Section 1.6.1) limit the FSK out of band energy sent to the line in accordance with Figure 3 assuming that the signal on the line is at -6dBm or less.

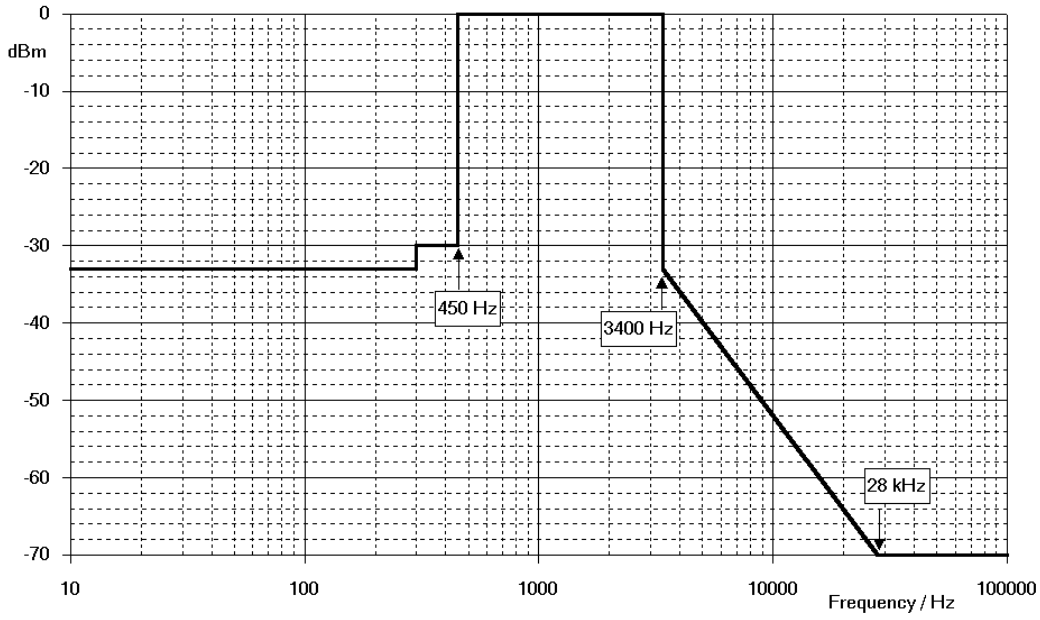


Figure 3 Tx limits

1.5.4 Tx Data Retiming

The Data Retiming block, when enabled in 1200bits/sec transmit mode, requires the controlling μC to load 1 bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical and it may easily be generated by a simple software loop. This facility removes the need for a UART in the μC without incurring an excessive software overhead.

The Tx re-timing circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the RDYN pin is pulled low. The RDYN output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.

So to use the retiming option the CLK input should be held low until the RDYN output is pulled low. When the RDYN pin goes low the next data bit should be applied at the TXD input and the CLK input pulled high and then low within the time limits set out in Figure 6.

To ensure synchronisation between the controlling device and the CMX654 when entering Tx retiming mode, the TXD pin must be held at a constant logic level from when the CLK pin is first pulled low to the end of loading in the second retimed bit. Similarly when exiting Tx retiming mode the TXD pin should be held at the same logic level as the last retimed bit for at least 2 bit times after the CLK line is pulled high.

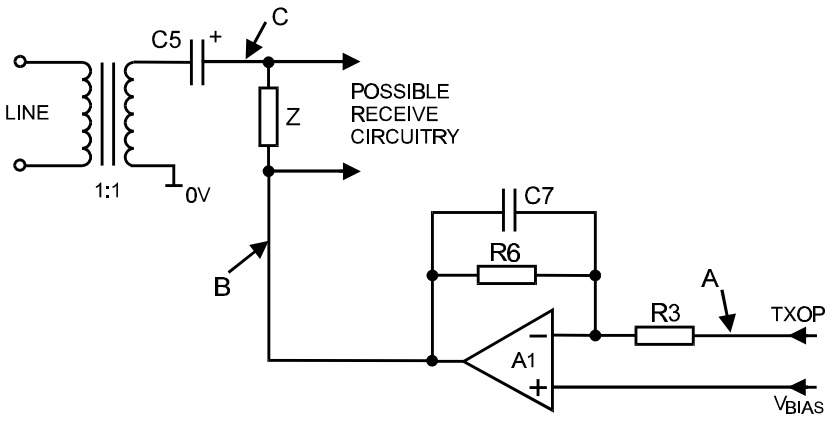
If the data retiming facility is not required, the CLK input to the CMX654 should be kept high at all times. The asynchronous data to the FSK modulator will then be connected directly to the TXD input pin. This is illustrated in Figure 5.

1.6 Application Notes

1.6.1 Line Interface

The signals on the telephone line are not suitable for direct connection to the CMX654. A Line Interface circuit is necessary to:

- Provide high voltage and dc isolation
- Provide the low impedance drive necessary for the line
- Filter the Tx and Rx signals



R3	See below	C5	22µF (±20%)
R6	100kΩ	C7	330pF

Resistors ±1%, capacitors ±10% unless otherwise stated.

Figure 4 Line Interface Circuit

Notes:

- The component(s) 'Z' between points B and C should match the line impedance.
- Device A1 must be able to drive 'Z' and the line.
- R3: The levels in dB (relative to a 775mV rms signal) at 'A', 'B' and 'C' in the line interface circuit are:

'A' = 20Log(V_{DD}/5)
'B' = 'A' + 20Log(100kΩ/R3)
'C' = 'B' - 6

V_{DD}	'A'	R3	'B'	'C'
3.3V	-3.6dB	100kΩ	-3.6dB	-9.6dB
5.0V	0dB	150kΩ	-3.5dB	-9.5dB

1.7 Performance Specification

1.7.1 Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

D4 Package	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

P3 Package	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	+85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Notes: 1. A Xtal frequency of 3.579545MHz ±0.1% is required for correct FSK operation.

Operating Characteristics
For the following conditions unless otherwise specified:

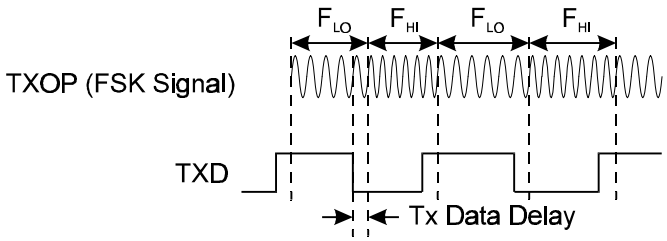
V_{DD} = 3.0V at Tamb = 25°C and V_{DD} = 3.3V to 5.5V at Tamb = -40 to +85°C,
Xtal Frequency = 3.579545MHz ± 0.1%
0dBV corresponds to 1.0Vrms
0dBm corresponds to 775mVrms into 600Ω.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (M0='1', M1='1')	1, 2	-	1	-	µA
I_{DD} (M0 or M1='0') at V_{DD} = 3.0V	1	-	1.0	1.25	mA
I_{DD} (M0 or M1='0') at V_{DD}= 5.0V	1	-	1.7	2.5	mA
Logic '1' Input Level		70%	-	-	V_{DD}
Logic '0' Input Level		-	-	30%	V_{DD}
Logic Input Leakage Current (Vin = 0 to V_{DD}), Excluding XTAL/CLOCK Input		-1.0	-	+1.0	µA
Output Logic '1' Level (I_{OH} = 360µA)		V_{DD}-0.4	-	-	V
Output Logic '0' Level (I_{OL} = 360µA)		-	-	0.4	V
RDYN O/P 'off' State Current (Vout = V_{DD})		-	-	1.0	µA
FSK Retiming					
Tx Data Rate		1194	-	1206	Baud
FSK Modulator					
TXOP Level	3	-1.0	0	+1.0	dB
Twist (Mark Level WRT Space Level)		-2.0	0	+2.0	dB
Tx 1200bits/sec (M1='0', M0='1').					
Bit Rate		0	1200	1212	Baud
Mark (Logical 1) Frequency		1297	-	1303	Hz
Space (Logical 0) Frequency		2097	-	2103	Hz
XTAL/CLOCK Input					
'High' Pulse Width	4	100	-	-	ns
'Low' Pulse Width	4	100	-	-	ns

Notes:
1. At 25°C, not including any current drawn from the CMX654 pins by external circuitry other than X1, C1 and C2.
2. TXD and CLK inputs at V_{SS}, M0 and M1 inputs at V_{DD}.
3. Relative to 775mVrms at V_{DD}= 5.0V for load resistances greater than 40kΩ.
4. Timing for an external input to the XTAL/CLOCK pin.

Data and Mode Timing	**Min.**	**Typ.**	**Max.**	**Units**

Delay to reliable data at TXOP after ZP to Tx mode change	-	-	20.0	ms
Data Retiming Disabled (reference Figure 5)				
Tx Data Delay (TXD to TXOP)	-	0.1	-	ms
Data Retiming Enabled (reference Figure 6)				
T_d = Internal CMX654 delay	-	-	1.0	µs
T_{chi} = CLK High time	1.0	-	-	µs
T_r = RDY low to CLK going low	-	-	800	µs
T_s = Data Set-up time	1.0	-	-	µs
T_h = Data Hold time	1.0	-	-	µs



Note: M0 and M1 are preset and stable. FLO and FHI are the two FSK signalling frequencies.

Figure 5 TXD to TXOP Delay Time

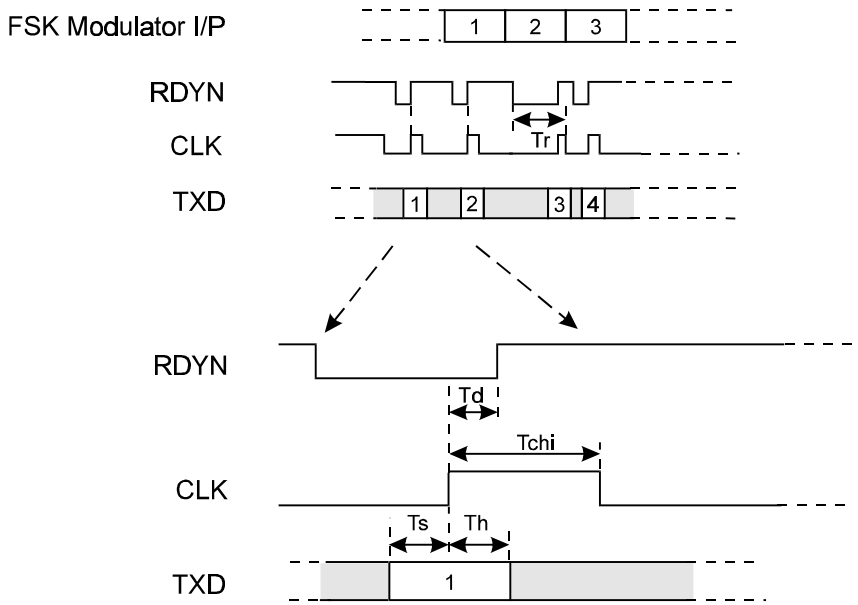
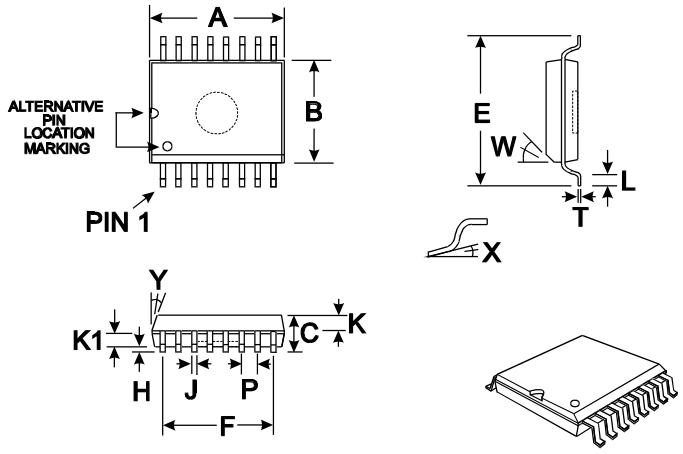


Figure 6 FSK Operation with Tx Data Retiming

1.7.2 Packaging



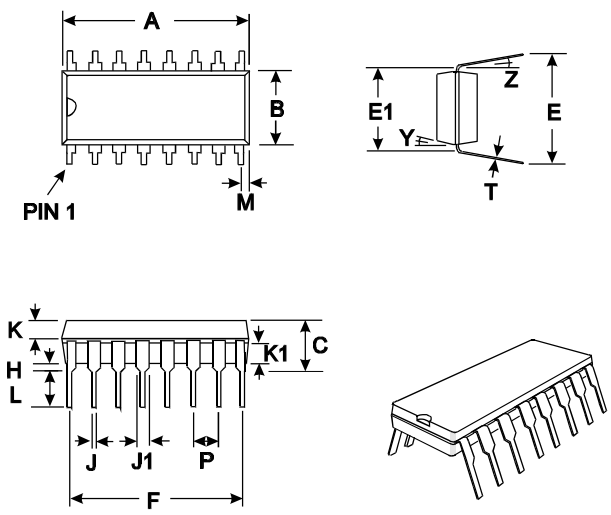
DIM.	MIN.	TYP.	MAX.
* A	0.395 (10.03)		0.413 (10.49)
* B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
F		0.350 (8.89)	
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are In degrees

Figure 7 16-pin SOIC (D4) Mechanical Outline: *Order as part no. CMX654D4*



DIM.	MIN.	TYP.	MAX.
* A	0.740 (18.80)		0.810 (20.57)
* B	0.240 (6.10)		0.262 (6.65)
C	0.135 (3.43)		0.200 (5.08)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
F		0.70 (17.78)	
H	0.015 (0.38)		0.040 (1.02)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
K1	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
M		0.028 (0.71)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		5°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 8 16-pin DIL (P3) Mechanical Outline: *Order as part no. CMX654P3*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

Consumer Microcircuits Limited
M-I-X-E-D S-I-G-N-A-L S-O-L-U-T-I-O-N-S

1 WHEATON ROAD
WITHAM - ESSEX
CM8 3TD - ENGLAND

Telephone: +44 1376 513833
Telefax: +44 1376 518247
e-mail: sales@cmlmicro.co.uk
http://www.cmlmicro.co.uk

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

Company contact information is as below:

CML Microcircuits (UK) Ltd
COMMUNICATION SEMICONDUCTORS

Oval Park, Langford, Maldon,
Essex, CM9 6WG, England
Tel: +44 (0)1621 875500
Fax: +44 (0)1621 875600
uk.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (USA) Inc.
COMMUNICATION SEMICONDUCTORS

4800 Bethania Station Road,
Winston-Salem, NC 27105, USA
Tel: +1 336 744 5050,
0800 638 5577
Fax: +1 336 744 5054
us.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (Singapore) Pte Ltd
COMMUNICATION SEMICONDUCTORS

No 2 Kallang Pudding Road, 09-05/
06 Mactech Industrial Building,
Singapore 349307
Tel: +65 7450426
Fax: +65 7452917
sg.sales@cmlmicro.com
www.cmlmicro.com

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