MX•COM, INC.
COMMUNICATION SEMICONDUCTORS

CMX641A

Dual SPM/Security Detector/Generator

DATA BULLETIN

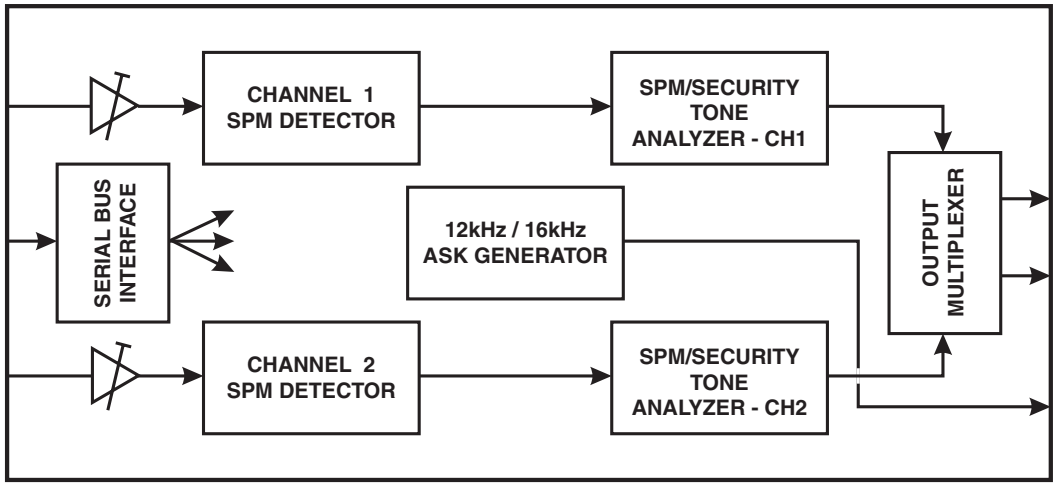
ADVANCE INFORMATION

Features

- **Two (12kHz/16kHz) SPM Detectors**
- **Selectable 12kHz/16kHz ASK Generator**
- **Selectable Tone Follower or Packet Mode 3-State Outputs**
- **Excellent Speech-Band Rejection**
- **Hardwired Control for Non-µC Systems**
- **Selectable Bandwidth Limits and Stable Center Frequency from a Standard Xtal**

Applications

- **SPM for Pair-Gain Systems**
- **Payphone Security Applications**
- **Call Charge Applications in PBX and PABX Line Cards**
- **Out-of-Band Signaling Systems**
- **Low-Voltage FX/MX641 Replacement**
- **µC Software-Programmable Secure Payphone Call Charging Apparatus**



The CMX641A is a low power, system selectable Dual Subscriber Pulse Metering (SPM) Detector – *two detectors on a single chip* – to indicate the presence on a telephone line of either 12kHz or 16kHz telephone call charge frequencies. The detection sensitivity, frequency and bandwidth are independently selectable for each channel, under µC control, as is the frequency of the security tone generator, which may be ASK modulated by an external signal. The CMX641A is also backwards compatible with the FX641 and MX641 dual SPM detectors, while offering a lower (3.0V) operating voltage and power.

The CMX641A has two modes of operation:

1. **Fixed Bandwidth Operating state**, in which the two channels are set to the same system frequency and sensitivity setting. Sensitivity and system frequency can be under either µC or external control. This state is fully pin and function compatible with the FX641 and MX641.
2. **Enhanced Features Operating state**, under µC control, in which each channel has independently controllable sensitivity, bandwidth and system frequency (12kHz or 16kHz). There is also a 12kHz/16kHz transmission tone which can be keyed on and off directly by a dedicated logic pin.

This device is suitable for PBX/PABX line-card installations, payphone security applications and pair-gain systems. It is available in 24-pin plastic DIP and SOIC packages and consumes ≈1.2mA at 3V.

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Note: This product is in development: Changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues.

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1. Block Diagram

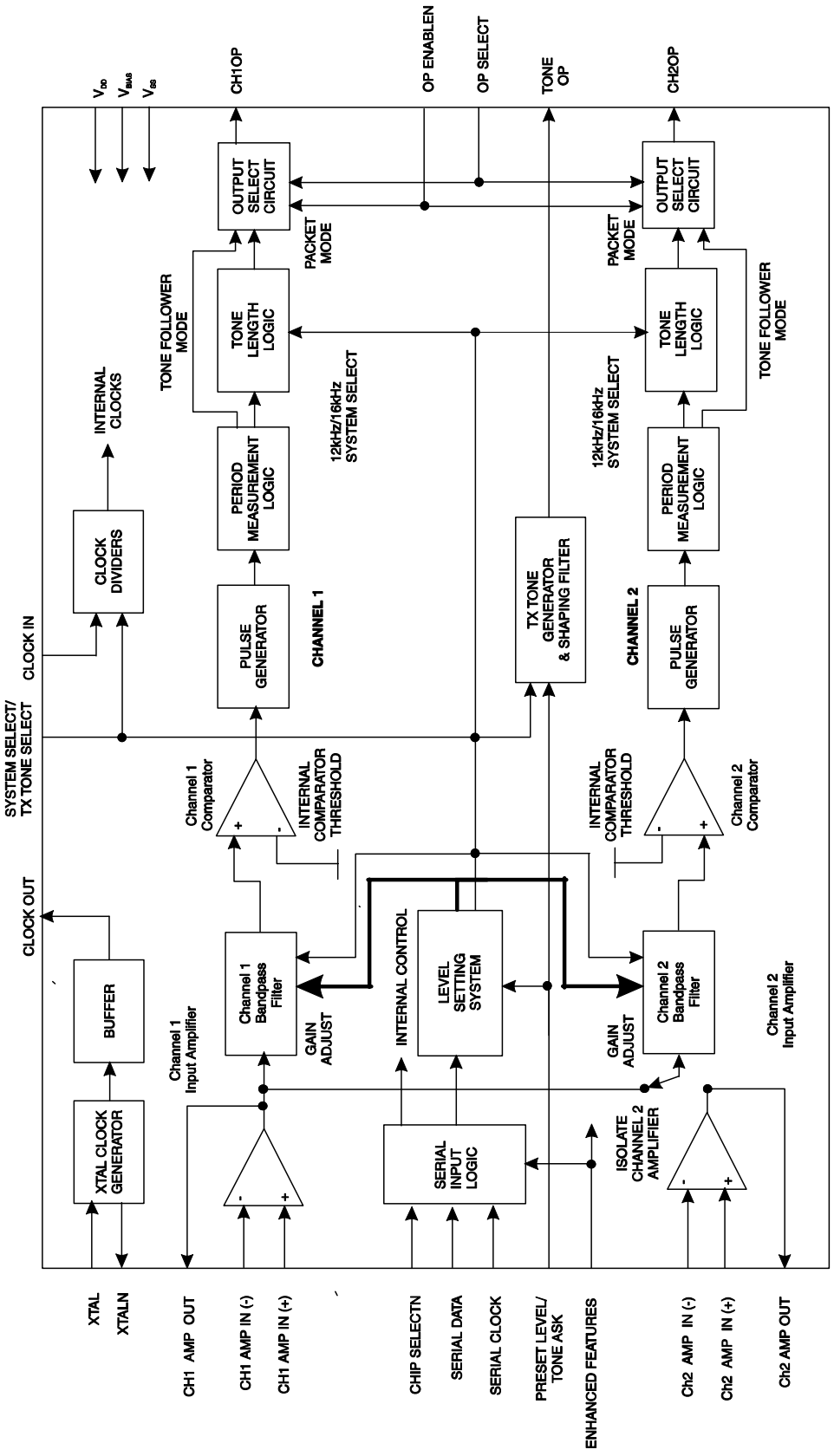

Figure 1: Block Diagram

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2. Signal List

		Signal		Description
D2	**P4**			
Pin No.	**Pin No.**	**Name**	**Type**	
1	1	XTAL	I/P	The input of the on-chip oscillator for use with a 3.579545MHz Xtal in conjunction with the XTALN output; circuit components are on-chip. When using an Xtal input, the CLOCK OUT pin should be connected directly to the CLOCK IN pin. If an external clock input is employed at the CLOCK IN pin, the XTAL pin must be connected directly to V_{DD} (see Figure 2). See Figure 4 for details of clock frequency distribution.
2	2	XTALN	O/P	The inverted output of the on-chip oscillator.
3	3	CLOCK OUT	O/P	The buffered output of the on-chip oscillator inverter. If a XTAL input is employed, this output should be connected directly to the CLOCK IN pin. This output can support up to 3 additional CMX641A microcircuits. See Figure 4 for details of clock distribution.
4	4	CLOCK IN	I/P	The 3.579545MHz input to the internal clock dividers. If an externally generated clock pulse input is employed, XTAL input pin should be connected to V_{DD}.
5	5	OP ENABLEN	I/P	For multi-chip output multiplexing; controls the state of both Ch1 and Ch2 outputs. When this input is placed high (logic '1') both outputs are set to a high impedance. When placed at logic low, both outputs are enabled.
6	6	CH2 OP	O/P	The digital output of the channel 2 SPM detector when enabled. The format of the signal at this pin, in common with CH1 OP is selectable to either 'Tone Follower' or 'Packet mode' via the OP SELECT pin. Logic '0' when tone is detected.
7	7	CH1 OP	O/P	The digital output of the channel 1 SPM detector when enabled. The format of the signal at this pin, in common with CH2 OP is selectable to either 'Tone Follower' or 'Packet mode' via the OP SELECT pin. Logic '0' when tone is detected.
8	8	V_{BIAS}	O/P	A bias line for the internal circuitry, held at ½$V_{DD.}$ This pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
9	9	CH1 AMP OP	O/P	The output of the Channel 1 input amplifier. See Figure 2 and Figure 3.
10	10	CH1 AMP IN (-)	I/P	The negative input to the Channel 1 input amplifier. See Figure 2 and Figure 3.
11	11	CH1 AMP IN (+)	I/P	The positive input to the Channel 1 Input amplifier. See Figure 2 and Figure 3.
12	12	V_{SS}	POWER	The negative supply rail (ground).

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13	13	ENHANCED FEATURES	I/P	This pin selects the device application. When (logic '0') the CMX641A is in Fixed Bandwidth Operating state. When (logic '1') it is in Enhanced Features Operating state. This pin has an internal pulldown resistor on-chip so that when unconnected, the default state is Fixed Bandwidth Operating state.
14	14	CH2 AMP IN (+)	I/P	The positive input to the Channel 2 input amplifier. See Figure 2 and Figure 3.
15	15	CH2 AMP IN (-)	I/P	The negative input to the Channel 2 input amplifier. See Figure 2 and Figure 3.
16	16	CH2 AMP OP	O/P	The output of the Channel 2 input amplifier. See Figure 2 and Figure 3.
17	17	OP SELECT	I/P	A logic input to set the Channel 1 and Channel 2 output format. When high (logic '1'), the outputs are in the Tone Follower mode; when low (logic '0'), the outputs are in Packet mode.
18	18			This is a dual function pin differing between Fixed Bandwidth Operating state and Enhanced Features Operating state. This input has an internal pullup resistor on chip so that the default (open circuit) modes are Fixed Sensitivity (Fixed Bandwidth Operating state) and No Tone (Enhanced Features Operating state).
		PRESET LEVEL		*(Fixed Bandwidth Operating state)*. A logic input to set the sensitivity mode of the CMX641A. When high (logic '1'), both channels are in the Fixed Sensitivity mode. The external components govern the input sensitivity; the SYSTEM SELECT pin selects 12kHz or 16kHz operation. When low logic (logic '0'), the system frequency and sensitivity of both channels are in the Controlled Sensitivity mode. Device sensitivities and system selection are via the CHIP SELECTN/SERIAL DATA/SERIAL CLOCK inputs.
		TONE ASK		*(Enhanced Features Operating state)*. A logic input used to ASK modulate the TONE OP pin. A logic high corresponds to no tone and a logic low to tone.
19	19	CHIPSELECTN	I/P	The serial data pins for use in data loading when using the CMX641A in Controlled Sensitivity mode (Fixed Bandwidth Operating state) or in Enhanced Features Operating state (See Figure 7 and Figure 8). When the device is in Fixed Sensitivity mode (Fixed Bandwidth Operating state), these pins should be connected to V_{SS} or V_{DD}.
20	20	SERIAL CLOCK	I/P	
21	21	SERIAL DATA	I/P	

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22	22			This is a dual function pin differing between Fixed Bandwidth Operating state and Enhanced Features Operating state. This pin has an internal pullup on chip so that the default modes are Detect 12kHz (Fixed Bandwidth Operating state, Fixed Sensitivity mode) or TX Tone = 12kHz (Enhanced Features Operating state).
		SYSTEM SELECT	I/P	*(Fixed Bandwidth Operating state).* In the Fixed Sensitivity mode, this pin selects the system frequency. High (logic '1')=12kHz; Low (logic '0')=16kHz. In the Controlled Sensitivity mode, this pin may be tied to V_{DD} or may be left unconnected. Future functions of this pin, if tied low, are reserved.
		TX TONE SELECT	I/P	*(Enhanced Features Operating state)*. This pin selects 12kHz or 16kHz as the transmit frequency at the TONE OP pin. When high (logic '1'), the Tx tone at the TONE OP pin is 12kHz. When low (logic '0'), the Tx tone is 16kHz.
23	23	TONE OP	O/P	Operates in Enhanced Features Operating state only. A 12kHz or 16kHz transmit tone appears at this pin under the control of the TONE ASK and the TX TONE SELECT pin. In Fixed Bandwidth Operating state, this pin is unused and should be left unconnected.
24	24	V_{DD}	POWER	The positive supply rail. Critical levels and voltages within the CMX641A are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Table 1: Signal List

Notes:

1. SYSTEM SELECT/TX TONE SELECT, ENHANCED FEATURES, and PRESET LEVEL/TONE ASK pins should never be simultaneously driven low - to V_{SS}
2. I/P = Input
3. O/P = Output
4. BI = Bi-directional

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3. External Components

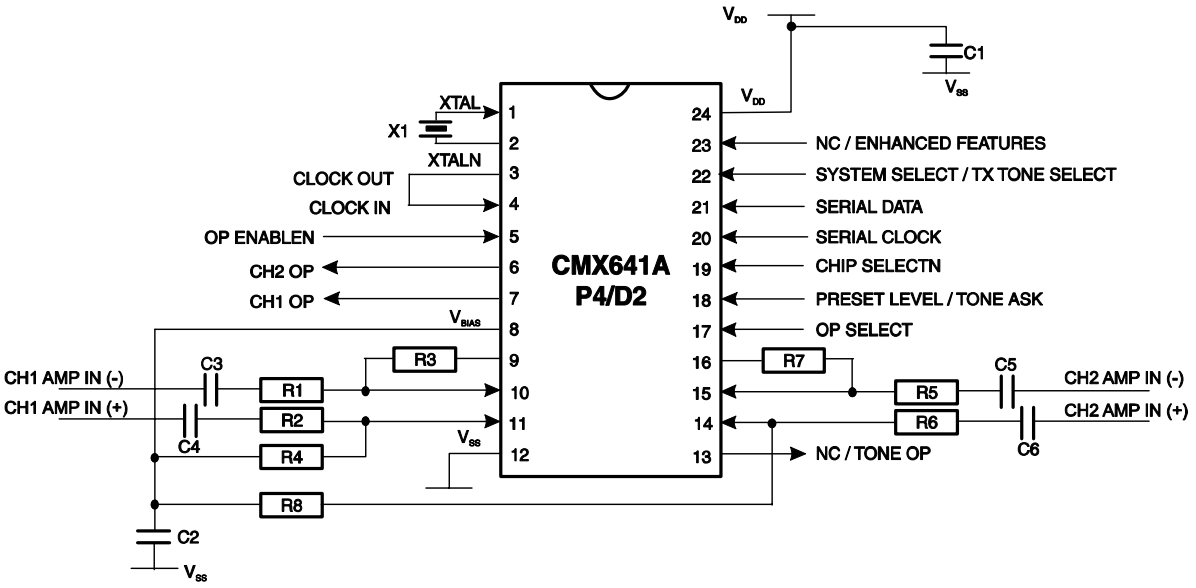

Figure 2: Recommended External Components

Fixed Bandwidth Operating State, *Controlled Sensitivity Mode* and Enhanced Features Operating State

R1	68kΩ	±1%
R2	68kΩ	±1%
R3	750kΩ	±1%
R4	750kΩ	±1%
R5	68kΩ	±1%
R6	68kΩ	±1%
R7	750kΩ	±1%
R8	750kΩ	±1%

C1	1.0µF	±20%
C2	1.0µF	±20%
C3	270pF	±5%
C4	270pF	±5%
C5	270pF	±5%
C6	270pF	±5%
X1	3.579545MHz	

Table 2: Recommended External Components

Fixed Bandwidth Operating State, *Fixed Sensitivity Mode*

In this mode input amplifier components are chosen to set the required sensitivity of the CMX641A. (See section 5.5).

Note: When calculating/selecting gain components, R3, R4, R7 and R8 should always be greater than or equal to 100kΩ.

Particular attention should be paid to decoupling V_{DD} and keeping the power, ground, and signal lines free from unnecessary noise.

Telephone systems may have unusually high DC and AC voltages present on the line, as either differential or common mode signals. If the CMX641A is part of a host system which does not have its own input protection, then protection diodes must be added to both signal inputs (+ and -) so that the voltage on any pin is limited to within V_{SS} – 0.3V and V_{DD} + 0.3V. The breakdown voltage of capacitors and the peak inverse voltage of diodes must be sufficient to withstand the sum of the DC and peak-peak AC voltage applied.

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4. General Description

4.1 Description of Blocks

4.1.1 Crystal Oscillator and Clock Dividers

These circuits derive the internal logic clocks, decode frequencies and transmit frequencies by frequency division of a reference frequency that may be generated by the on-chip crystal oscillator or applied from an external source.

If the on-chip oscillator is used, a 3.579545MHz crystal should be connected across the XTAL and XTALN pins and CLOCK IN pin should be connected to CLOCK OUT. All other oscillator components are on-chip. If an external clock source is used then it should be applied to the CLOCK IN pin and the XTAL pin connected to V_{DD}.

4.1.2 Input Operational Amplifiers

The input signals are input to the CMX641A via these amplifiers. In Controlled Sensitivity mode of the Fixed Bandwidth Operating state, or when in Enhanced Features Operating state, the external components shown in Figure 2 should be used. When used in the Fixed Sensitivity mode of the Fixed Bandwidth Operating state, external gain setting components should be calculated using Figure 6.

In Enhanced Features Operating state, with the channels set to 12kHz/16kHz detect, the channel 2 amplifier can optionally be isolated and may be used as an independent amplifier. In this case, both channels are internally connected to amplifier 1. The amplifiers can be connected as differential mode or single ended, depending upon the application (see Figure 3).

4.1.3 SPM Tone Bandpass Filter

These are tone bandpass/audio reject filters automatically centered on the system frequency (12kHz or 16kHz) being detected. When in Controlled Sensitivity mode of the Fixed Bandwidth Operating state or when in Enhanced Features Operating state, the level sensitivity of the device is set by adjusting the passband gain of these filters. When in Fixed Sensitivity mode of the Fixed Bandwidth Operating state, their gain is constant so that the internal device sensitivity is also constant.

4.1.4 Level Detection and Pulse Generator Circuits

The outputs from the bandpass filters are input to these circuits, which perform the signal level discrimination function for the CMX641A. Signals that fulfill the system level requirements cause a stream of digital pulses, one per 32 cycles of input signal, to be generated. These pulses are sent to the period measurement circuitry.

4.1.5 Period Measurement Logic

This digital circuit block inputs the stream of pulses from the level detection circuits and measures their repetition rate against a predetermined maximum and minimum. Because each pulse from the level detect circuit occur once per 32 cycles of input signal, this has the effect of averaging the input signal period over this number of cycles. A valid SPM tone is recognized when 3 successive correctly spaced pulses are received. If the Tone Follower output format is selected, this causes a signal to appear immediately at the relevant channel output signifying receipt of a valid SPM signal. Depending upon the frequency, within the legal bandwidth, received, the CMX641A should respond within 10-15ms (see section 6 and Figure 5).

4.1.6 Tone Length Logic

This digital circuit block is used when Packet output format is selected. Its output responds when 40ms of valid tone is received within any 48ms window, signifying receipt of a valid packet of SPM tone (see section 6). Once the CMX641A has responded, within any 48ms window, 40ms of no-tone, or of tone outside the chosen bandwidth or below the level threshold will cause the output to derespond. (See Figure 5).

4.1.7 Tx Tone Generator and Shaping Filter

These are active in Enhanced Features Operating state only. They generate a low distortion sinewave for transmission by the CMX641A as an SPM security tone. The output at the TONE OP pin is modulated on-off by the TONE ASK pin. A high (logic ‘1’) selects no tone and low (logic ‘0’) selects tone. The transmission frequency is selected by the TX TONE SELECT pin. A high (logic ‘1’) selects 12kHz and a low (logic ‘0’) selects 16kHz. (See Table 8).

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4.1.8 Output Select Circuits

These drive the output logic pins 'Channel 1 Output' and 'Channel 2 Output'. These outputs can be made high impedance by setting the OP ENABLEN pin high. When enabled, the format at these pins is either Tone Follower or Packet. (See Table 9). A high (logic '1') indicates the tone is absent, a low (logic '0') indicates the tone is present.

4.2 Operating States

There are two operating states for the CMX641A: **Fixed Bandwidth** and **Enhanced Features**.

4.2.1 Fixed Bandwidth Operating State (ENHANCED FEATURES pin = logic '0' or open circuit)

In this operating state, the CMX641A is function and pin compatible with the FX641 and MX641. It is a dual-channel SPM detector with both detectors set to the same level sensitivity and system frequency (12kHz or 16kHz) via a 6-bit serial data word from a host µController. Alternatively, for non µController systems, the sensitivity and system frequency can be set via external components and logic inputs. In this state, the decode bandwidth of both channels is internally fixed at ±1.5% of the nominal center frequency.

4.2.1.1 Fixed Bandwidth Operating State (ENHANCED FEATURES pin = logic '0' or Open Circuit)

This state is selected by leaving pin 23 open circuit. In this state, the CMX641 has full pin, function and software compatibility with the FX641 and MX641. There are two operating modes: ***Controlled*** and ***Fixed Sensitivity***.

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4.2.1.1.1 Controlled Sensitivity Mode (PRESET LEVEL pin = logic '0')

This mode allows the sensitivity to be set from a µController via a 6-bit serial data input. This same serial input also sets operation (bit 0) for either 12kHz or 16kHz systems. Both channels are set identically.

		12kHz System Bit D_0 = '1'			16kHz System Bit D_0 = '0'		
Seria Data Bits D_5-D_1	Bandpass Filter Gain (dB)	Minimum Sensitivity dB(ref.)	Nominal Sensitivity dB(ref.)	Maximum Sensitivity dB(ref.)	Minimum Sensitivity dB(ref.)	Nominal Sensitivity dB(ref.)	Maximum Sensitivity dB(ref.)
00000	0	-16.2	-17.5	-18.8	-16.9	-18.2	-19.5
00001	1.0	-17.2	-18.5	-19.8	-17.9	-19.2	-20.5
00010	2.0	-18.2	-19.5	-20.8	-18.9	-20.2	-21.5
00011	3.0	-19.2	-20.5	-21.8	-19.9	-21.2	-22.5
00100	4.0	-20.2	-21.5	-22.8	-20.9	-22.2	-23.5
00101	5.0	-21.2	-22.5	-23.8	-21.9	-23.2	-24.5
00110	6.0	-22.2	-23.5	-24.8	-22.9	-24.2	-25.5
00111	7.0	-23.2	-24.5	-25.8	-23.9	-25.2	-26.5
01000	8.0	-24.2	-25.5	-26.8	-24.9	-26.2	-27.5
01001	9.0	-25.2	-26.5	-27.8	-25.9	-27.2	-28.5
01010	10.0	-26.2	-27.5	-28.8	-26.9	-28.2	-29.5
01011	11.0	-27.2	-28.5	-29.8	-27.9	-29.2	-30.5
01100	12.0	-28.2	-29.5	-30.8	-28.9	-30.2	-31.5
01101	13.0	-29.2	-30.5	-31.8	-29.9	-31.2	-32.5
01110	14.0	-30.2	-31.5	-32.8	-30.9	-32.2	-33.5
01111	15.0	-31.2	-32.5	-33.8	-31.9	-33.2	-34.5
10000	16.0	-32.2	-33.5	-34.8	-32.9	-34.2	-35.5
10001	17.0	-33.2	-34.5	-35.8	-33.9	-35.2	-36.5
10010	18.0	-34.2	-35.5	-36.8	-34.9	-36.2	-37.5
10011	19.0	-35.2	-36.5	-37.8	-35.9	-37.2	-38.5
10100	20.0	-36.2	-37.5	-38.8	-36.9	-38.2	-39.5
10101	21.0	-37.2	-38.5	-39.8	-37.9	-39.2	-40.5
10110	22.0	-38.2	-39.5	-40.8	-38.9	-40.2	-41.5
10111	23.0	-39.2	-40.5	-41.8	-39.9	-41.2	-42.5
11000	24.0	-40.2	-41.5	-42.8	-40.9	-42.2	-43.5
11001	25.0	-41.2	-42.5	-43.8	-41.9	-43.2	-44.5
11010	26.0	-42.2	-43.5	-44.8	-42.9	-44.2	-45.5
11011	27.0	-43.2	-44.5	-45.8	-43.9	-45.2	-46.5
11100	These states should never be used. If sensitivities of this order are required, (e.g. the Swedish Rural SPM specification, it is recommended that the Controlled sensitivity setting be set to 20dB (10100) and the external components be selected to set the Input Amp gain to a higher figure.						
11101							
11110							
11111							

Table 3: Controlled Sensitivity Setting Information in Fixed Bandwidth Operating State

The figures in Table 3 assume:

The recommended amplifier components (see Figure 2) are employed.

The applied V_{DD} is 5.0V. 0dB(ref.) = 775Vrms.

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Table 3 shows the serial data input to produce the required sensitivity. Minimum, nominal and maximum sensitivity figures are provided to make complete allowance for internal circuit offsets and component tolerances. The gain of each bandpass filter, and therefore the device sensitivity, is adjusted by the applied serial bits D_1 to D_5. The system frequency is selected by bit D_0 ('1' = 12kHz; '0' = 16kHz). Data is loaded bit 5 (D_5) first (See Figure 7).

In controlled sensitivity mode, the 'will detect' bandwidth is internally set at ±1.5% i.e. in 12kHz mode, the CMX641A will detect frequencies between 11.82kHz to 12.18kHz inclusive. In 16kHz mode, it will detect frequencies between 15.76kHz to 16.24kHz inclusive. The 'will not detect' bandedges are ±4% so that, in 12kHz mode, the CMX641A will not respond to frequencies of 11.52kHz or lower or to 12.48kHz or higher. In 16kHz, the equivalent frequencies are 15.36kHz and 16.64kHz.

4.2.1.1.2 Fixed Sensitivity Mode (PRESET LEVEL pin = logic '1' or open circuit)

In this mode, the sensitivity of each channel is set by correct selection of external components around each Channel input amplifier. See section 5.5 and Figure 6 for a method of selecting amplifier gain and components to meet a particular sensitivity requirement.

4.2.2 Enhanced Features Operating State (ENHANCED FEATURES pin = logic '1')

In this state, the following features of the two SPM detector channels are independently controllable via a 16-bit serial data word from a host µController.

i. The decode bandwidths, which can be set to ±1.5%, ±3%, ±5% and ±7.5% of the nominal tone frequency.

ii. The level sensitivity.

iii. The system frequencies, which have one of three possible settings: 12kHz & 12kHz, 16kHz & 16kHz, or 12kHz for Channel 2 and 16kHz for Channel 1.

When the two channels are set to 12kHz/16kHz mode, there is an option to disconnect the channel 2 decode path from its own amplifier and have both channels connected to the channel 1 input. The channel 2 amplifier is then independent and available for some other use, say gain setting or filtering, within the host circuitry.

There is also a transmit tone, selectable to 12kHz or 16kHz, which is ASK modulated via a logic input pin.

4.2.2.1 Enhanced Features Operating State (ENHANCED FEATURES pin = logic '1')

This state is selected by tying pin 23 to logic 1. It has individually programmable tone detect bandwidths, signal sensitivities and a 12kHz or 16kHz ASK keyed transmission tone. Control of the CMX641A in this state is via a 16-bit serial data word, as shown in Table 4. Data is loaded bit 15 (D15) first (See Figure 8).

Channel 2		Channel 1		System Select
D15-D11	D10-D9	D8-D4	D3-D2	D1-D0
Level Sensitivity set as in Table 3 above	Bandwidth Control	Level Sensitivity set as in Table 3 above	Bandwidth Control	12kHz or 16kHz Select

Table 4: 16-Bit Serial Input Word in Enhanced Features Operating State

4.2.2.1.1 Channel Level Sensitivities

These are independently programmable via bits D15-D11 for channel 2 and bits D8-D4 for channel 1. The 5-bit coding and sensitivities are as given in Table 3 above for the Fixed Bandwidth Operating State. For example, if D15-D11 = '01001' and D8-D4 = '00101', both in 12kHz mode, then channel 2 would have a nominal sensitivity of –26.5dB(ref) and channel 1 would have a nominal sensitivity of –22.5dB(ref).

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4.2.2.1.2 Will Detect and Will Not Detect Bandwidths

There are four individually programmable bandwidths per channel. The 'will detect' bandwidth can be programmed to ±1.5%, ±3%, ±5% or ±7%. The corresponding 'will not detect' band edges are ±4%, ±5.5%, ±7.5% and ±10%. Bits D10 and D9 control channel 2 and bits D3 and D2 control channel 1.

D10-D9 (Channel 2) D3-D2 (Channel 1)	Lower Will Not Detect	Lower Will Detect	Upper Will Detect	Upper Will Not Detect
00	11.52kHz (-4%)	11.82kHz (-1.5%)	12.18kHz (+1.5%)	12.48kHz (+4%)
01	11.34kHz (-5.5%)	11.64kHz (-3.0%)	12.36kHz (+3.0%)	12.66kHz (+5.5%)
10	11.10kHz (-7.5%)	11.40kHz (-5.0%)	12.60kHz (+5.0%)	12.90kHz (+7.5%)
11	10.80kHz (-10.0%)	11.10kHz (-7.5%)	12.90kHz (+7.5%)	13.20kHz (+10.0%)

Table 5: Setting 12kHz Will Detect/Will Not Detect Bandwidths in Enhanced Features Operating State

D10-D9 (Channel 2) D3-D2 (Channel 1)	Lower Will Not Detect	Lower Will Detect	Upper Will Detect	Upper Will Not Detect
00	15.36kHz (-4.0%)	15.76kHz (-1.5%)	16.24kHz (+1.5%)	16.64kHz (+4.0%)
01	15.12kHz (-5.5%)	15.52kHz (-3.0%)	16.48kHz (+3.0%)	16.88kHz (+5.5%)
10	14.80kHz (-7.5%)	15.20kHz (-5.0%)	16.80kHz (+5.0%)	17.20kHz (+7.5%)
11	14.40kHz (-10.0%)	14.80kHz (-7.5%)	17.20kHz (+7.5%)	17.60kHz (+10.0%)

Table 6: Setting 16kHz Will Detect/Will Not Detect Bandwidths in Enhanced Features Operating State

The CMX641A will always respond to valid inputs between the Lower 'Will Detect' and Upper 'Will Detect' frequencies inclusive. It will not respond to frequencies at or below the Lower 'Will Not Detect' or at or above the Upper 'Will Not Detect'. The response and deresponse times will depend upon the output format chosen, i.e. Tone Follower or Packet output.

4.2.2.1.3 System Select

Bits D1 and D0 select the operating frequencies of the CMX641A in Enhanced Features Operating State.

D1-D0	Channel 1 Output	Channel 2 Output	Amp 1	Amp 2
00	Detects 16kHz	Detects 16kHz	Input to channel 1	Input to channel 2
01	Detects 16kHz	Detects 12kHz	Input to channel 1	Input to channel 2
10	Detects 16kHz	Detects 12kHz	Input to channel 1 & 2	Available as independent amplifier
11	Detects 12kHz	Detects 12kHz	Input to channel 1	Input to channel 2

Table 7: Setting System Frequencies in Enhanced Features Operating State

The operating frequencies can be set in four ways as shown in Table 7. In three of the four cases, Amplifier 1 is the input to channel 1 and Amplifier 2 is the input to channel 2. However, when bits D1-D0=10, both channels take their input from Amplifier 1. This makes Amplifier 2 available for independent use, perhaps as a gain or filter block.

However it should be noted that each channel will detect its system frequency only in the absence of the other. The device is not designed to be immune to the presence of the other tone. Each channel will function correctly when either 12kHz or 16kHz, but not both, is present.

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4.2.2.1.4 ASK Tone Output

This is output from the TONE OP pin under the control of the TONE ASK input and the TX TONE SELECT pins. The TONE ASK pin keys the transmit tone on-off. A logic high corresponds to no tone and logic low to tone. The output frequency is selected by the TX TONE SELECT pin. A logic high selects 12kHz and logic low selects 16kHz. (See Table 8). The tone output is ramped up to its maximum level and down to nil output with time constants of TBD and TBD respectively.

TONE ASK	TX TONE SELECT	TONE OP
0	0	16kHz
0	1	12kHz
1	X	BIAS

Table 8: Selecting Transmission Tone in Enhanced Features Mode

4.2.3 Features Common to both Operating States

In both states, three output formats are available for the channel output pins. These output formats are selectable via the logic input pins OP SELECT and OP ENABLEN. (See Table 8).

i. In Tone Follower mode, the logic output has very short response and deresponse times so that it forms an 'envelope' of the input tone. Host systems will decide whether the received signal fulfils the system tone pulse length requirements.

ii. In Packet mode, the channel output only responds after 40ms of received continuous tone. The CMX641A then ignores the erroneous 20ms on, 20ms off "ringing" pattern which occurs on some telephone lines.

iii. The deresponse time is also 40ms, so that the decode output pin forms a delayed envelope of the input tone and host systems can decide, as in the Tone Follower mode, whether the received tone duration fulfils local system requirements.

iv. The outputs can be set to a high impedance state for device multiplexing.

OP ENABLEN	OP SELECT	CH1 & CH2 OP FORMAT
0	0	Packet Mode
0	1	Tone Follower Mode
1	X	High Z

Table 9: Selection of Output Format via OP ENABLEN and OP SELECT pins

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5. Application Notes

5.1 Signal Input Configurations

Figure 3 shows how the input amplifiers can be connected as differential mode or common mode amplifiers, according to the application.

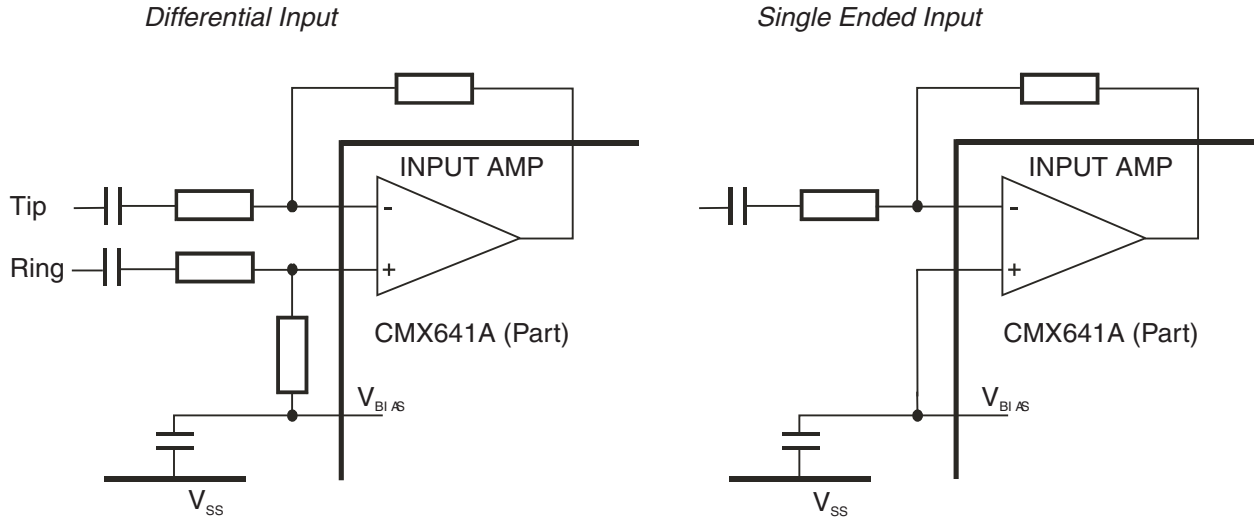

Figure 3: Example Input Configurations

5.2 Crystal/Clock Distribution

The CMX641A requires a 3.579545MHz crystal or an external clock pulse input. With the exception of the crystal, all oscillator components are incorporated on chip. If a crystal is employed, the Clock Out pin should be connected directly to the Clock In pin.

To reduce component and layout complexity the clock requirements of up to 3 additional CMX641A microcircuits may be supplied from a crystal driven CMX641A acting as the master system clock. With reference to Figure 4, the clock should be distributed as illustrated and the XTAL pins of the driven devices should be connected directly to V_{DD}.

Note that the maximum load on the master Clock Out pin should not be exceeded.

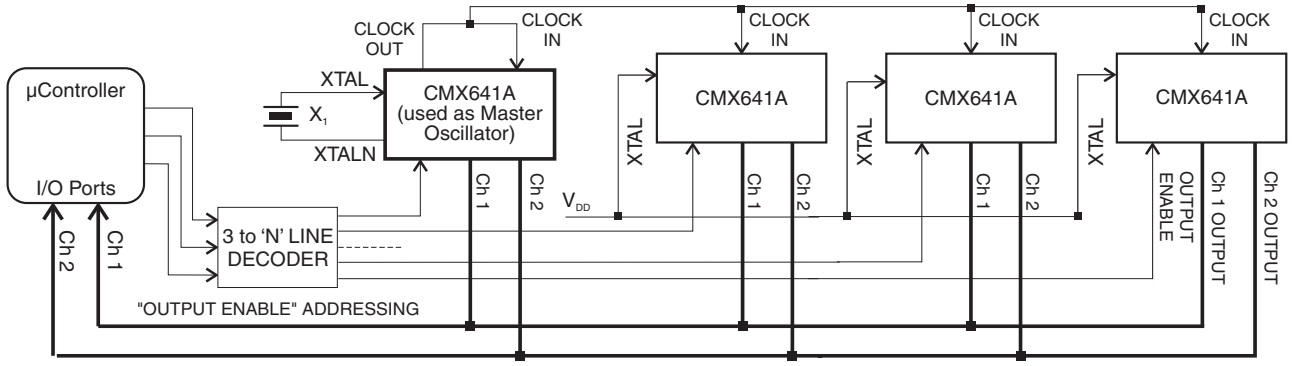

Figure 4: Example of Clock Distribution and 8-Channel Output Multiplexing

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5.3 Channel 1 and Channel 2 Output Format

Figure 5 illustrates the two output formats: Tone Follower mode and Packet mode.

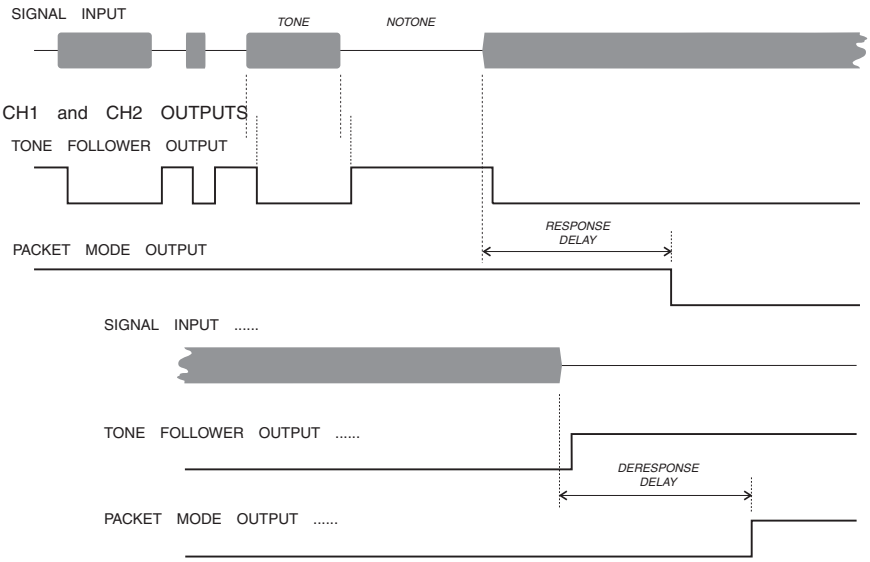

Figure 5: Tone Follower and Packet Mode Outputs

5.4 Setting Level Sensitivity via the Input Serial Data Word

The serial data word input is used to set the device sensitivity in the Controlled Sensitivity mode of the Fixed Bandwidth Operating state and in the Enhanced Features Operating state.

In Controlled Sensitivity mode of the Fixed Bandwidth Operating state, the CMX641A operates identically to the FX641 and MX641. The input word is 6 bits and Table 3 lists the device sensitivities vs input codes.

In the Enhanced Features Operating State, channel 1's sensitivity is controlled by applying the codes in Table 3 to bits D15-D11. Channel 2's sensitivity is controlled by applying these codes to bits D8-D4.

Example: Suppose the CMX641A is required to work in a system in which 16kHz signals, at or above –22dB(ref) must be detected and signals at or below –27dB(ref) must not be detected. Reference to Table 3 shows that bandpass filter gain settings of 6dB or 7dB will meet this level specification.

Thus in Fixed Bandwidth Operating State and Controlled Sensitivity Mode:

Inputting D5-D0 = '001100' or '001110' (See Table 3) will set both channels to meet this specification. Selecting '001100' makes both channels' minimum 'Will Detect' level –22.9dB(ref) and its maximum 'Will Not Detect' level –25.5dB(ref). This means that the detection threshold of any device will lie between these two levels.

In Enhanced Features Operating State *Channel 2:*

Inputting D15-D11 = '00110' or '00111' (See Table 3 and Table 4) and D1-D0 = '00' (See Table 7) will program channel 2 to meet this level specification. Selecting '00111' makes the channel 2 minimum 'Will Detect' level –23.9dB(ref) and its maximum 'Will Not Detect' level –26.5dB(ref). This means that Channel 2's detection threshold will lie between these two levels.

In Enhanced Features Operating State *Channel 1:*

Inputting D8-D4 = '00110' or '00111' (See Table 3 and Table 4) and D1-D0 = '00', '01' or '10' (See Table 7) will program channel 1 to meet this level specification. Selecting '00110' makes the CMX641A minimum 'Will Detect' level –22.9dB(ref) and its maximum 'Will Not Detect' level –25.5dB(ref). This means that channel 1's detection threshold will lie between these two levels. The two channels may be set to identical detection thresholds, if desired.

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5.5 Setting Level Sensitivity via External Components

In Fixed Bandwidth Operating state, Fixed Sensitivity mode, the sensitivities of the two channels are set by the correct selection of the components around the Channel Input Amplifiers.

Input Gain Calculation: The input amplifiers, with their external circuitry, are available to set the sensitivity of the CMX641A to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels. With reference to the graph in Figure 6, the following steps will assist in the determination of the required gain/attenuation.

Step 1

Draw two horizontal lines from the Y-axis {Signal Level dB(ref)}

The upper line will represent the required 'Must' decode level

The lower line will represent the required 'Must-Not' decode level.

Step 2

Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis {Amplifier Gain (dB)}.

The point where the vertical line meets the X-axis will indicate the MINIMUM Input gain required for reliable decoding of valid signals.

Step 3

Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis.

The point where the vertical line meets the X-axis will indicate the MAXIMUM allowable Input amp gain. Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.

Step 4

Refer to the gain components shown in Figure 2. The user should calculate and select external components (R1/R3/C3, R2/R4/C4 and R5/R7/C5, R6/R8/C6) to provide amplifier gains within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain figure outside these limits. Resistors R3, R4, R7 and R8 should always be greater than or equal to 100kΩ. It is recommended that the designed gain is near the center of the calculated range.

Note that the device sensitivity is directly proportional to the applied power supply (V_{DD}). The graph in Figure 6 is for the calculation of input gain components for the CMX641A using a V_{DD} of 5.0 (±0.1) volts.

Subtract 4.44dB from the amplifier gain for operation at 3.0V volts.

5.6 Aliasing

Due to the switched capacitor filters employed in the CMX641A, care should be taken to avoid any aliasing effects by removing all frequencies above 579.390kHz (16kHz mode) or 434.543kHz (12kHz mode). This can be achieved by adding bypass capacitors across R3, R4, R7, and R8, setting the –3dB breakpoint of each resistor-capacitor combination such that there is sufficient attenuation at the alias frequency and negligible effect at the desired SPM frequency.

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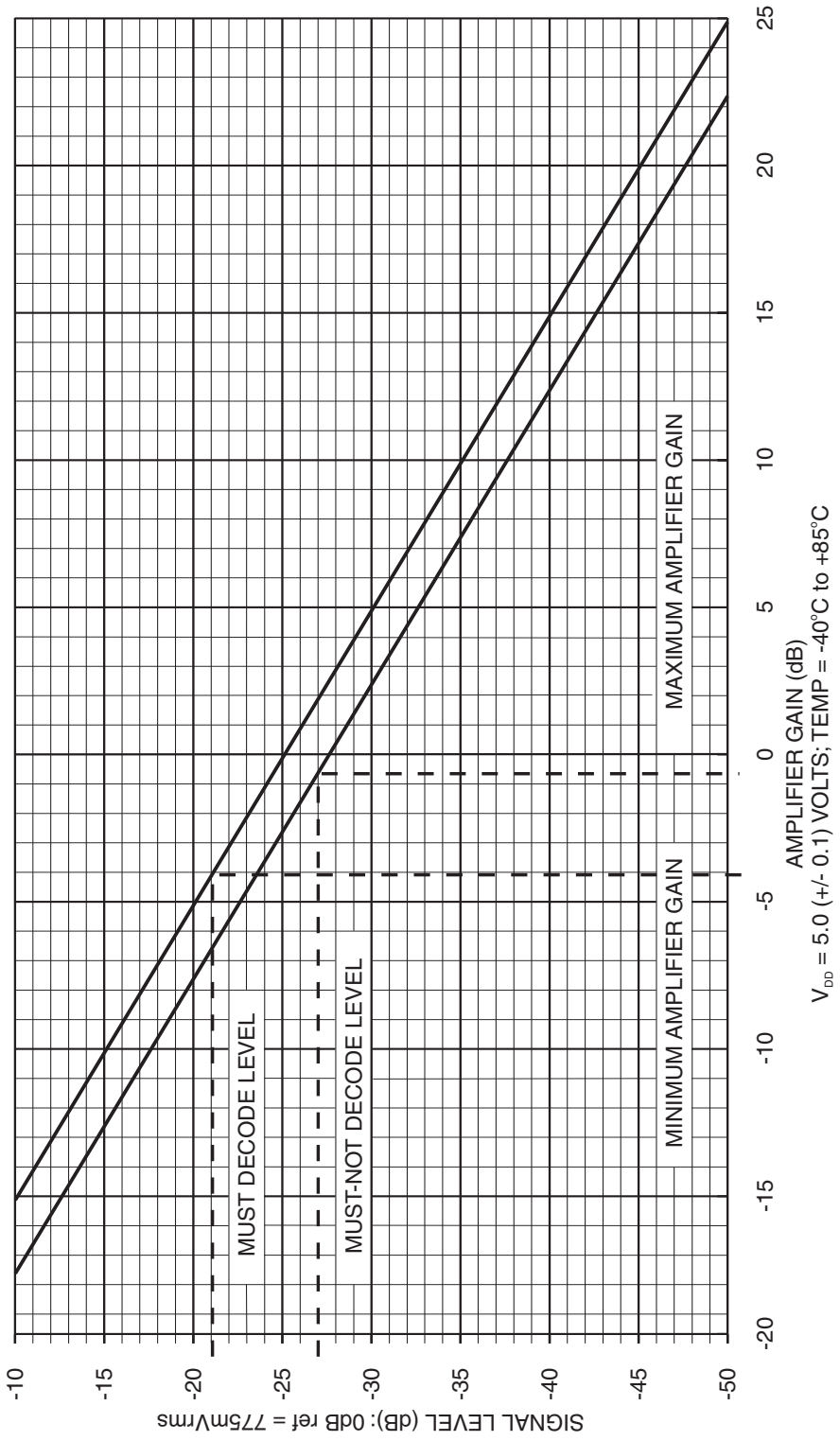

Figure 6: Input Gain Calculation Graph for use in the Fixed Sensitivity Mode of the Fixed Bandwidth Operating State

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6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA
D2/P4 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		-40	+85	°C
Xtal Frequency		3.558918	3.589368	MHz

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6.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, Audio Level 0dB(ref) = 775Vrms. Noise Bandwidth = 50kHz,

V_{DD} = 3.0V to 5.5V, Tamb = - 40°C to +85°C. System Setting = 12kHz or 16kHz.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1		2.0	5.0	mA
	2		1.2	3.0	mA
Input/Output Parameters					
Clock Out Load				15	pF
Logic Inputs					
Input logic “1” level		80%			V_{DD}
Input logic “0” level				20%	V_{DD}
Input leakage current (Vin = 0 to V_{DD})	3	-5.0		+5.0	µA
Input capacitance			7.5		pF
Input current (Vin =0)	4	-15.0			µA
Channel Outputs					
Output logic “1” level (1_{OH} = 120µA) (Enabled)	5	90%			V_{DD}
Output logic “0” level (1_{OL} = 360µA) (Enabled)	5			10%	V_{DD}
Off state leakage current (High Z output)	6	-5.0		5.0	µA
Mode Change Time				500	ms
Tone Follower Mode					
Response and De-Response time	8,9,10			15.0	ms
Packet Mode					
Response and De-Response time	8,9,10	40.0		48.0	ms
Input Amplifiers					
Input impedance (at 100Hz)		10.0			MΩ
Open Loop voltage gain (I/P = 1mVrms at 100Hz)			500		V/V
Common Mode Range		10%		90%	V_{DD}
Input Signal Level				100%	V_{DD}
Output Impedance (Open Loop)			6.0		kΩ

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	Notes	Min.	Typ.	Max.	Units
Overall Performance					
12kHz Detect Bandwidth	8,11	11.82		12.18	kHz
12kHz Detect Bandwidth	8,12	11.64		12.36	kHz
12kHz Detect Bandwidth	8,13	11.40		12.60	kHz
12kHz Detect Bandwidth	8,14	11.10		12.90	kHz
12kHz Not Detect Frequencies (below 12kHz)	8,11			11.52	kHz
12kHz Not Detect Frequencies (below 12kHz)	8,12			11.34	kHz
12kHz Not Detect Frequencies (below 12kHz)	8,13			11.10	kHz
12kHz Not Detect Frequencies (below 12kHz)	8,14			10.80	kHz
12kHz Not Detect Frequencies (above 12kHz)	8,11	12.48			kHz
12kHz Not Detect Frequencies (above 12kHz)	8,12	12.66			kHz
12kHz Not Detect Frequencies (above12kHz)	8,13	12.90			kHz
12kHz Not Detect Frequencies (above12kHz)	8,14	13.20			kHz
16kHz Detect Bandwidth	8,11	15.76		16.24	kHz
16kHz Detect Bandwidth	8,12	15.52		16.48	KHz
16kHz Detect Bandwidth	8,13	15.20		16.80	kHz
16kHz Detect Bandwidth	8,14	14.80		17.20	kHz
16kHz Not-Detect Frequencies (below 16kHz)	8,11			15.36	kHz
16kHz Not-Detect Frequencies (below 16kHz)	8,12			15.12	kHz
16kHz Not-Detect Frequencies (below 16kHz)	8,13			14.80	kHz
16kHz Not Detect Frequencies (below 16kHz)	8,14			14.40	kHz
16kHz Not-Detect Frequencies (above 16kHz)	8,11	16.64			kHz
16kHz Not-Detect Frequencies (above 16kHz)	8,12	16.88			kHz
12kHz Not-Detect Frequencies (above 12kHz)	8,13	17.20			kHz
12kHz Not-Detect Frequencies (above 12kHz)	8,14	17.60			kHz
Level Sensitivity					kHz
Level Sensitivity set by input serial data	8,9, 15,16	2.6	1.6	0.6	dB
Level Sensitivity set by external components	1,8,9, 17,18	-25.4	-26.4	-27.4	dB
Signal Quality Requirements for Correct Operation					
Signal to Noise Ratio (Amp input)	9,19, 20,21	22.0	20.0		dB
Signal to Voice Ratio (Amp input)	9,19, 20,22	-36.0	-40.0		dB
Signal to Voice Ratio (Amp output)	9,19, 21,22	-1.0		-27.0	dB
Tx Output					
Output Impedance	27		1.0	2.5	kΩ
Output Frequency	23	11.94		12.6	kHz
Output Frequency	24	15.92		16.80	kHz
Signal Level	1	3.0	3.4	3.7	Vp-p
Output Distortion				2	%
Response/De-response Times	23,25			100	µs
	24, 25			80	µs
Rise/Fall Times	23,26		500	600	µs
	24,26		400	500	µs

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Notes:

1. At 5.0V. Not including any current drawn from the pins by external circuitry.
2. At 3.0V. Not including any current drawn from the pins by external circuitry.
3. Logic pins with no internal pull-up or pull-down resistors; CHIP SELECTN, SERIAL DATA, SERIAL CLOCK, OP ENABLEN, OP SELECT and CLOCK IN pins.
4. Logic pins with an internal pull-up or pull-down resistor; PRESET LEVEL/TONE ASK, SYSTEM SELECT/TX TONE SELECT, ENHANCED FEATURES.
5. Tone Follower or Packet Mode enabled.
6. Tristate selected.
7. Time taken to change between any two of the operational modes: Tone follower, Packet or Tristate, and with a maximum capacitive load of 30pF on an output.
8. With adherence to Signal to Voice and Signal to Noise specifications.
9. 12kHz and/or 16kHz system.
10. The time delay after a valid serial data load (or after device powerup, change of bandwidth setting or change in input signal conditions), before the condition of the outputs can be guaranteed correct.
11. With 'Will Detect' bandwidth set to ±1.5%, Fixed Bandwidth Operating State or Enhanced Features Operating State.
12. With 'Will Detect' bandwidth set to ±3.0%, Enhanced Features Operating State only.
13. With 'Will Detect' bandwidth set to ±5.0%, Enhanced Features Operating State only.
14. With 'Will Detect' bandwidth set to ±7.5%, Enhanced Features Operating State only.
15. With the input amplifier gain at 0dB and the Bandpass filter gain set to 0dB (Table 3); subtract 1dB from this specification for each single dB of Bandpass filter gain programmed.
    Alternatively, with the input components as recommended in Figure 2, the sensitivity is as defined in Table 3.
16. In Fixed Bandwidth Operating State, Controlled Sensitivity mode; or in Enhanced Features Operating State.
17. In Fixed Bandwidth Operating State, Preset Sensitivity Mode.
18. With input amplifier gain setting 0dB via external components and measured at amplifier output with V_{DD} = 5.0V. Signal sensitivity is proportional to V_{DD}.
19. For immunity to false responses and/or deresponses.
20. Common mode SPM and balanced voice signal.
21. With SPM and voice signal balanced; to avoid false deresponses due to saturation, the peak to peak voice + noise level at the output of the input amplifier should be no greater than the dynamic range of the device. For this reason, the signal to voice figure at the Amp output will vary with the sensitivity setting. The lowest signal to voice figure occurs at the highest sensitivity setting (Table 3, 27dB).
22. Maximum voice frequencies = 3.4kHz.
23. Output tone = 12kHz selected.
24. Output tone = 16kHz selected.
25. The time between a logic '1-0' transition at TONE ASK input and the tone at TONE OP reaching 10% of its full value or between a '0-1' transition at TONE ASK input and the tone falling to 90% of its full value.
26. The time for the tone at TONE OP to rise from 10% to 90% or to fall from 90% to 10% of its full value.
27. Tx circuit enabled in Enhanced Features Operating State.

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6.1.4 Timing

Parameter		Min.	Typ.	Max.	Units
t_{PWH}	Serial Clock 'High' Pulse Width	250	-	-	ns
t_{PWL}	Serial Clock 'Low' Pulse Width	250	-	-	ns
t_{CYC}	Serial Clock Period	600	-	-	ns
t_{CSE}	Chip Select 'Low' to Clock 'High' Edge	450	-	-	ns
t_{DH}	Data Hold Time	50.0	-	-	ns
t_{DS}	Data Setup Time	250	-	-	ns
t_{CSH}	Chip Select 'High' from:				
	Clock 'High' Edge	50.0	-	-	ns
	Clock 'High' Edge	-	-	1	Serial clock period

Table 10: Data Load Timing

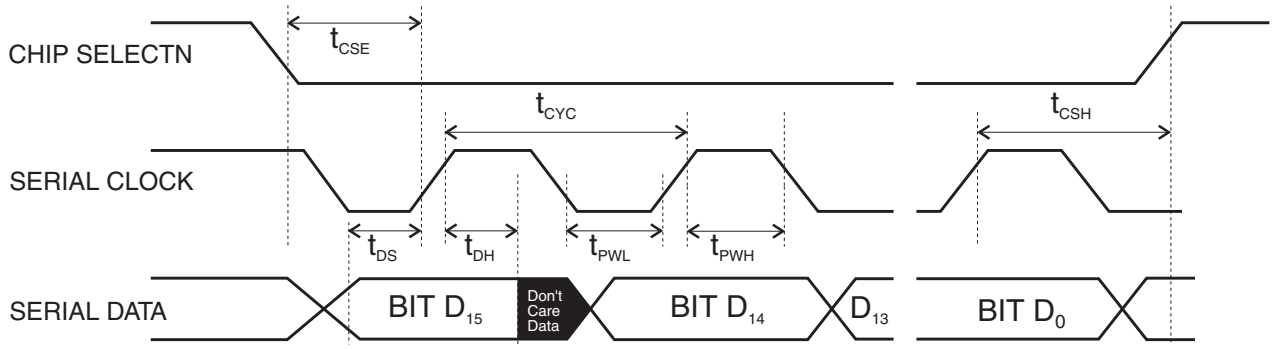

Figure 7: Data Load Timing for the Fixed Bandwidth Operating Style, Controlled Sensitivity Mode

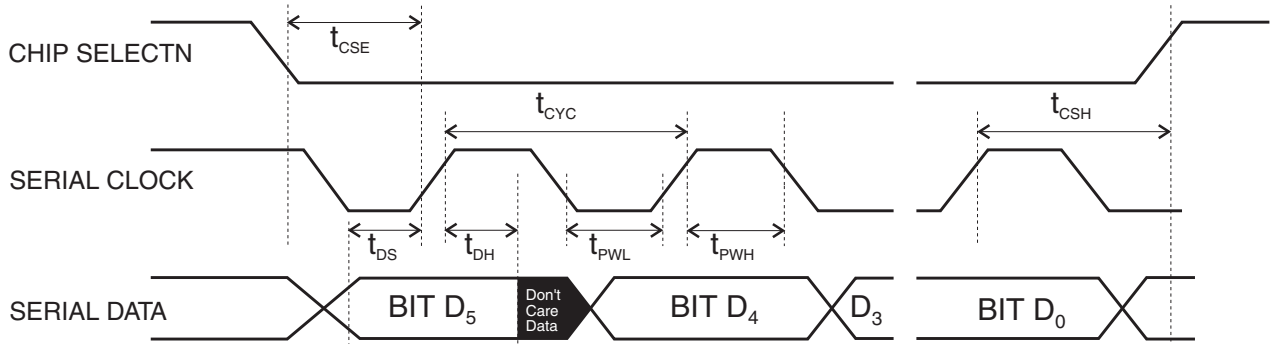

Figure 8: Data Load Timing for Enhanced Features Operating State

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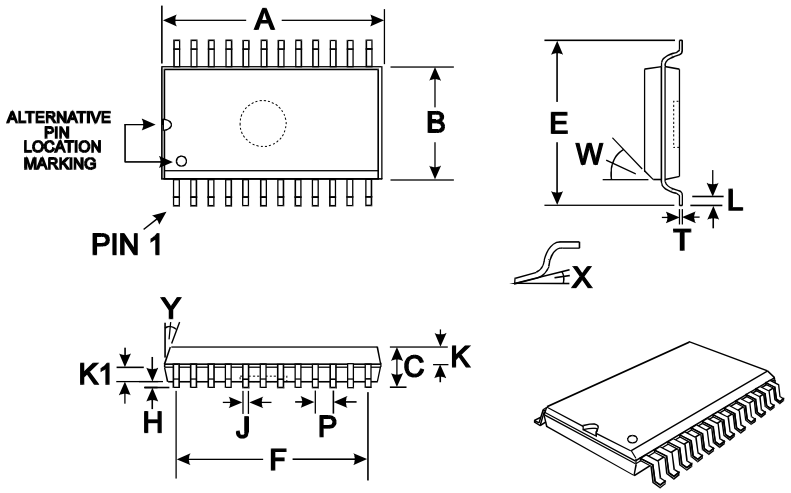
6.2 Packaging



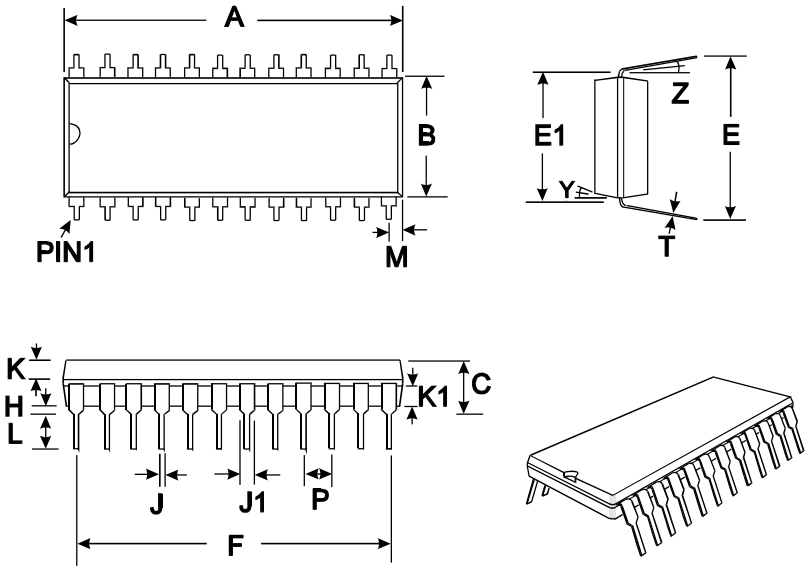
DIM.	MIN.	TYP.	MAX.
* A	0.597 (15.16)		0.613 (15.57)
* B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
F		0.550 (14.1)	
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 24-pin SOIC (D2) Mechanical Outline: *Order as part . CMX641AD2*



DIM.	MIN.	TYP.	MAX.
* A	1.200 (30.48)		1.270 (32.26)
* B	0.500 (12.70)		0.555 (14.10)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.06)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin PDIP (P4) Mechanical Outline: *Order as part no. CMX641AP4*

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