PROCESS CP314V

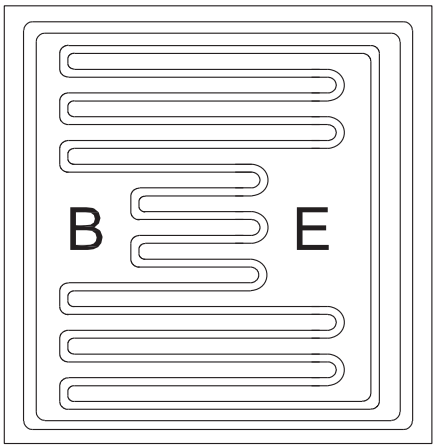
Small Signal Transistor

NPN - High Current Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	40 x 40 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	7.9 x 8.7 MILS
Emitter Bonding Pad Area	9.0 x 14 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au-As - 13,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 5 INCH WAFER

10,583

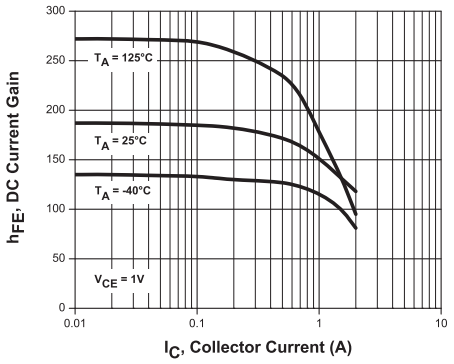
PRINCIPAL DEVICE TYPES

CBCP68
CBCX68
CMPT651
CZT651
MPS650
MPS651

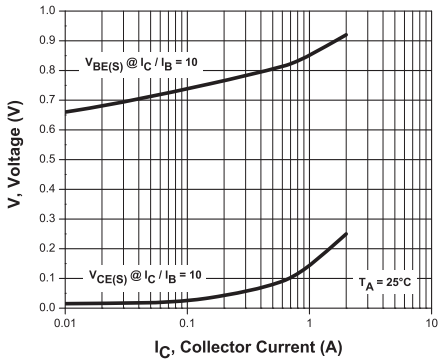
PROCESS CP314V

Typical Electrical Characteristics

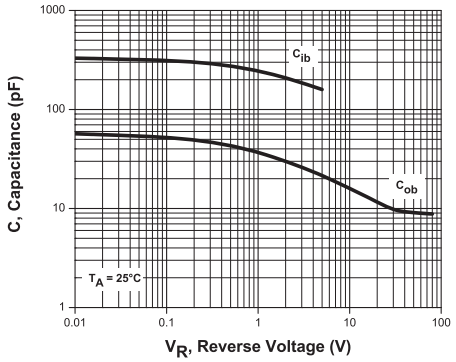
DC Current Gain



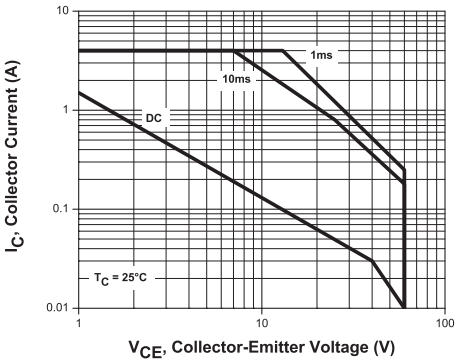
"ON" Voltage



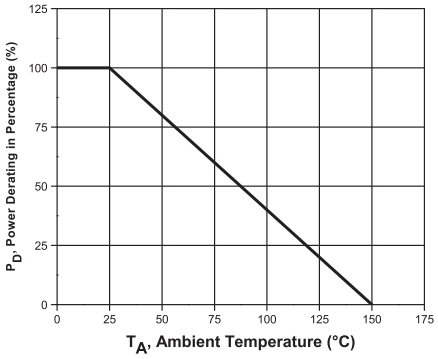
Capacitance



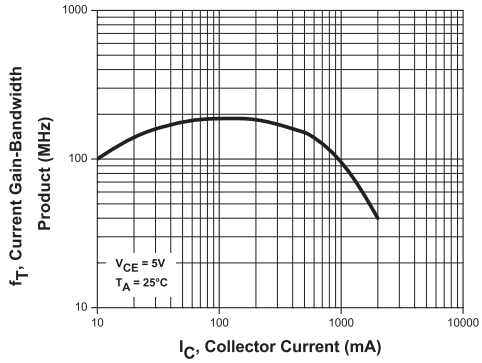
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



R1 (22-March 2010)