CLEAR LOGIC

CL3128A

Laser Processed Logic Device Family

Key Features

- Laser Processed Logic Device (LPLD™) technology offers the ultimate combination of performance, flexibility, and low cost
- Functionally, architecturally, and electrically compatible with industry-standard Altera® MAX® 3000
- High Density
  - 2,500 Usable gates
  - 128 Macrocells
  - 96 Maximum user I/O pins
- Laser fuse technology provides very fast, dense interconnect routing
- Low current consumption
- Supports 3.3 volt operation
- Alpha particle immune

CL3000 Product Family Overview

Feature	CL3128A	CL3256A
Useable Gates	2,500	5,000
Macrocells	128	256
Logic array Blocks	8	16
Max user I/O pins	96	158
Speed Grades	-4, -5, -7, -10	-5, -6, -7, -10
Packages	100-Pin TQFP 144-Pin TQFP	144-Pin TQFP 208-Pin PQFP

3KA tbl 01A

Description

The Clear Logic CL3000 Laser Processed Logic Device (LPLD®) family offers the ultimate combination of performance, flexibility, and cost. This family is a system level second source to Altera MAX® 3000A products. For designs not requiring in-system reprogrammability, design verification can be performed using the programmable Altera devices, and Clear Logic LPLDs can be used for low cost, high volume production.

Clear Logic's innovative laser-based technology eliminates NRE costs, test vector development, ordering minimums and long lead times. No re-simulation or re-layout is required, as the device uses a cell-based, PLD-like architecture. Clear Logic's NoFault® technology ensures complete test coverage through the use of specialized testing modes which are transparent to the user.

The Clear Logic CL3000 Laser Processed Logic Device family is based upon a large array of macrocells. Each macrocell contains a logic array with five product terms, a product-term select matrix, and a configurable register. A group of sixteen macrocells forms a block. Laser-configured metal fuses implement logical functions and control signal routing.

Laser configuration provides reduced cost and enhanced performance. These inherent performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

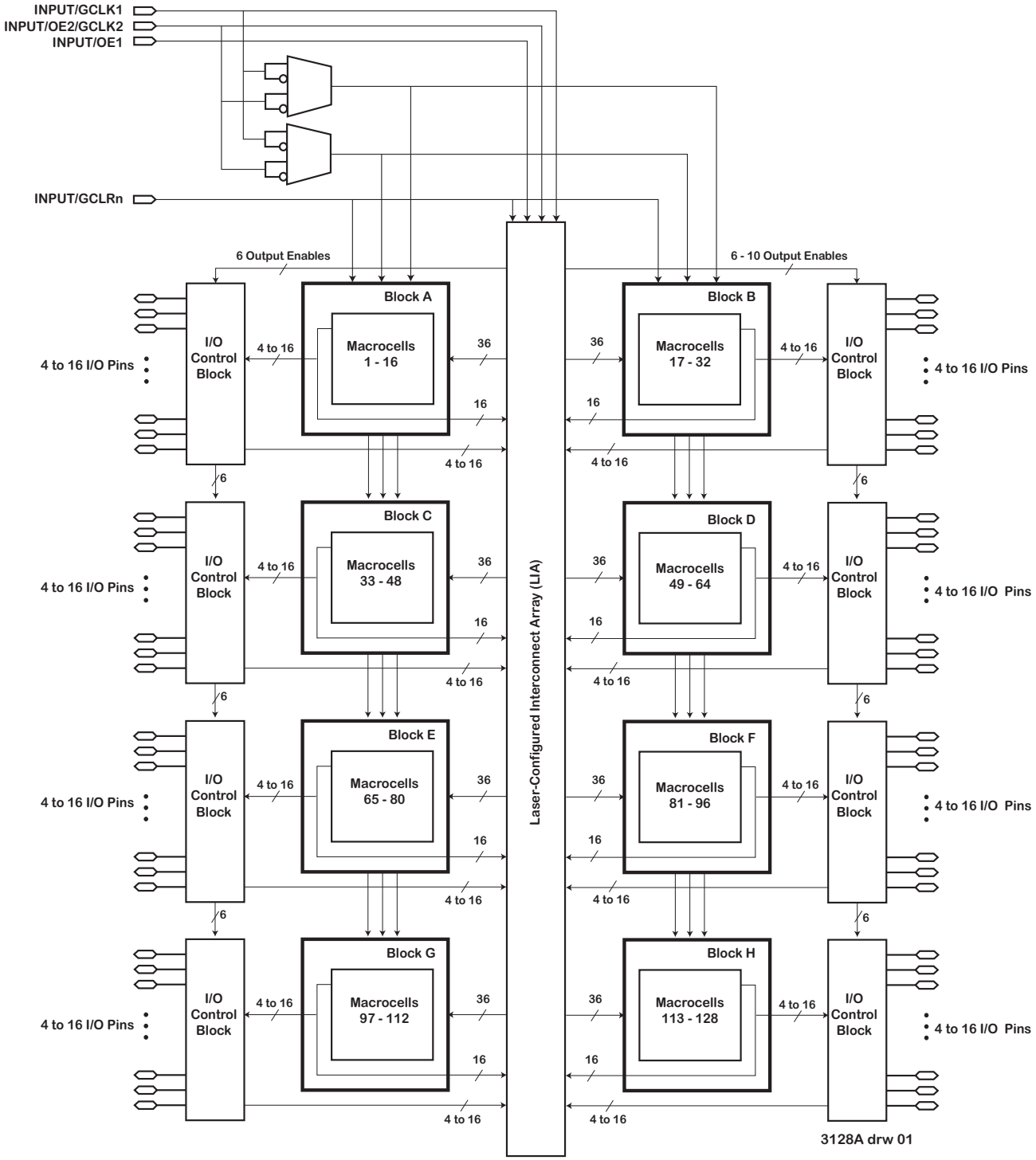
Additional Information

For further information on designing with the CL3000 LPLD family (See CL7000), please consult the following documents:

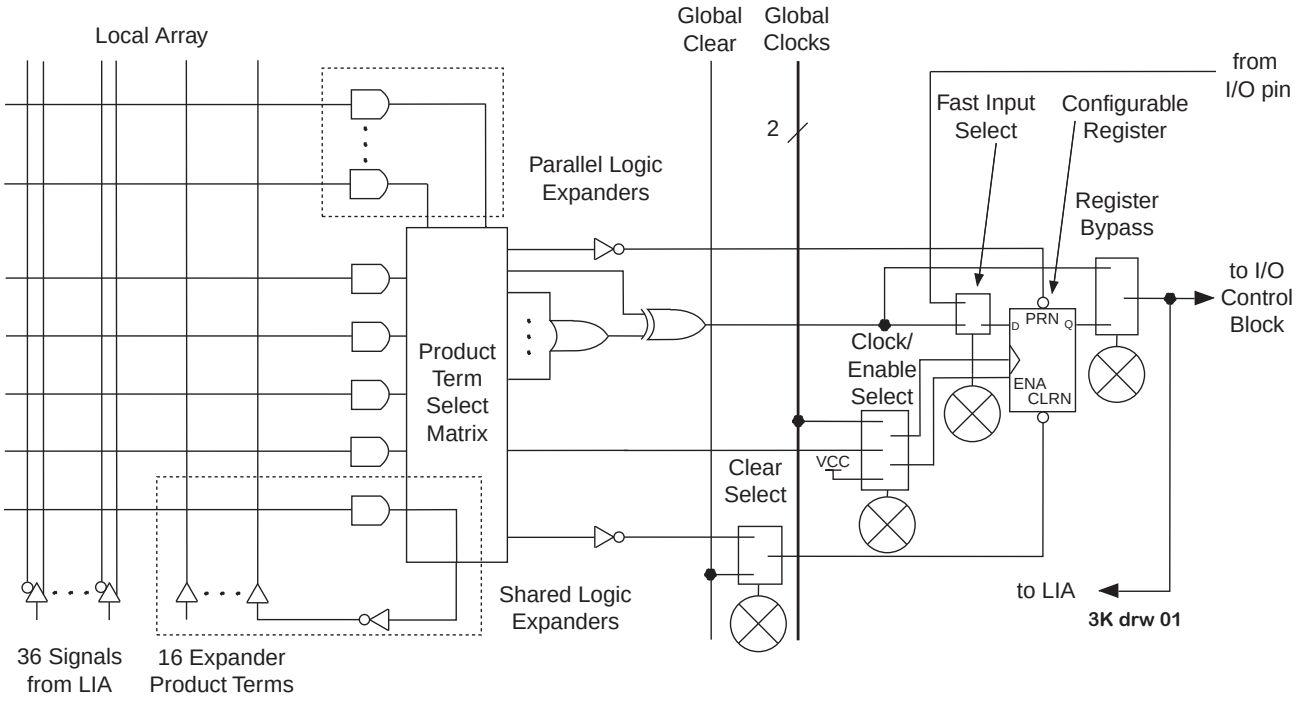
- AN-01: Requesting a First Article. This document provides instructions on how to submit a bitstream file for generation of first articles.
- AN-02: Clear Logic Packaging Guide. This document provides specifications and drawings for packages used by the CL7000 family.
- AN-09: CL7000 Technology White Paper. This document outlines the technologies employed by the CL7000 LPLD family.
- AN-10: Calculating CL7000 Power Consumption. This document provides guidelines for calculating power consumption based on design characteristics.
- AN-11: CL7000 Test Methodology. This document discribes how Clear Logic provides 100% stuck-at fault coverage.

- AN-12: CL7000 LPLD Timing and Function Compatability. This document shows how a seamless conversion from CPLD to ASIC can be achieve with no additional engineering with Clear Logic.

Block Diagram



Macrocell Diagram



CLEARLOGIC

Pin Configuration

Pin Name	100 pin TQFP	144 pin TQFP
INPUT/GCLK1	87	125
INPUT/GCLRn	89	127
INPUT/OE1	88	126
INPUT/OE2/GCLK2	90	128
TDI	4	4
TMS	15	20
TCK	62	89
TDO	73	104
GNDINT	38, 86	52, 57, 124, 129
GND	11, 26, 33, 43, 53, 59, 65, 74, 78, 95	3, 13, 17, 26, 33, 59, 64, 77, 85, 94, 105, 114, 135
VCCINT	39, 91	51, 58, 123, 130
VCCIO	3, 18, 34, 51, 66, 82	24, 50, 73, 76, 95, 115, 144
NC (No Connect)	-	1, 2, 12, 19, 34, 35, 36, 43, 46, 47, 48, 49, 66, 75, 90, 103, 108, 120, 121, 122
Total user I/O pins	**80**	**96**

3128A tbl 01

DC Electrical Specifications

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage, internal logic and input buffers		3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers 3.3 volt operation 2.5 volt operation		 3.0 2.3	 3.6 2.7	 V V
V_I	Input voltage		-0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient Operating temperature Commercial temperature range Industrial temperature range		 0 -40	 70 85	 °C °C
T_J	Ambient Operating temperature Commercial temperature range Industrial temperature range		 0 -40	 90 105	 °C °C
t_R	Input signal rise time			40	ns
t_F	Input signal fall time			40	ns

3KA tbl 02

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground	-0.5	4.6	V
V_I	DC input voltage[1]	With respect to ground	-2.0	5.75	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_A	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	PQFP, and TPFP packages, Under bias		135	°C

3KA tbl 03

DC Electrical Specifications cont.

DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input Voltage		1.7	5.75	V
V_{IL}	Input LOW Voltage[1]		-0.5	0.8	V
V_{OH}	3.3-V high-level TTL output Voltage	I_{OH} = -8 mA DC, V_{CCIO} = 3.00 V	2.4		V
	3.3-V high-level CMOS output Voltage	I_{OH} = -0.1 mA DC, V_{CCIO} = 3.00 V	V_{CCIO}-0.2		V
	2.5-V high-level output Voltage	I_{OH} = -100 µA DC, V_{CCIO} = 2.30 V	2.1		V
		I_{OH} = -1 mA DC, V_{CCIO} = 2.30 V	2.0		
		I_{OH} = -2 mA DC, V_{CCIO} = 2.30 V	1.7		
V_{OL}	3.3-V high-level TTL output Voltage	I_{OH} = 8 mA DC, V_{CCIO} = 3.00 V		0.45	V
	3.3-V high-level CMOS output Voltage	I_{OH} = 0.1 mA DC, V_{CCIO} = 3.00 V		0.2	V
	2.5-V high-level output Voltage	I_{OH} = 100 µA DC, V_{CCIO} = 2.30 V		0.2	V
		I_{OH} = 1 mA DC, V_{CCIO} = 2.30 V		0.4	V
		I_{OH} = 2 mA DC, V_{CCIO} = 2.30 V		0.7	V
I_{IN}	Input Leakage Current	V_I = VCC or GND	-10	10	µA
I_{OZ}	Output Leakage Current	V_O = VCC or GND	-10	10	µA

3KA tbl 04

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

3KA tbl 05

AC Electrical Specifications

I/O Element Timing Parameters

			Speed: -4		Speed: -5		Speed: -6		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C_L = 35 pF		4.5		5.0		6.0	ns
t_{PD2}	I/O input to non-registered output	C_L = 35 pF		4.5		5.0		6.0	ns
t_{SU}	Global clock setup time		3.0		3.2		3.7		ns
t_H	Global clock hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C_L = 35 pF	1.0	2.8	1.0	3.0	1.0	3.3	ns
t_{CH}	Global clock high time		2.0		2.0		3.0		ns
t_{CL}	Global clock low time		2.0		2.0		3.0		ns
t_{ASU}	Array clock setup time		1.4		1.0		0.8		ns
t_{AH}	Array clock hold time		0.8		0.8		1.9		ns
t_{ACO1}	Array clock to output delay	C_L = 35 pF		4.4		5.2	1.0	6.2	ns
t_{ACH}	Array clock high time		2.0		2.0		3.0		ns
t_{ACL}	Array clock low time		2.0		2.0		3.0		ns
t_{CNT}	Minimum global clock period			5.2		5.5		6.4	ns
f_{CNT}	Max. internal global clock frequency		192.3		181.8		156.3		MHz
t_{ACNT}	Minimum array clock period			5.2		5.5		6.4	ns
f_{ACNT}	Max. internal array clock frequency		192.3		181.8		156.3		MHz

3KA tbl 06A1

AC Electrical Specifications cont.

External Timing Parameters

			Speed: -7		Speed: -10		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C_L = 35 pF		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C_L = 35 pF		7.5		10.0	ns
t_{SU}	Global clock setup time		4.9		6.6		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C_L = 35 pF	1.0	4.5	1.0	5.9	ns
t_{CH}	Global clock high time		3.0		4.0		ns
t_{CL}	Global clock low time		3.0		4.0		ns
t_{ASU}	Array clock setup time		1.6		2.1		ns
t_{AH}	Array clock hold time		2.1		3.4		ns
t_{ACO1}	Array clock to output delay	C_L = 35 pF		7.8		10.4	ns
t_{ACH}	Array clock high time		3.0		4.0		ns
t_{ACL}	Array clock low time		3.0		4.0		ns
t_{CNT}	Minimum global clock period			8.4		11.2	ns
f_{CNT}	Max. internal global clock frequency		119.0		89.3		MHz
t_{ACNT}	Minimum array clock period			8.4		11.2	ns
f_{ACNT}	Max. internal array clock frequency		119.0		89.3		MHz

3KA tbl 06A2

AC Electrical Specifications cont.

Internal Timing Parameters[4]

			Speed: -4		Speed: -5		Speed: -6		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			0.3		0.3		0.3	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.3		0.3	ns
t_{SEXP}	Shared expander delay			1.9		2.4		2.8	ns
t_{PEXP}	Parallel expander delay			0.5		0.6		0.5	ns
t_{LAD}	Logic array delay			1.9		2.5		2.5	ns
t_{LAC}	Logic control array delay			1.8		2.3		2.5	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.2	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		0.3		0.4		0.3	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		0.8		0.9		0.8	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		5.3		5.4		5.3	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		4.0		4.0		4.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		4.5		4.5		4.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C_L = 5 pF[3]		4.0		4.0		4.0	ns
t_{SU}	Register setup time		1.4		0.8		1.0		ns
t_H	Register hold time		0.8		1.0		1.7		ns
t_{RD}	Register delay			1.2		1.4		1.6	ns
t_{COMB}	Combinatorial delay			1.3		1.0		1.6	ns
t_{IC}	Array clock delay			1.9		2.3		2.7	ns
t_{EN}	Register enable time			1.8		2.3		2.5	ns
t_{GLOB}	Global control delay			1.0		0.9		1.1	ns
t_{PRE}	Register preset time			2.3		2.6		2.3	ns
t_{CLR}	Register clear time			2.3		2.6		2.3	ns
t_{LIA}	LIA delay			0.7		0.8		1.3	ns

3KA tbl 07A1

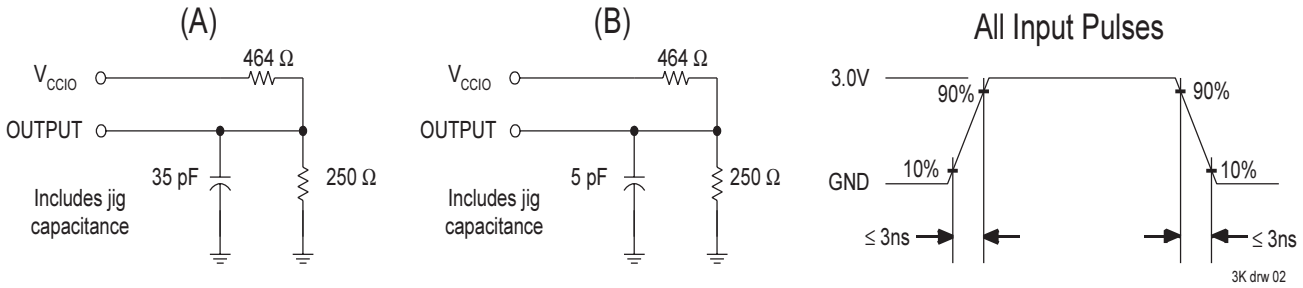
AC Electrical Specifications cont.

Internal Timing Parameters[4]

			Speed: -7		Speed: -10		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			0.4		0.6	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.6	ns
t_{SEXP}	Shared expander delay			3.6		4.9	ns
t_{PEXP}	Parallel expander delay			0.8		1.1	ns
t_{LAD}	Logic array delay			3.7		5.0	ns
t_{LAC}	Logic control array delay			3.4		4.6	ns
t_{IOE}	Internal output enable delay			0.0		0.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		0.6		0.7	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		1.1		1.2	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		5.6		5.7	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C_L = 5 pF[3]		4.0		5.0	ns
t_{SU}	Register setup time		1.3		1.7		ns
t_H	Register hold time		2.4		3.8		ns
t_{RD}	Register delay			2.1		2.8	ns
t_{COMB}	Combinatorial delay			1.5		2.0	ns
t_{IC}	Array clock delay			3.4		4.6	ns
t_{EN}	Register enable time			3.4		4.6	ns
t_{GLOB}	Global control delay			1.4		1.8	ns
t_{PRE}	Register preset time			3.9		5.2	ns
t_{CLR}	Register clear time			3.9		5.2	ns
t_{LIA}	LIA delay			1.3		1.7	ns

3KA tbl 07A2

AC Test Conditions



Notes to Tables

1. During transitions, inputs may undershoot to -2.0V for periods shorter than 20ns. Otherwise, minimum DC input voltage is 0.3V.

2. Typical values are at V_{CC} of 5.0 volts and ambient temperature of 25 ºC.

3. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.

4. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

Revision History

20 Oct.. 2000: Created preliminary document.

1 Dec. 2000: Updated application note reference.

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL3128ATC100-10	Commercial	100-pin Thin QFP	-10	EPML3128ATC100-10
CL3128ATC100-7			-7	EPM3128ATC100-7
CL3128ATC100-5			-5	EPM3128ATC100-5
CL3128ATC100-4			-4	N/A
CL3128ATC144-10		144-pin Thin QFP	-10	EPM3128ATC144-10
CL3128ATC144-7			-7	EPM3128ATC144-7
CL3128ATC144-5			-5	EPM3128ATC144-5
CL3128ATC144-4			-4	N/A

3128A tbl 02