CDP1881C, CDP1882, CDP1882C

CMOS 6-Bit Latch and Decoder Memory Interfaces

March 1997

Features

- **Performs Memory Address Latch and Decoder Functions Multiplexed or Non-Multiplexed**
- **Decodes Up to 16K Bytes of Memory**
- **Interfaces Directly with CDP1800-Series Microprocessors at Maximum Clock Frequency**
- **Can Replace CDP1866 and CDP1867 (Upward Speed and Function Capability)**

Ordering Information

PACKAGE	5V	10V	TEMP. RANGE (^oC)	PKG. NO.
PDIP	CDP1881CE	-	-40 to +85	E20.3
PDIP	CDP1882CE	-	-40 to +85	E18.3
PDIP Burn-In	CDP1882CEX	-	-40 to +85	E18.3
SBDIP	-	CDP1882D	-40 to +85	D18.3

Description

The CDP1881C, CDP1882 and CDP1882C are CMOS 6-bit memory latch and decoder circuits intended for use in CDP1800 series microprocessor systems. They can interface directly with the multiplexed address bus of this system at maximum clock frequency, and up to four 4K x 8-bit memories to provide a 16K byte memory system. With four 2K x 8-bit memories an 8K byte system can be decoded.

The devices are also compatible with non-multiplexed address bus microprocessors. By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general purpose memory-system applications.

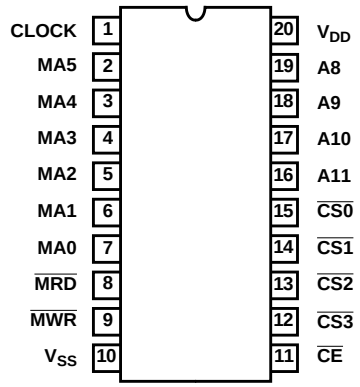
The CDP1881C, CDP1882 and CDP1882C are intended for use with 2K or 4K byte RAMs and are identical except that in the CDP1882 $\overline{MWR}$ and $\overline{MRD}$ are excluded.

The CDP1882 is functionally identical to the CDP1882C. It differs in that the CDP1882 has recommended operating voltage range of 4V to 10.5V and the C version has a recommended operating voltage range of 4V to 6.5V.

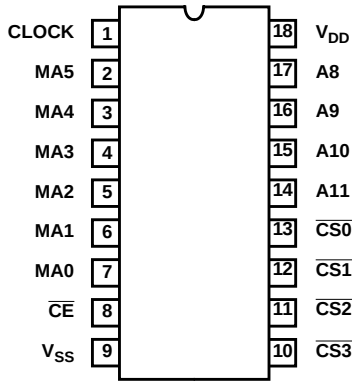
The CDP1881C, CDP1882 and CDP1882C are supplied in 20 lead and 18 lead packages, respectively. The CDP1881C is supplied only in a dual-in-line plastic package (E suffix). The CDP1882 is supplied in dual-in-line, hermetic side-brazed ceramic (D suffix) and in plastic (E suffix) packages.

Pinouts

CDP1881C
(PDIP)
TOP VIEW



CDP1882, CDP1882C
(PDIP, CERDIP)
TOP VIEW



File Number **1367.2**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1882 . . . . . -0.5V to +11V
CDP1881C and CDP1882C. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
18 Lead PDIP	85	N/A
20 Lead PDIP	80	N/A
SBDIP Package	85	22

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D. . . . . -55^oC to $+125^oC$
Package Type E. . . . . -40^oC to $+85^oC$
Storage Temperature Range (T_{STG}) . . . . . -65^oC to $+150^oC$
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . $+265^oC$

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	CDP1882		CDP1881C, CDP1882C		UNITS
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications

At T_A = -40^oC to $+85^oC$, V_{DD} ± 5%, Except as Noted:

PARAMETER	SYMBOL	CONDITIONS			CDP1882			CDP1881C, CDP1882C			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	1	10	-	5	50	µA
		-	0, 10	10	-	10	100	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	3.2	6.4	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.3	-4.6	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1, 9	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		1, 9	-	10	7	-	-	-	-	-	V

Static Electrical Specifications At T_A = -40°C to +85°C, V_{DD} ± 5%, Except as Noted: **(Continued)**

PARAMETER	SYMBOL	CONDITIONS			CDP1882			CDP1881C, CDP1882C			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	-	-	±1	µA
			0, 10	10	-	-	±2	-	-	-	µA
Operating Current (Note 2)	I_{DD1}	0, 5	0, 5	5	-	-	2	-	-	2	mA
		0, 10	0, 10	10	-	-	4	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF
Minimum Data Retention Voltage	V_{DR}	$V_{DD} = V_{DR}$			-	2	2.4	-	2	2.4	V
Data Retention Current	I_{DR}	V_{DD} = 2.4V			-	0.01	1	-	0.5	5	µA

NOTES:

1. Typical values are for T_A = +25°C.
2. $I_{OL} = I_{OH}$ = 1µA.
3. Operating current measured at 200kHz for V_{DD} = 5V and 400kHz for V_{DD} = 10V, with outputs open circuits (equivalent to typical CDP1800 system at 3.2MHz, 5V; and 6.4MHz, 10V).

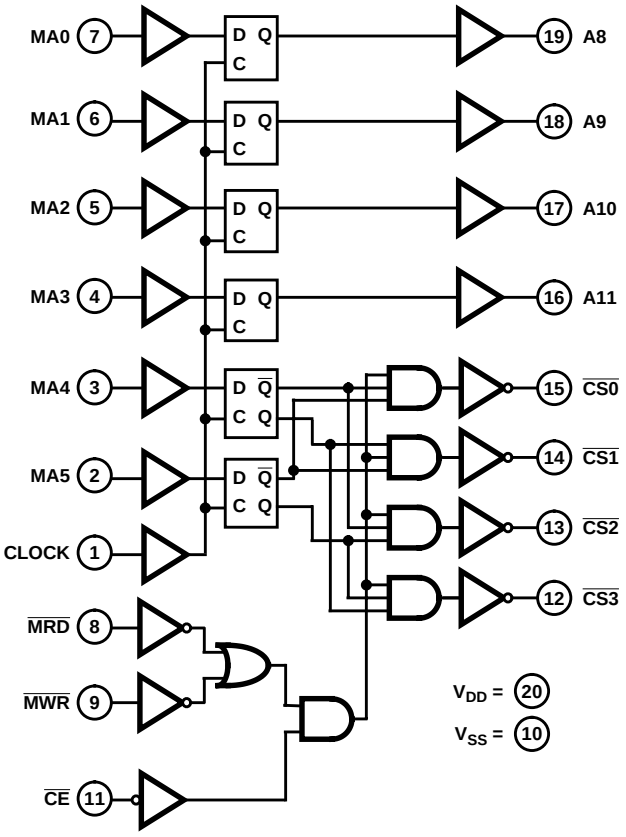


FIGURE 1. FUNCTIONAL DIAGRAM FOR THE CDP1881C

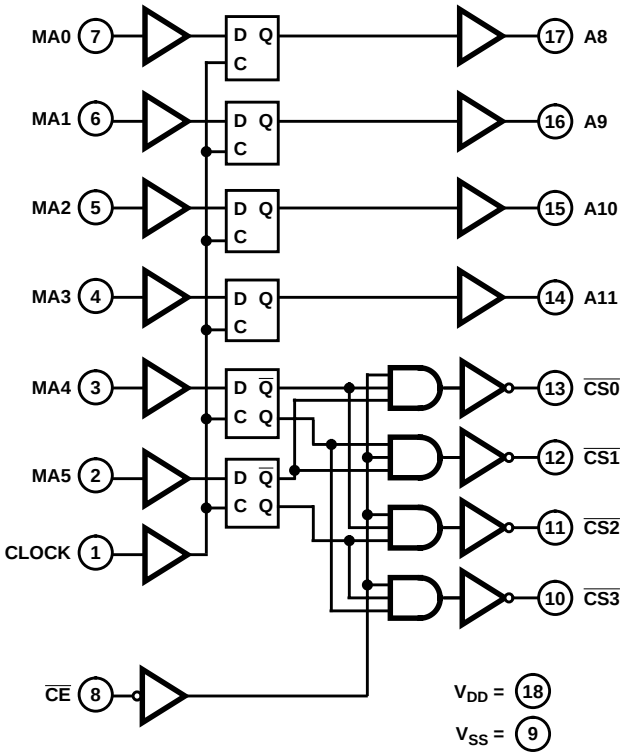


FIGURE 2. FUNCTIONAL DIAGRAM FOR THE CDP1882, CDP1882C

TRUTH TABLE

INPUTS						OUTPUTS			
(NOTE 1) $\overline{\text{MWR}}$	(NOTE 1) $\overline{\text{MRD}}$	$\overline{\text{CE}}$	CLK	MA4	MA5	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	$\overline{\text{CS2}}$	$\overline{\text{CS3}}$
1	1	X	X	X	X	1	1	1	1
X	X	1	X	X	X	1	1	1	1
0	X	0	1	0	0	0	1	1	1
0	X	0	1	1	0	1	0	1	1
0	X	0	1	0	1	1	1	0	1
0	X	0	1	1	1	1	1	1	0
0	X	0	0	X	X	Previous State			
X	0	0	1	0	0	0	1	1	1
X	0	0	1	1	0	1	0	1	1
X	0	0	1	0	1	1	1	0	1
X	0	0	1	1	1	1	1	1	0
X	0	0	0	X	X	Previous State			

NOTE:

1. CDP1881C Only

INPUTS			OUTPUTS
$\overline{\text{CE}}$	CLK	MA0, MA1, MA2, MA3	A8, A9, A10, A11
X	1	1	1
X	1	0	0
X	0	X	Previous State

Logic 1 = High, Logic 0 = Low, X = Don't Care

Dynamic Electrical Specifications at T_A = -40°C to +85°C, $V_{DD} \pm 5\%$, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 1)

PARAMETER		V_{DD} (V)	CDP1882			CDP1881C, CDP1882C			UNITS
			MIN	(NOTE 1) TYP	(NOTE 2) MAX	MIN	(NOTE 1) TYP	(NOTE 2) MAX	
Minimum Setup Time	t_{MACL}	5	-	10	35	-	10	35	ns
Memory Address to CLOCK		10	-	8	25	-	-	-	ns
Minimum Hold Time	t_{CLMA}	5	-	8	25	-	8	25	ns
Memory Address After CLOCK		10	-	8	25	-	-	-	ns
Minimum CLOCK Pulse Width	t_{CLCL}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ± 5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 1) **(Continued)**

PARAMETER		V_{DD} (V)	CDP1882 MIN	CDP1882 (NOTE 1) TYP	CDP1882 (NOTE 2) MAX	CDP1881C, CDP1882C MIN	CDP1881C, CDP1882C (NOTE 1) TYP	CDP1881C, CDP1882C (NOTE 2) MAX	UNITS
PROPAGATION DELAY TIMES									
$\overline{\text{Chip}}$ $\overline{\text{Enable}}$ to $\overline{\text{Chip}}$ $\overline{\text{Select}}$	t_{CECS}	5	-	75	150	-	75	150	ns
		10	-	45	100	-	-	-	ns
$\overline{\text{MRD}}$ or $\overline{\text{MRW}}$ to $\overline{\text{Chip}}$ $\overline{\text{Select}}$ (Note 3)	t_{MCS}	5	-	75	150	-	75	150	ns
		10	-	40	100	-	-	-	ns
CLOCK to $\overline{\text{Chip}}$ $\overline{\text{Select}}$	t_{CLCS}	5	-	100	175	-	100	175	ns
		10	-	65	125	-	-	-	ns
CLOCK to Address	t_{CLA}	5	-	100	175	-	100	175	ns
		10	-	65	125	-	-	-	ns
Memory Address to $\overline{\text{Chip}}$ $\overline{\text{Select}}$	t_{MACS}	5	-	100	175	-	100	175	ns
		10	-	75	125	-	-	-	ns
Memory Address to Address	t_{MAA}	5	-	80	125	-	80	125	ns
		10	-	40	60	-	-	-	ns

NOTES:

1. Typical values are for T_A = 25°C.
2. Maximum limits of minimum characteristics are the values above which all devices function.
3. For CDP1881C type only.

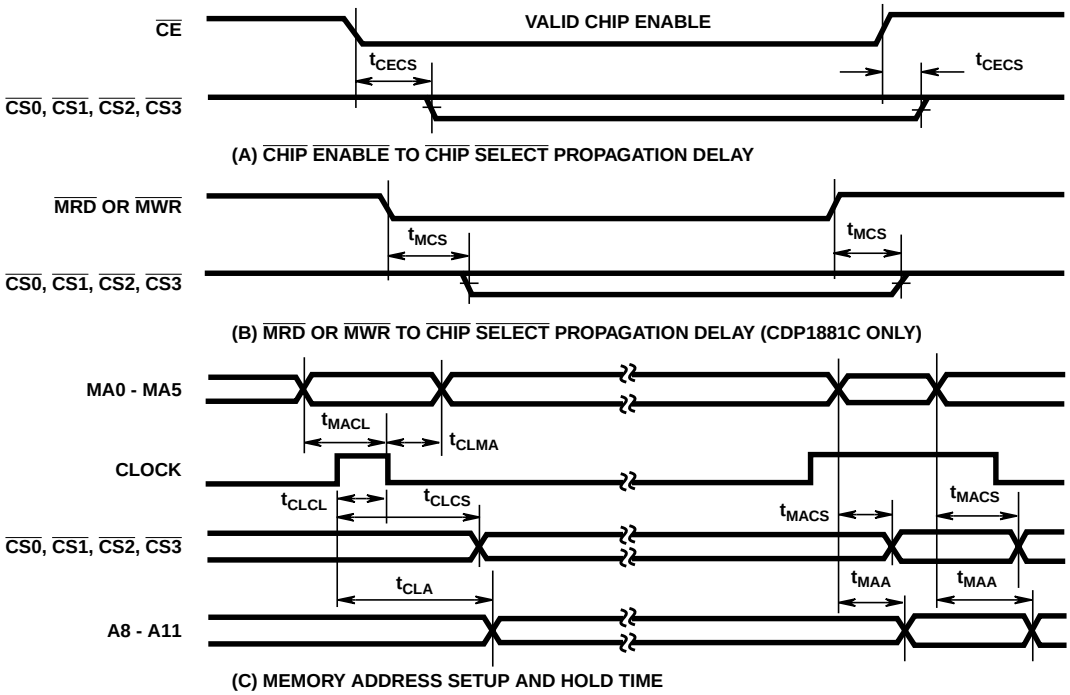


FIGURE 3. TIMING WAVEFORMS

Signal Descriptions/Pin Functions

CLOCK: Latch-Input Control - a high at the clock input will allow data to pass through the latch to the output pin. Data is latched on the high to low transition of the clock input. This input is connected to TPA in CDP1800-series systems.

MA0 - MA3: Address inputs to the high-byte address latches.

MA4 - MA5: High byte address inputs decoded to produce chip selects $\overline{CS0}$ - $\overline{CS3}$.

MRD, MWR: MEMORY READ ($\overline{MRD}$) and MEMORY WRITE ($\overline{MWR}$) signal inputs on the CDP1881C. A low at either input, when the $\overline{CE}$ pin is low, will enable the decoder chip select outputs ($\overline{CS0}$ - $\overline{CS3}$).

CE: CHIP ENABLE input - a low at the $\overline{CE}$ input of CDP1882, CDP1882C will enable the chip select decoder. A low at the $\overline{CE}$ input of CDP1881C, coincident with a low at either $\overline{MRD}$ or $\overline{MRW}$ pin, will enable the chip select decoder. A high on this pin forces $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$ to a high (false) state.

A8 - A11: Latched high-byte address outputs.

CS0 - CS3: One of four latched and decoded Chip Select outputs.

V_{DD}, V_{SS}: Power and ground pins, respectively.

Application Information

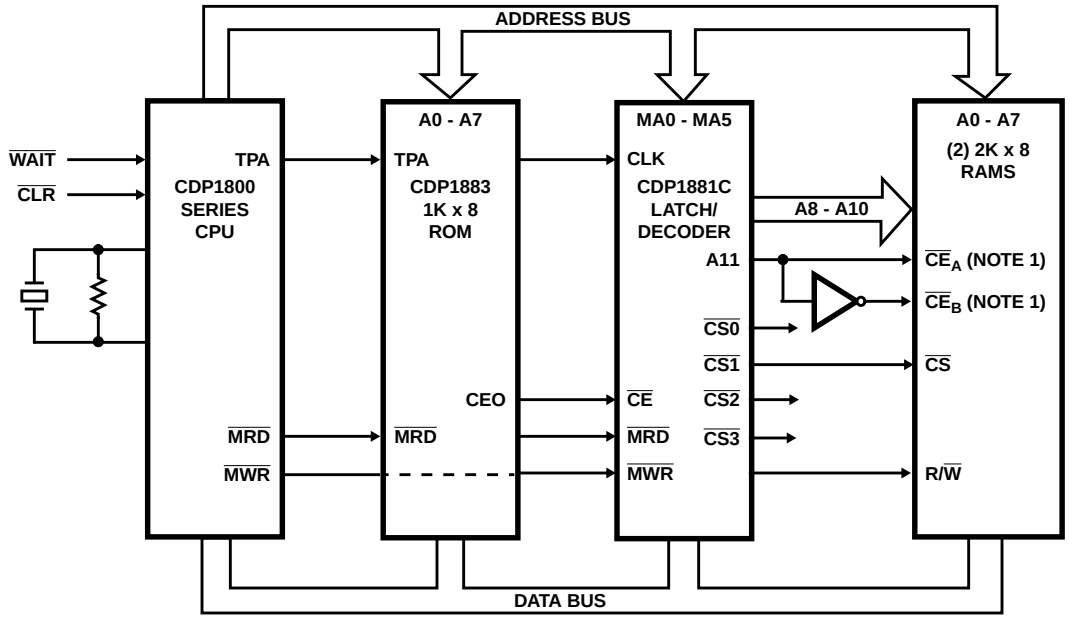
The CDP1881C, CDP1882, CDP1882C can interface directly with the multiplexed address bus of the CDP1800-series microprocessor family at maximum clock frequency. A single CDP1881C or CDP1882 is capable of decoding up to 16K-bytes of memory.

The CDP1881C is provided with $\overline{MRD}$ and $\overline{MWR}$ inputs for controlling bus contention, and is especially useful for interfacing with RAMs that do not have an output enable function ($\overline{OE}$). Figure 4 shows the CDP1881C in a minimum system configuration which includes the CDP1833 ROM (1K x 8) and two 2K x 8 RAMS. The CDP1881C in this example performs the following functions:

1) Latch and decode high-order address bits for use as chip selects.
2) Gate chip selects with $\overline{MRD}$ and $\overline{MWR}$ to prevent bus contention with the CPU.
3) Latch high-order address bits A8 to A11.

A system using the CDP1882 is shown in Figure 5. The CDP1882 performs the memory address latch and decoder functions. Note that the RAM has an output enable ($\overline{OE}$) pin which eliminates the need for $\overline{MRD}$ and $\overline{MWR}$ inputs on the latch/decoder. Instead, the $\overline{MRD}$ line is connected directly to the RAM output enable ($\overline{OE}$) pin.

In Figure 6 the CDP1882 is used to decode a 16K-byte ROM system consisting of four CDM5332s.



NOTE: $\overline{CE}_A$ = $\overline{CE}$ RAM NUMBER 1
$\overline{CE}_B$ = $\overline{CE}$ RAM NUMBER 2

FIGURE 4. MINIMUM 1800-SERIES USING THE CDP1881C

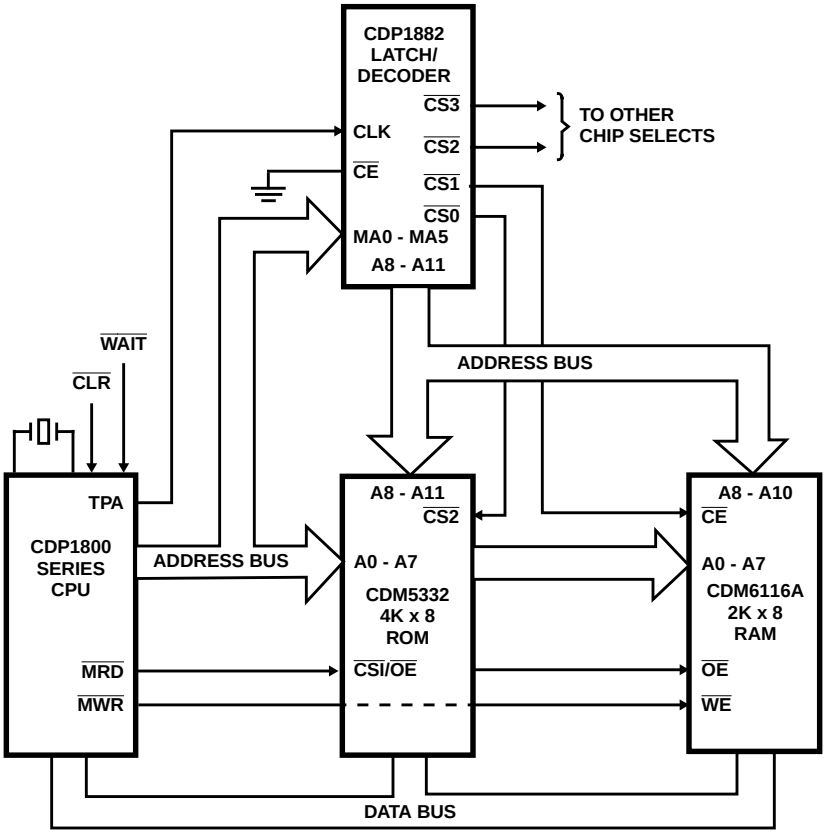


FIGURE 5. CDP1800-SERIES SYSTEM USING THE CDP1882

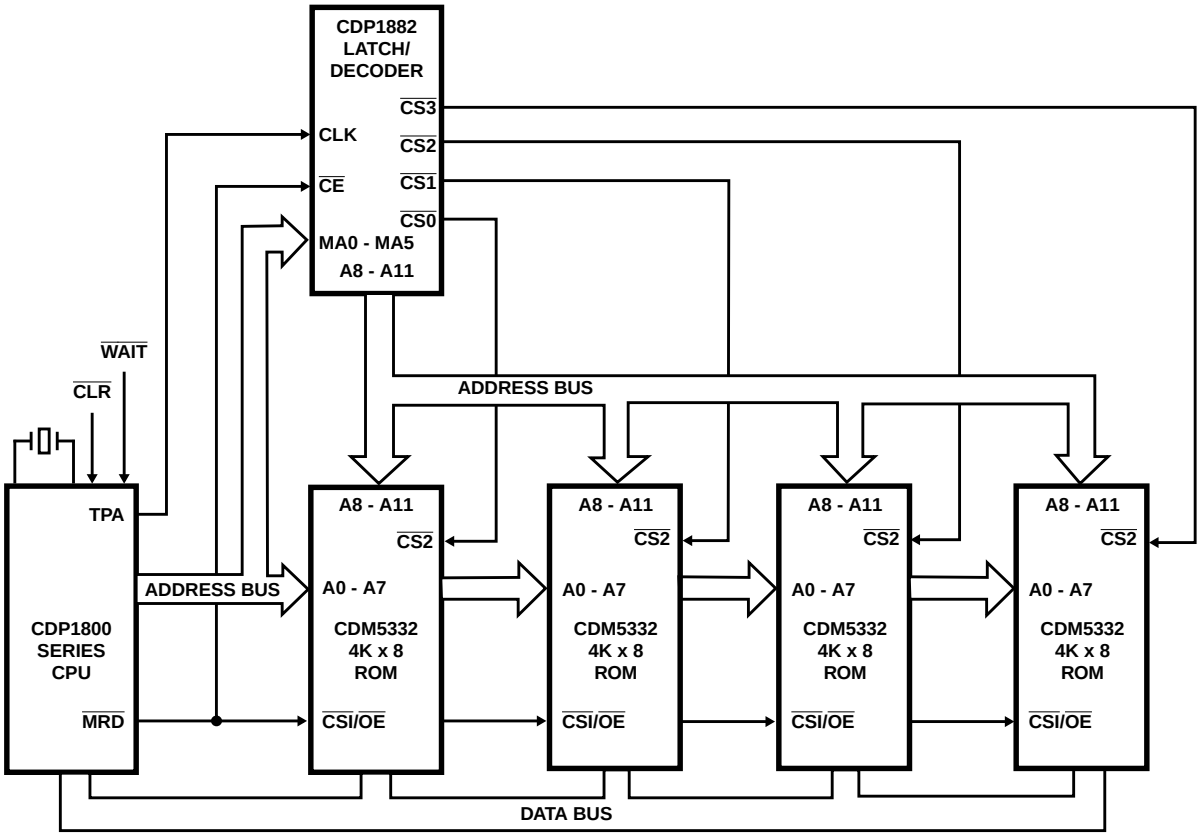


FIGURE 6. 6K-BYTE ROM SYSTEMS USING THE CDP1882

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