CDB61584A

Product Databook

FEATURES

- **Socketed CS61584A Dual Line Interface**
- **All Required Components for CS61584A Evaluation**
- **Locations to Evaluate Protection Circuitry**
- **LED Status Indications for Alarm Conditions**
- **Support for Hardware and Host Modes**

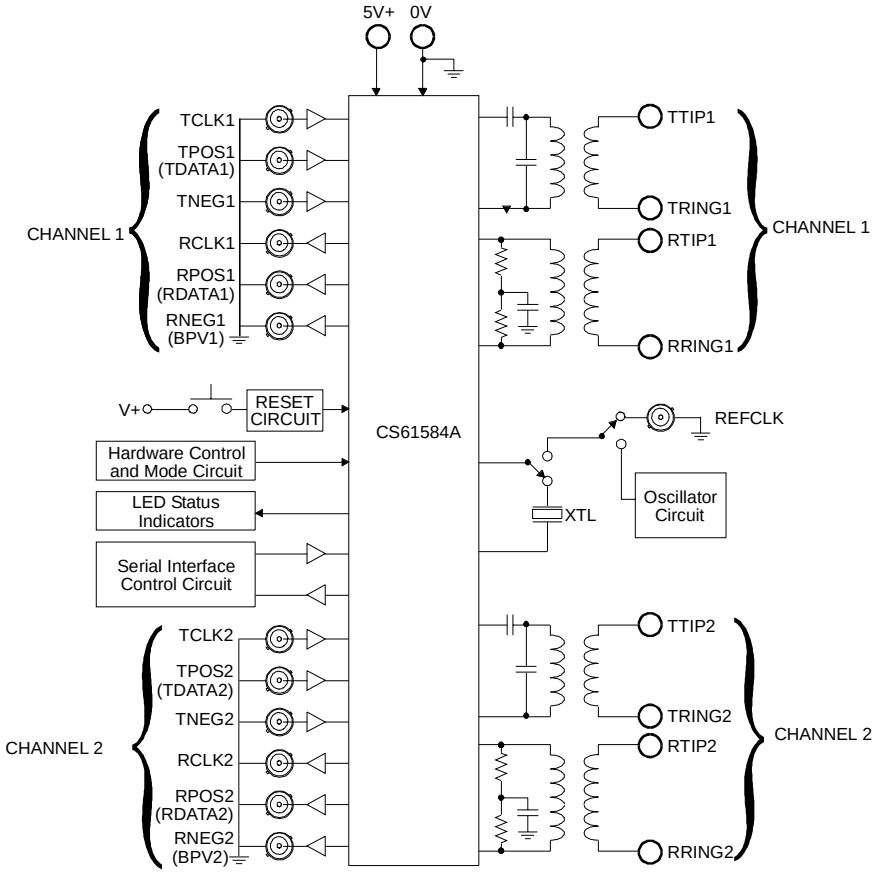
Dual Line Interface Unit

DESCRIPTION

The evaluation board includes a socketed CS61584A dual line interface device and all support components necessary for evaluation. The board is powered by an external +5 Volt supply.

The board may be configured for 100Ω twisted-pair T1, 75Ω coax E1, or 120Ω twisted-pair E1 operation. Binding posts and bantam jacks are provided for line interface connections. Several BNC connectors provide clock and data I/O at the system interface. Reference timing may be derived from a quartz crystal, crystal oscillator, or an external reference clock. Four LED indicators monitor device alarm conditions.

ORDERING INFORMATION:
CDB61584A



POWER SUPPLY

As shown on the evaluation board schematic in Figures 1-5, power is supplied to the board from an external +5 Volt supply connected to the two binding posts labeled V+ and GND. Zener diode Z1 protects the components on the board from reversed supply connections and over-voltage damage. Capacitor C16 provides power supply decoupling and ferrite bead L1 helps isolate the CS61584A and buffer supplies. Both sides of the evaluation board contain extensive areas of ground plane to insure optimum performance.

Capacitors C3, C5-C8, C13, C18, and C38 provide power supply decoupling for the CS61584A. The BGREF pin is pulled down through resistor R10 to provide an internal current reference. The buffers are decoupled using capacitors C9, C15, and C19. Ferrite beads L2-L4 help reduce the power supply noise that is coupled from the buffers to the power supply.

BOARD CONFIGURATION

Slide switch SW6 selects hardware or host mode operation. Hardware mode is selected when switch SW6 is in the "HW" position and sets the MODE pin of the CS61584A to a logic 0. Host mode is selected when switch SW6 is in the "SW" position and sets the MODE pin of the CS61584A to a logic 1.

Hardware Mode

In Hardware mode operation, the evaluation board is configured using DIP switches SW2, SW3, and SW4. In this mode, the switches establish the digital control inputs for both line interface channels. Closing a DIP switch towards the label sets the CS61584A control pin of the same name to a logic 1. The host processor interface J26 should not be used in the Hardware mode.

The CDB61584A switches and functions are listed below:

- TAOS1, TAOS2: transmit all ones;
- LLOOP: local loopback of both channels;
- RLOOP1,2: remote loopback 1,2;
- PD1, PD2: power down;
- ATTEN0, ATTEN1: jitter attenuator selection;
- CLKE: RCLK edge polarity;
- 1XCLK: clock frequency selection;
- CONx1, CONx2: line configuration settings.

All switch inputs are pulled-down using resistor networks RP2-RP5.

The LOS1 and LOS2 LED indicators illuminate when the line interface receiver has detected a loss of signal. Headers J7 and J13 must be jumpered in the "TNEG" position to provide connectivity to the BNC input in Hardware mode.

Host Mode

In Host mode operation, the evaluation board supports serial-port operation over interface port J26 using the printer port of a host PC equipped with the enclosed software. The evaluation board is connected to the host PC using the ribbon cable provided. The SW2 switch position labeled "ATTEN0" must be open to set the P/S pin of the CS61584A to a logic 0 and enable serial-port operation.

An external microprocessor may also interface to the evaluation board for the purposes of system software development. The CS61584A interrupt pin is connected to pin 23 of interface port J26 to facilitate software development. The SW2 switch position labeled "CLKE/IPOL" establishes the polarity of the interrupt pin. If an active low interrupt is selected (IPOL low), the interrupt pin must be pulled-up through resistor R55 by placing a jumper on header J24. The SW2 switch position labeled "RLOOP1" must be in the open position for proper operation of the interrupt.

The LOS1 and LOS2 LED indicators illuminate when the line interface receiver has detected a loss of signal. If coder mode is enabled in the CS61584A register set, the AIS alarm condition is

provided when headers J7 and J13 are jumpered in the "AIS" position. The AIS1 and AIS2 LED indicators illuminate when the line interface receiver has detected the all-ones receive input signal. Resistors R26 and R27 pull-down the TNEG(1,2) inputs when coder mode is disabled but headers J7 and J13 are jumpered in the "AIS" position.

Further details concerning Host mode operation are described in the "readme.txt" file on the enclosed disk.

Manual Reset

A momentary contact switch SW1 provides a manual reset by forcing the RESET pin of the CS61584A to a logic 1. Although the transmit and receive circuitry are continuously calibrated, the reset can be used to initialize the control logic and clear the register set. Both channels are powered up after exiting reset.

TRANSMIT CIRCUIT

The transmit clock and data signals are supplied on BNC inputs labeled TCLK(1,2), TPOS(1,2), and TNEG(1,2). In Hardware and Host mode (with coder mode disabled), data is supplied on the TPOS(1,2) and TNEG(1,2) BNC inputs in RZ format. In Host mode with coder mode enabled, data is supplied on the TDATA(1,2) BNC input in NRZ format and the TNEG(1,2) BNC input may be used to indicate the AIS alarm condition as described in the Host Mode section.

The transmitter output is transformer coupled to the line interface through 1:1.15 step-up transformers T1 and T4. The signal is available at either the TTIP(1,2) and TRING(1,2) binding posts or the TX(1,2) bantam jacks.

Capacitors C2 and C11 prevent output stage imbalances from producing a DC current that may saturate the transformer and result in an output level offset. Capacitors C1 and C12 provide transmitter return loss and are socketed so the value may be changed according to the application. A 220 pF capacitor is required for 100Ω twisted-pair T1 or 120Ω twisted-pair E1 applications. A 470 pF capacitor is required for 75Ω coax E1 applications. These capacitors are included with the evaluation board.

Optional diode locations D6-D9 and D10-D13 and optional resistor locations R8-R9 and R18-R19 provide test locations to evaluate transmit line interface protection circuitry.

RECEIVE CIRCUIT

The receive signal is input at either the RTIP(1,2) and RRING(1,2) binding posts or the RX(1,2) bantam jacks. The receive signal is transformer coupled to the CS61584A through 1:1.15 step-down transformers T2 and T3.

The receive line is terminated by resistors R3-R4 and R14-R15 to provide impedance matching and receiver return loss. They are socketed so the values may be changed according to the application. The evaluation board is supplied from the factory with 38.3Ω resistors for terminating 100Ω twisted-pair T1 lines, 45.3Ω resistors for terminating 120Ω twisted-pair E1 lines, and 28.7Ω resistors for terminating 75Ω coaxial E1 lines. Capacitors C4 and C10 provide a differential input voltage reference.

Optional resistor locations R1-R2, R12-R13, R16-R17, and R24-R25 provide test locations to evaluate receive line interface protection circuitry.

The recovered clock and data signals are available on BNC outputs labeled RCLK(1,2), RPOS(1,2), and RNEG(1,2). In Hardware and Host mode (with coder mode disabled), data is available on the RPOS(1,2) and RNEG(1,2) BNC outputs in RZ format. In Host mode with coder mode enabled, data is available on the RDATA(1,2) BNC output in NRZ format and bipolar violations are reported on BPV(1,2).

REFERENCE CLOCK

The CDB61584A requires a T1 or E1 reference clock for operation. This clock may operate at either a 1-X rate (1.544 MHz or 2.048 MHz) or an 8-X rate (12.352 MHz or 16.384 MHz) and can be supplied by either a quartz crystal, crystal oscillator, or external reference. The evaluation board is supplied from the factory with two crystal oscillators for T1 and E1 operation.

Quartz Crystal

A quartz crystal may be inserted at socket Y1. Because the crystal operates at an 8-X rate, the SW2 switch position labeled "1XCLK" must be open to set the 1XCLK pin of the CS61584A to a logic 0 and enable 8-X clock operation.

Crystal Oscillator

A crystal oscillator may be inserted at socket U4 in the orientation indicated by the silkscreen. Header J14 must be jumpered in the "OSC" position to provide connectivity to the REFCLK pin of the CS61584A. The SW2 switch position labeled "1XCLK" must be open (logic 0) for 8-X clock operation or closed (logic 1) for 1-X clock operation.

External Reference

An external reference may be provided at the REFCLK BNC input. Header J14 must be jumpered in the "REFCLK" position to provide connectivity to the REFCLK pin of the CS61584A. The SW2 switch position labeled "1XCLK" must be open (logic 0) for 8-X clock operation or closed (logic 1) for 1-X clock operation.

BUFFERING

Buffers U2, U3, and U6 provide additional drive capability for the BNC and Host mode connections. The buffer outputs are filtered with an RC network to reduce the transients caused by buffer switching.

JTAG ACCESS

The CS61584A implements JTAG boundary scan to support board-level testing. Interface port J56 provides access to the four JTAG pins on the CS61584A. The J-TMS pin of the CS61584A is pulled-down by resistor R28 to disable boundary scan unless the pin is externally pulled high using the interface port.

TRANSFORMER SELECTION

The evaluation board is supplied from the factory with Pulse Engineering PE-65388 transformers installed at locations T1-T4. They are socketed to permit the evaluation of other transformers.

LINE PROTECTION EVALUATION

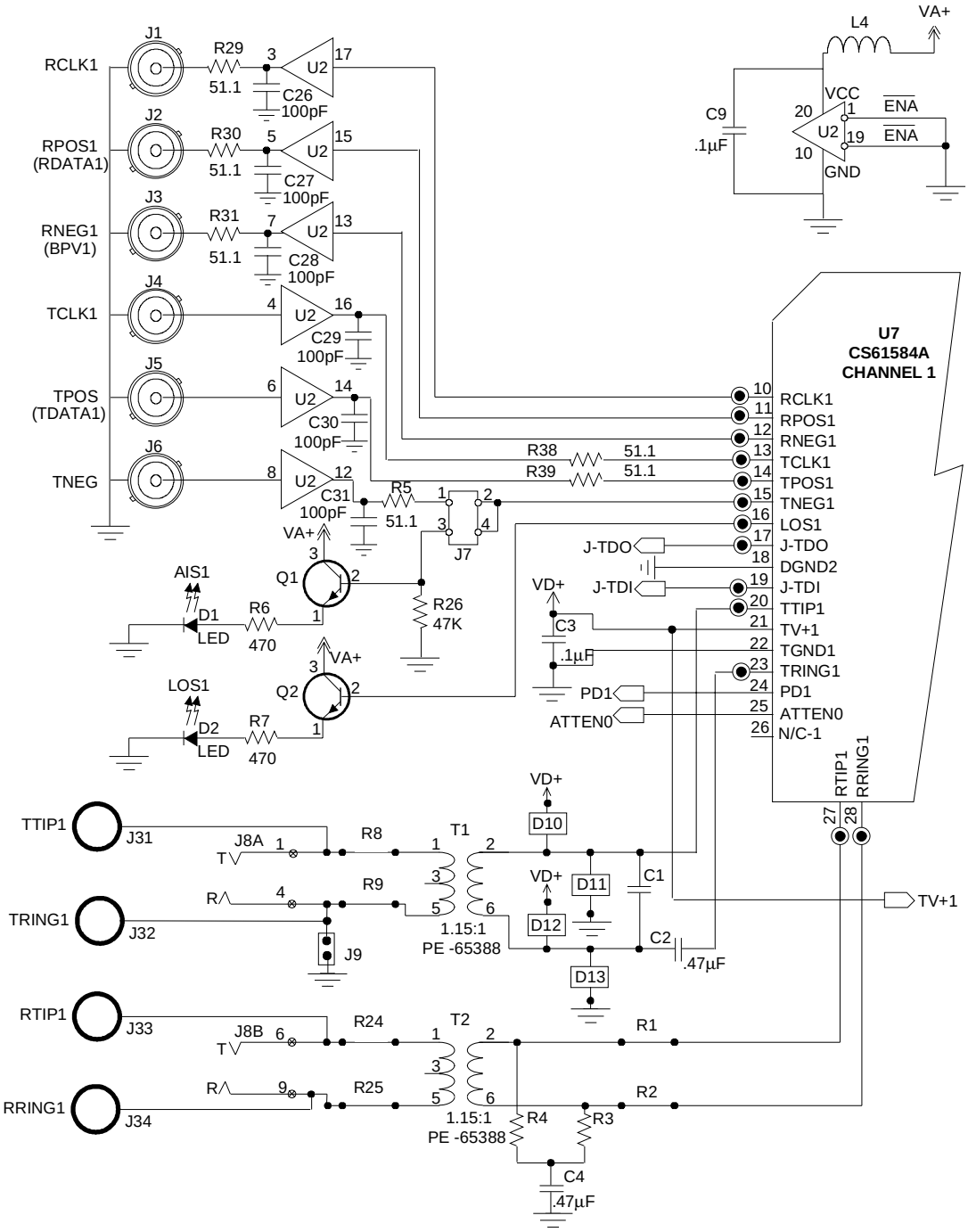
Several optional resistor and diode locations on the transmit and receive line interface allow for the installation and evaluation of various types of protection circuitry. Each location is drilled with 60 mil vias to permit the installation of sockets. These sockets can be obtained from McKenzie at (510) 651-2700 by requesting part #PPC-SIP-1X32-620C and are identical to the socket type installed at the receive resistor locations on the board. They allow the line protection circuitry to be easily changed during testing. Note that the traces forming shorts between the socket locations on the line interface may need to be cut prior to the installation of protection circuitry.

PROTOTYPING AREA

Four prototyping areas with power supply and ground connections are provided on the evaluation board. These areas can be used to develop and test a variety of additional circuits such as framer devices, system synchronizer PLLs, or specialized interface logic.

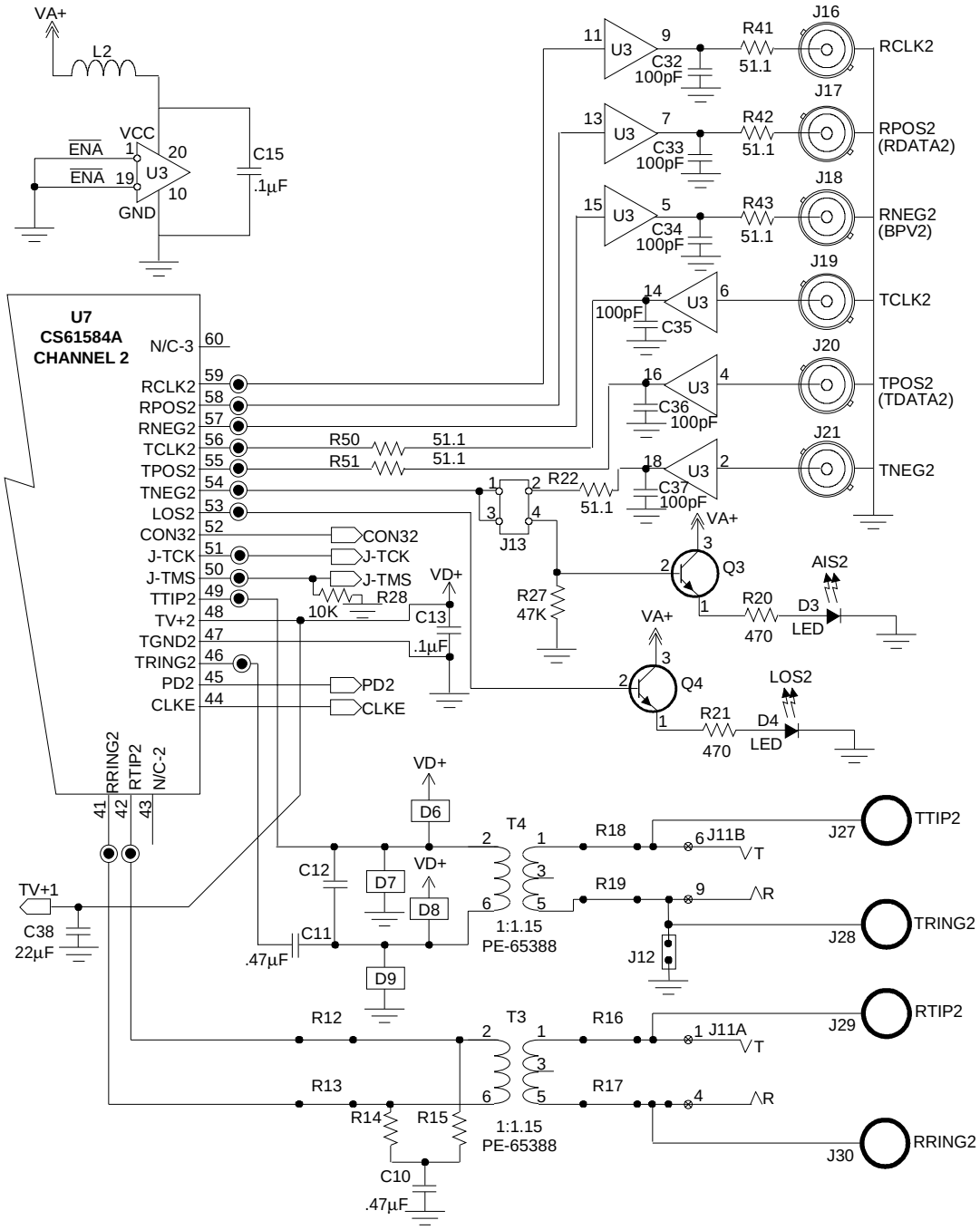
EVALUATION HINTS

1) The orientation of pin 1 for the CS61584A is labeled "1" on the left side of the socket U7.
2) A jumper must not be placed on header J10 when using the CDB61584A.
3) Component locations R3-R4, R14-R15, C1, and C12 must have the correct values installed according to the application. All the necessary components are included with the evaluation board.
4) Closing a DIP switch on SW2, SW3, and SW4 towards the label sets the CS61584A control pin of the same name to logic 1.
5) When performing a manual loopback of the recovered signal to the transmit signal at the BNC connectors, the recovered data must be valid on the falling edge of RCLK to properly latch the data in the transmit direction. To accomplish this, the SW2 switch position labeled "CLKE" must be closed (logic 1) during Hardware mode operation or the CLKE bit in the Control A register must be set to a 1 during Host mode operation.
6) Jumpers can be placed on headers J9 and J12 to provide a ground reference on TRING for 75Ω coax E1 applications.
7) Properly terminate TTIP/TRING when evaluating the transmit output pulse shape. For more information concerning pulse shape evaluation, refer to the Crystal application note entitled "Measurement and Evaluation of Pulse Shapes in T1/E1 Transmission Systems."



Notes: Components R3, R4, and C1 are socketed to permit value changes to the application.
Component locations R1, R2, R8, R9, R24, R25, and D10-D13 provide areas for evaluating protection circuitry.

Figure 1. Channel 1 Circuitry



Notes: Components R14, R15, and C12 are socketed to permit value changes according to the application.
Component locations R12, R13, R16-R19, and D6-D9 provide areas for evaluating protection circuitry.

Figure 2. Channel 2 Circuitry

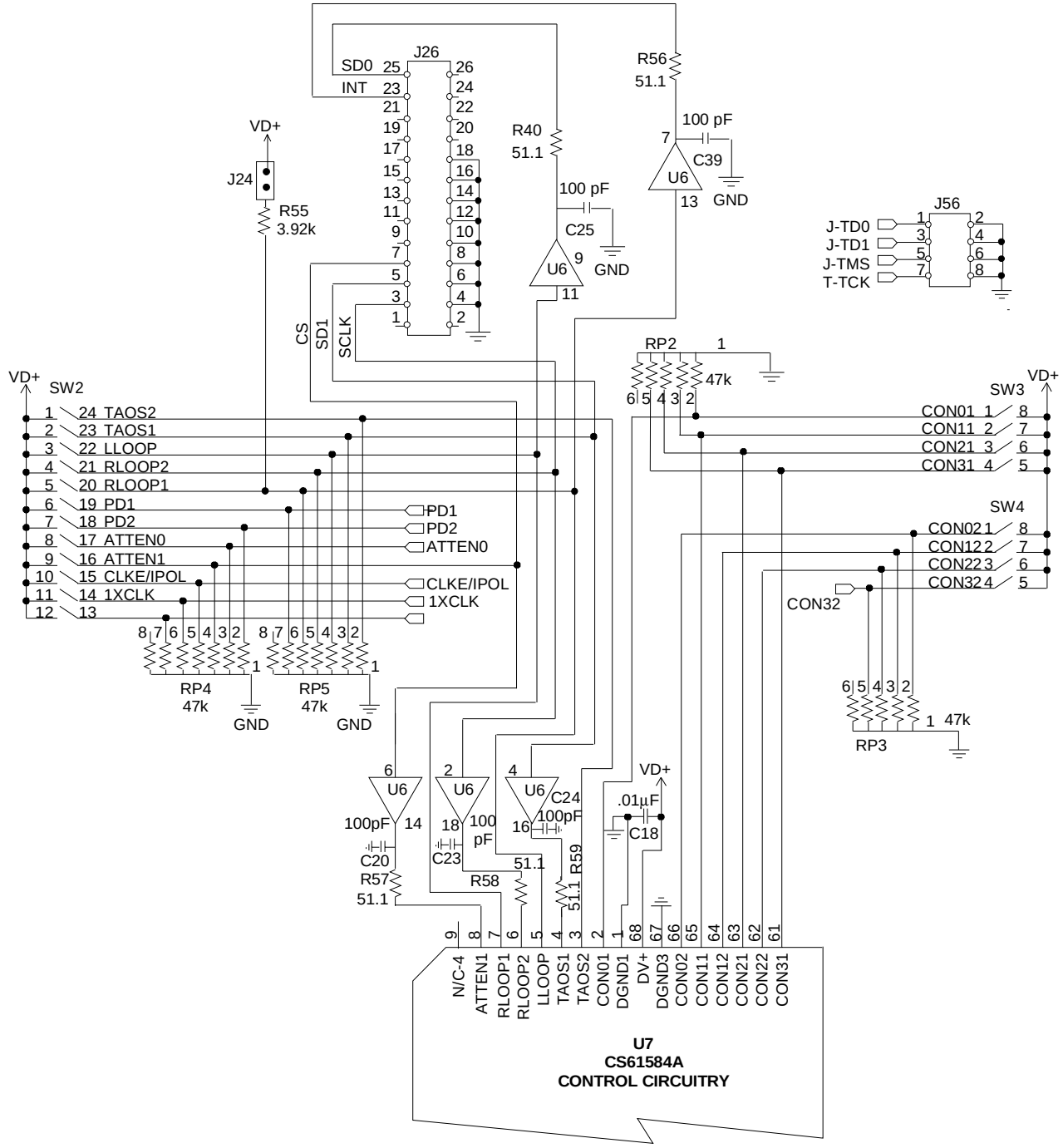


Figure 3. Control Circuitry

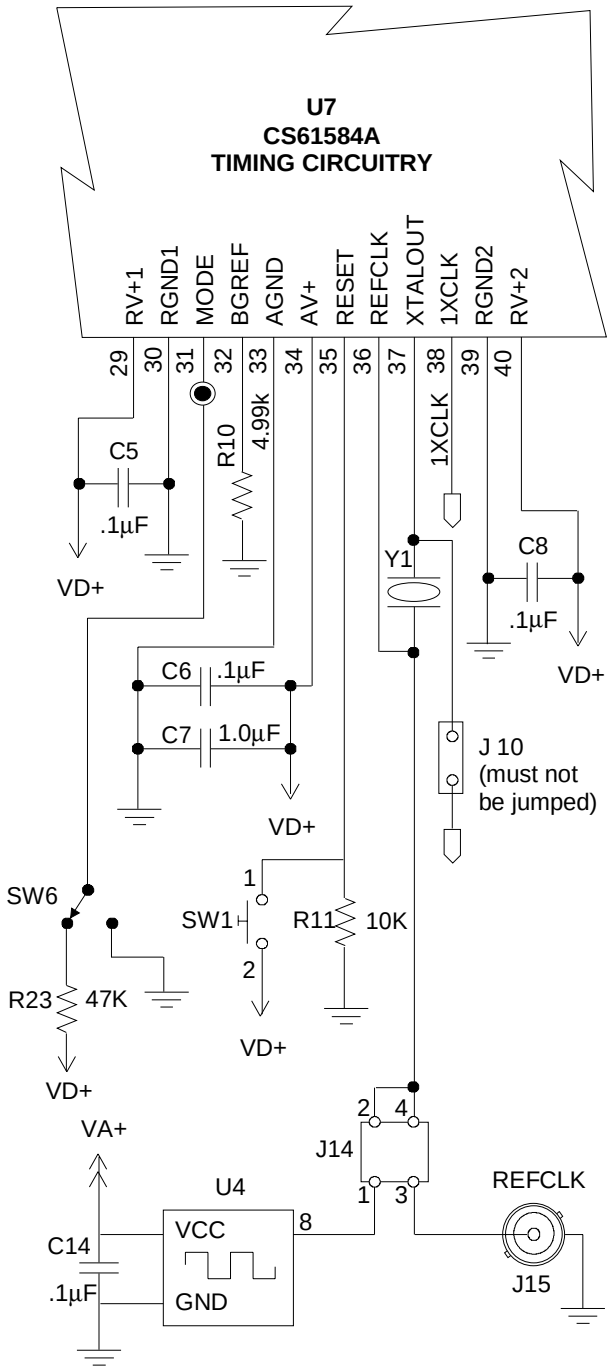


Figure 4. Timing Circuitry

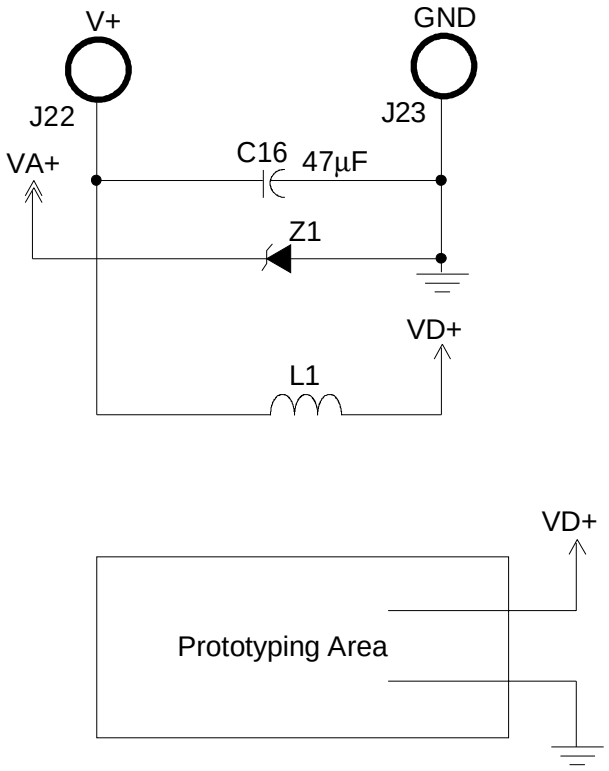


Figure 5. Common Circuitry

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