



CMOS High Voltage Logic – CD40106B

Hex Schmitt Trigger Inverter in bare die form

Rev 1.0
17/02/2023

Description

The CD40106B Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-} , show low variation with respect to temperature (typ. $0.0005V/^{\circ}C$ at $V_{CC} = 10V$), and hysteresis, $V_{T+} - V_{T-} \geq 0.2 V_{DD}$ is guaranteed. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features:

- Wide supply voltage range: 3V to 15V
- High noise immunity: $0.70 V_{DD}$ (typ.)
- Low power TTL compatibility:
 - Fan out of 2 driving 74L or 1 driving 74LS
- Hysteresis:
 - $0.40 V_{DD}$ (typ.)
 - $0.20 V_{DD}$ (guaranteed).

Ordering Information

The following part suffixes apply:

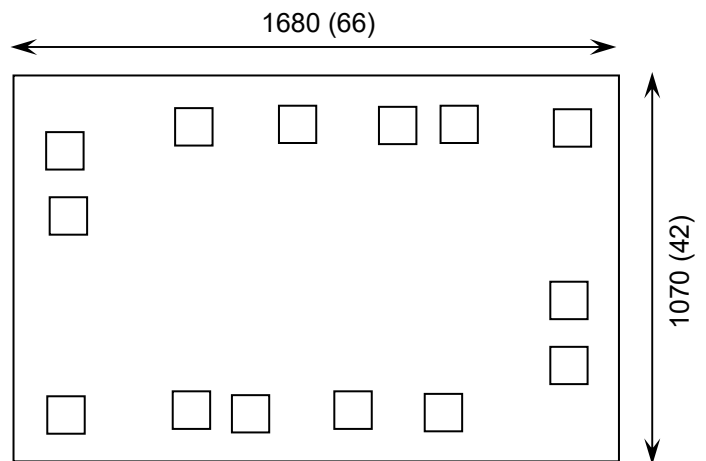
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in μm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness \leftrightarrow $350\mu m$ (14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1680 x 1070 66.14 x 42.13	μm mils
Minimum Bond Pad Size	105 x 105 4.713 x 4.13	μm mils
Die Thickness	350 (± 20) 13.78 (± 0.79)	μm mils
Top Metal Composition	Al 1%Si 1.1 μm	
Back Metal Composition	N/A – Bare Si	

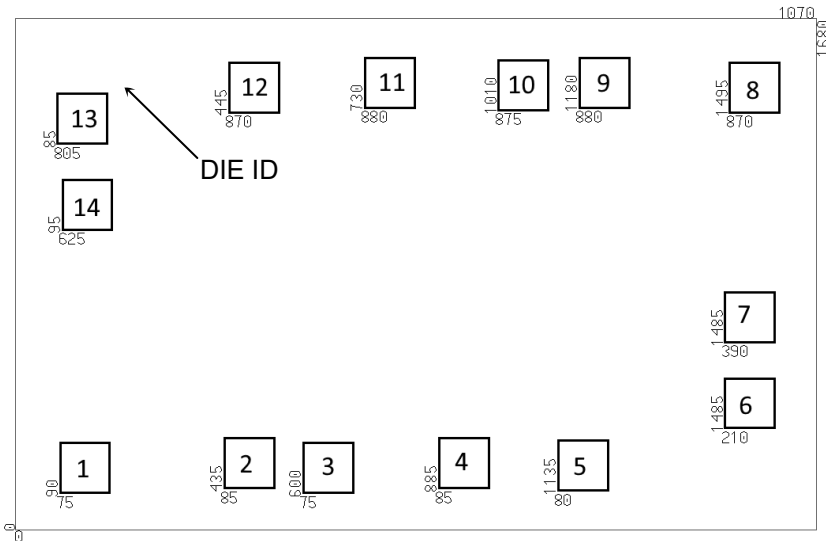




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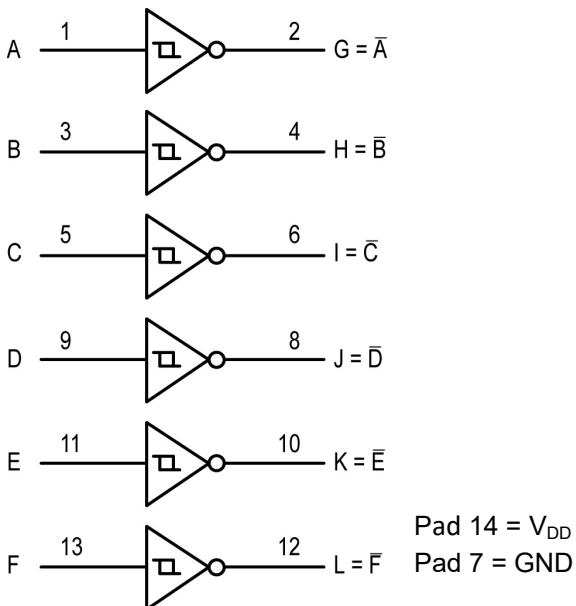
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (μm)	
		X	Y
1	A	90	75
2	$G = \bar{A}$	435	85
3	B	600	75
4	$H = \bar{B}$	885	85
5	C	1135	80
6	$I = \bar{C}$	1485	210
7	V_{SS}	1485	390
8	$J = \bar{D}$	1495	870
9	D	1180	880
10	$K = \bar{E}$	1010	875
11	E	730	880
12	$L = \bar{F}$	445	870
13	F	85	805
14	V_{DD}	95	625

CONNECT CHIP BACK TO V_{DD}

Logic Diagram



Function Table

INPUT	OUTPUT
L	H
H	L





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD}	-0.5 to $V_{CC} + 18$	V_{DC}
Input Voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V_{DC}
Recommended Operating V_{DD} range	V_{DD}	3 to 15	V
Maximum Power Dissipation ²	P_D	700	mW
Storage Temperature Range	T_{STG}	-65 to +150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions ($V_{SS} = 0V$ unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD}	3 to 15	V_{DC}
Input Voltage	V_{IN}	0 to V_{DD}	V_{DC}
Operating Temperature Range	T_A	-55 to +125	°C

DC Electrical Characteristics³ $T_A = 25^\circ C$ unless otherwise stated

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ³	
Maximum Quiescent Device Current	I_{DD}	5V		4	30	30	μA
		10V		8	60	60	
		15V		16	120	120	
Maximum Low-Level Output Voltage	V_{OL}	5V	$ I_{OUT} \leq 1\mu A$	0.05	0.05	0.05	V
		10V		0.05	0.05	0.05	
		15V		0.05	0.05	0.05	
Minimum High-Level Output Voltage	V_{OH}	5V	$ I_{OUT} \leq 1\mu A$	4.95	4.95	4.95	V
		10V		9.95	9.95	9.95	
		15V		14.95	14.95	14.95	
Minimum Negative-Going Threshold Voltage	V_{T-MIN}	5V	$V_{OUT} = 4.5V$	0.7	0.7	0.7	V
		10V	$V_{OUT} = 9V$	1.4	1.4	1.4	
		15V	$V_{OUT} = 13.5V$	2.1	2.1	2.1	
Maximum Negative-Going Threshold Voltage	V_{T-MAX}	5V	$V_{OUT} = 4.5V$	2.0	2.0	2.0	V
		10V	$V_{OUT} = 9V$	4.0	4.0	4.0	
		15V	$V_{OUT} = 13.5V$	6.0	6.0	6.0	
Minimum Positive - Going Threshold Voltage	V_{T+MIN}	5V	$V_{OUT} = 0.5V$	3.0	3.0	3.0	V
		10V	$V_{OUT} = 1V$	6.0	6.0	6.0	
		15V	$V_{OUT} = 1.5V$	9.0	9.0	9.0	

3. $-55^\circ C \leq T_J \leq +125^\circ C$





CMOS High Voltage Logic – CD40106B

Rev 1.0
16/07/2021

DC Electrical Characteristics $T_A = -55$ to $+125^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	GUARANTEED LIMITS			UNITS
				25°C	85°C	FULL RANGE ³	
Maximum Positive - Going Threshold Voltage	$V_{T+ MAX}$	5V	$V_{OUT} = 0.5V$	4.3	4.3	4.3	V
		10V	$V_{OUT} = 1V$	8.6	8.6	8.6	
		15V	$V_{OUT} = 1.5V$	12.9	12.9	12.9	
Minimum Hysteresis Voltage ($V_{T+} - V_{T-}$)	$V_{H MIN}$	5V		1.0	1.0	1.0	V
		10V		2.0	2.0	2.0	
		15V		3.0	3.0	3.0	
Maximum Hysteresis Voltage ($V_{T+} - V_{T-}$)	$V_{H MAX}$	5V		3.6	3.6	3.6	V
		10V		7.2	7.2	7.2	
		15V		10.8	10.8	10.8	
LOW Level Output Current ⁴	I_{OL}	5V	$V_{OUT} = 0.4V$	0.52	0.44	0.36	mA
		10V	$V_{OUT} = 0.5V$	1.30	1.10	0.90	
		15V	$V_{OUT} = 1.5V$	3.60	3.00	2.4	
HIGH Level Output Current ⁴	I_{OH}	5V	$V_{OUT} = 4.6V$	-0.52	-0.44	-0.36	mA
		10V	$V_{OUT} = 9.5V$	-1.30	-1.10	-0.90	
		15V	$V_{OUT} = 13.5V$	-3.60	-3.00	-2.4	
Input Current	I_{IN}	15V	$V_{IN} = 0V$	-0.30	-0.30	-1.0	μA
		15V	$V_{IN} = 15V$	0.30	0.30	1.0	

4. I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics⁵ $T_A = 25^\circ\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{k}\Omega$ unless otherwise stated

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	TYPICAL	MAX	UNITS
Maximum Propagation Delay, Input to Output (Figure 3)	t_{PLH}, t_{PHL}	5V	$t_r = t_f = 20\text{ns}$	220	400	ns
		10V		80	200	
		15V		70	160	
Maximum Output Rise and Fall Time (Figure 3)	t_{TLH}, t_{THL}	5V	$t_r = t_f = 20\text{ns}$	100	200	ns
		10V		50	100	
		15V		40	80	
Input Capacitance	C_{IN}	-	Any Input	5	7.5	pF
Power Dissipation Capacitance Per Gate ⁶	C_{PD}	-	-	TYPICAL		pF
				14		

5. Not production tested in die form, characterized by chip design.

6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.





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Typical Characteristics

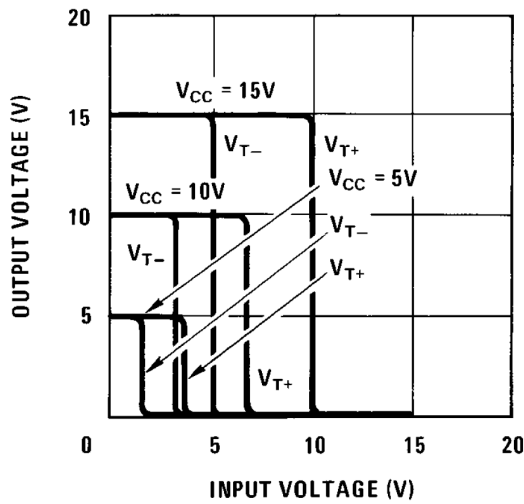


Figure 1 – Transfer Characteristics

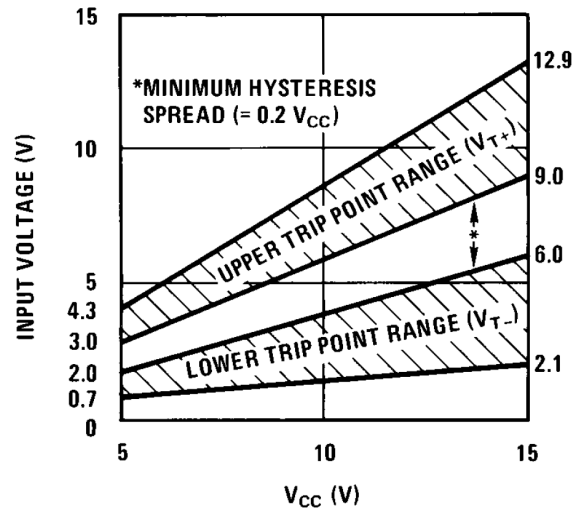


Figure 2 – Guaranteed Trip Point Range

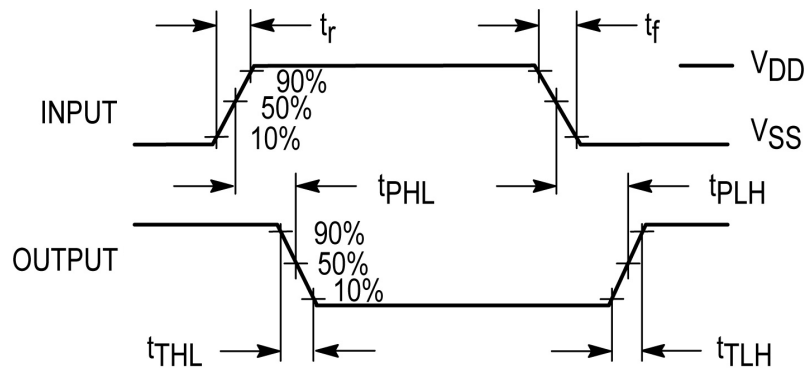


Figure 3 – Switching Time Waveform





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Typical Characteristics continued

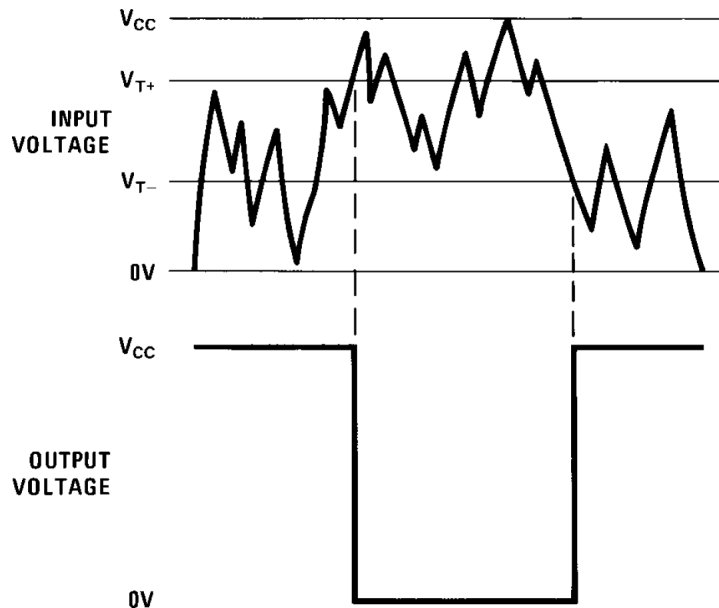


Figure 4 – Hysteresis Waveform

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