FAIRCHILD SEMICONDUCTOR™

October 1987
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CD4010C
Hex Buffers (Non-Inverting)

General Description

The CD4010C hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3V to 15V providing $V_{CC} \leq V_{DD}$. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

Features

- Wide supply voltage range: 3.0V to 15V
- Low power: 100 nW (typ.)
- High noise immunity: 0.45 V_{DD} (typ.)
- High current sinking: 8 mA (min.) at $V_O = 0.5V$ capability: and $V_{DD} = 10V$

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

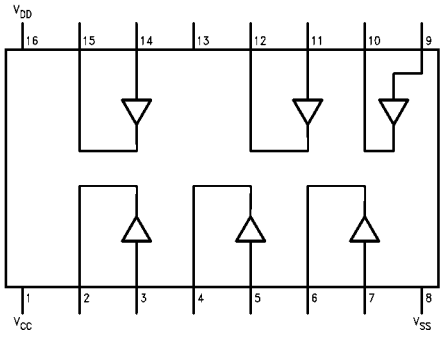
Ordering Code:

Order Number	Package Number	Package Description
CD4010CM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
CD4010CN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

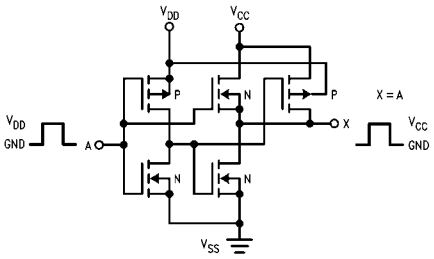
Connection Diagram

Pin Assignments for DIP and SOIC



Top View

Schematic Diagram



Hex COS/MOS to DTL or TTL converter (inverting).
Connect V_{CC} to DTL or TTL supply.
Connect V_{DD} to COS/MOS supply.

Absolute Maximum Ratings(Note 1)

Voltage at Any Pin (Note 2)	V_{SS} − 0.3V to V_{SS} +15.5V
Operating Temperature Range	−45°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
Operating Range (V_{DD})	V_{SS} + 3V to V_{SS} + 15V

Note 1: "Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits."

Note 2: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

DC Electrical Characteristics

Symbol	Characteristics	Test Conditions (Volts)		Limits							Units
				−40°C		+25°C			+85°C		
		V_O	V_{DD}	Min	Max	Min	Typ	Max	Min	Max	
I_{CC}	Quiescent Device		5		3		0.03	3		42	µA
	Current		10		5		0.05	5		70	µA
P_D	Quiescent Device		5		15		0.15	15		210	µW
	Dissipation/Package		10		50		0.5	50		700	µW
	Output Voltage		5		0.01		0	0.01		0.05	V
V_{OL}	LOW Level		10		0.01		0	0.01		0.05	V
V_{OH}	HIGH Level		5	4.99		4.99	5		4.95		V
			10	9.99		9.99	10		9.95		V
	Noise Immunity (All Inputs)										
V_{NL}		$V_O \geq 1.5$	5	1.6		1.5	2.25		1.4		V
		$V_O \geq 3.0$	10	3.2		3	4.5		2.9		V
V_{NH}		$V_O \geq 3.5$	5	1.4		1.5	2.25		1.5		V
		$V_O \geq 7.0$	10	2.9		3	4.5		3		V
	Output Drive Current	0.4	5	3.6		3			2.4		mA
I_DN	N-Channel (Note 3)	0.5	10	9.6		8			6.4		mA
I_DP	P-Channel (Note 3)	2.5	5	−1.5		−1.25			−1		mA
		9.5	10	−0.72		−0.6			−0.48		mA
I_{IN}	Input Current						10				pA

Note 3: I_DN and I_DP are tested one output at a time.

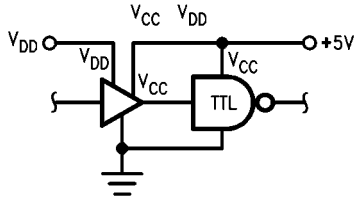
AC Electrical Characteristics (Note 4)

T_A= 25°c, C_L= 15 pF, unless otherwise noted. Typical Temperature coefficient for all values of V_{DD}= 0.3%/°C

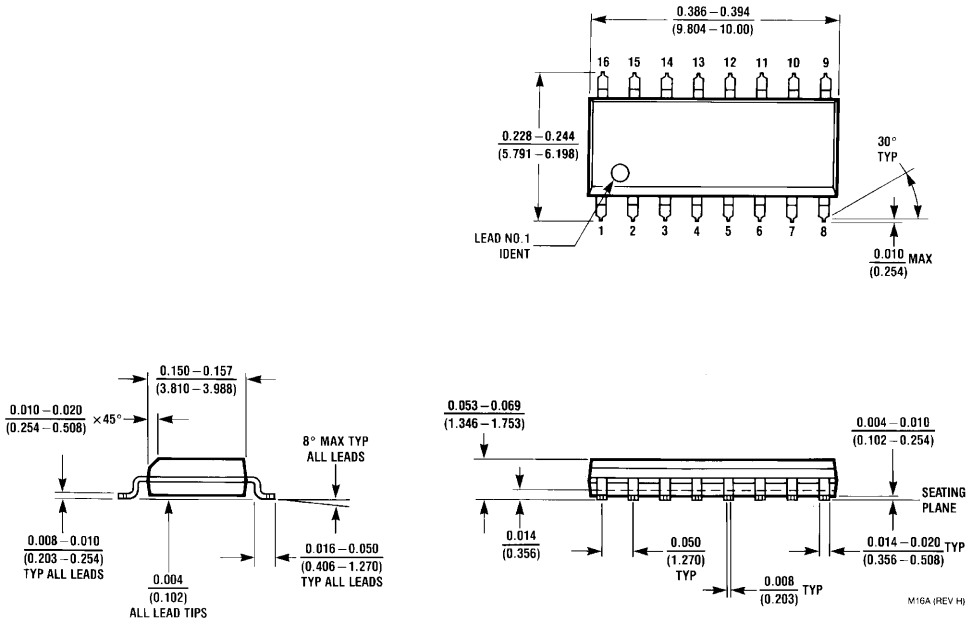
Symbol	Characteristics	Test Conditions		Limits			Units
			V_{DD} (Volts)	Min	Typ	Max	
t_{PHL}	Propagation Delay Time:	$V_{CC} = V_{DD}$	5	—	15	70	
t_{PLH}	HIGH-to-LOW Level (t_{PHL})		10	—	10	40	ns
		V_{DD} = 10V		—	10	35	
		V_{CC} = 5V					
	LOW-to-HIGH Level (t_{PLH})	$V_{CC} = V_{DD}$	5	—	50	100	
			10	—	25	70	
		V_{DD} = 10V		—	15	40	ns
		V_{CC} = 5V					
t_{THL}	Transition Time:	$V_{CC} = V_{DD}$	5	—	20	60	ns
t_{TLH}	HIGH-to-LOW Level (t_{THL})		10	—	16	50	
	LOW-to-HIGH Level (t_{TLH})	$V_{CC} = V_{DD}$	5	—	80	160	ns
			10	—	50	120	
	Input Capacitance (C_I)	Any Input		—	5	—	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

Typical Application

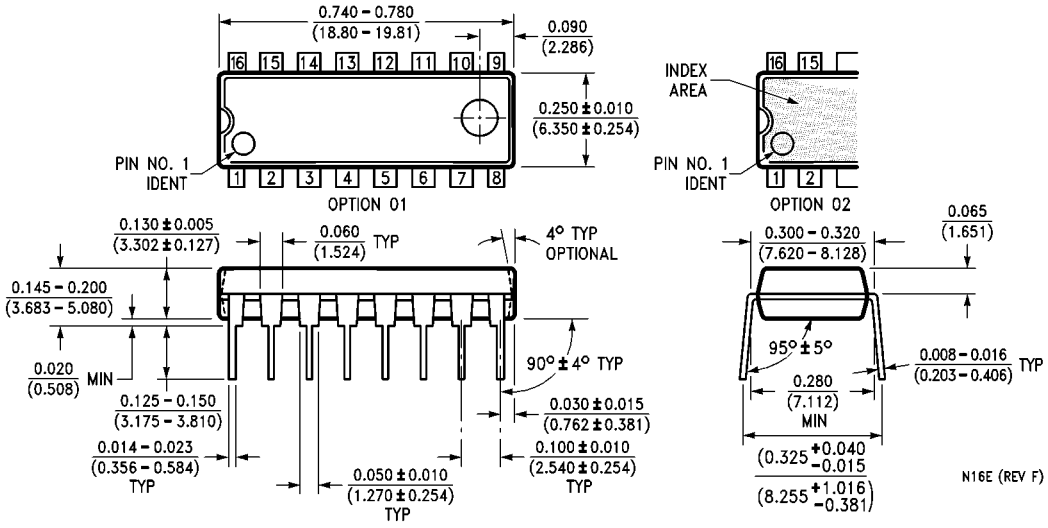


Physical Dimensions inches (millimeters) unless otherwise noted



16-Line Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E