



# Low-EMI Clock Generator for Intel® Mobile 133-MHz/3 SO-DIMM Chipset Systems

## Features

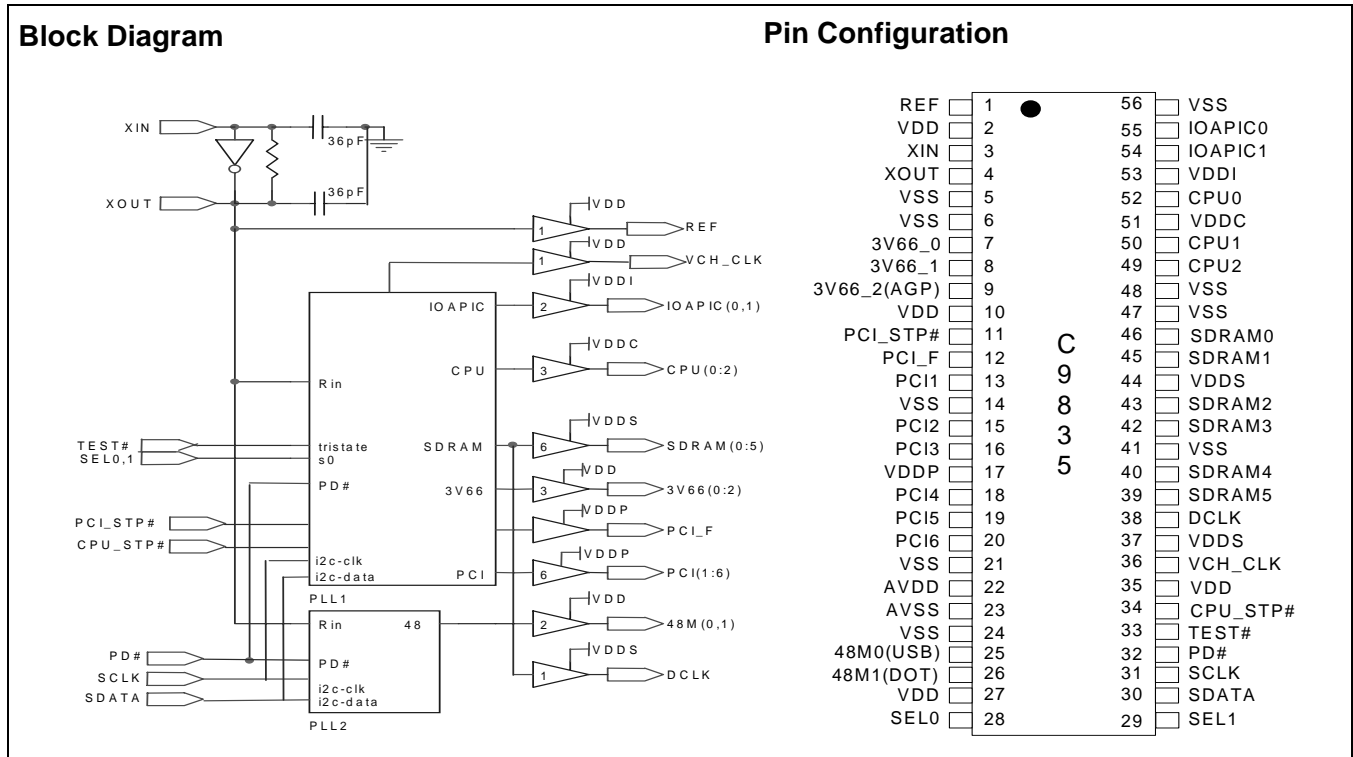
- Meets Intel's® Mobile 133.3MHz Chipset
- Three CPU Clocks (66.6/100/133.3 MHz, 2.5V)
- Six SDRAM Clocks, 1-DCLK (100/133.3 MHz, 3.3V)
- Seven PCI Clocks (33MHz, 3.3V), one free running
- Two IOAPIC clocks, synchronous to CPU clock (33.3 MHz, 2.5V)
- One REF Clock
- Two 48-MHz fixed non-SSCG clocks (USB and DOT)
- Three 3V66 clocks (66.6 MHz, 3.3V) ICH, HUBLINK, and AGP memory
- One selectable frequency for VCH video channel clock (48-MHz non-SSCG, 66.6-MHz CPU-SSCG, 3.3V)
- Power management using power-down, CPU stop, and PCI stop pins
- Three function select pins (include test-mode select)
- Cypress Spread Spectrum for best electromagnetic interference (EMI) reduction
- SMBUS support with readback
- 56-pin SSOP and TSSOP packages

Table 1. Function Table<sup>[1]</sup>

TEST#	SEL1	SEL0	CPU(0:2)	SDRAM(0:5) DCLK	3V66(0:2)	PCIF(1:6)	48M(0:1)	REF	IOAPIC(0:10)
0	X	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	X	1	TCLK/2	TCLK/2	TCLK/3	TCLK/6	TCLK/2	TCLK	TCLK/6
1	0	0	66.6	100.0 <sup>[2]</sup>	66.6	33.3	48	14.318	33.3
1	0	1	100.0	100.0 <sup>[2]</sup>	66.6	33.3	48	14.318	33.3
1	1	0	133.3	133.3	66.6	33.3	48	14.318	33.3
1	1	1	133.3	100.0 <sup>[2]</sup>	66.6	33.3	48	14.318	33.3

**Note:**

1. These are the frequencies that are selectable after power up using the SEL1 and SEL0 hardware pins. Other frequencies may be chosen using the devices SMBUS interface. See the expanded frequency for a complete listing of all of the available frequencies.
2. Will be set to 133MHz, when SMBUS Byte3, Bit 0 is set to logic 1.



**Pin Description<sup>[3]</sup>**

Pin	Name	PWR	Description
1	REF	VDD	3.3V 14.318 MHz clock output
3	XIN	VDD	<b>Oscillator buffer input.</b> Connect to a crystal or to an external clock.
4	XOUT	VDD	<b>Oscillator buffer output.</b> Connect to a crystal. Do not connect when an external clock is applied at X <sub>IN</sub> .
49, 50, 52	CPU(0:2)	VDDC	2.5V Host bus clock outputs
7, 8, 9	3V66(0:2)	VDD	3.3V Fixed 66.6 MHz clock outputs
12	PCI_F	VDDP	<b>3.3V PCI clock output.</b> This clock continues to run when PCI_STP# is at a logic low level.
13, 15, 16, 18, 19, 20	PCI (1:6)	VDDP	<b>3.3V PCI clock outputs.</b> These clocks synchronously stop in a low state when PCI_STP# is brought to a logic low level. They synchronously resume running when PCI_STP# is brought to a logic high state.
25, 26	48M(0,1)	VDD	3.3V Fixed 48 MHz clock outputs
36	VCH_CLK	VDD	<b>3.3V selectable 66.6 MHz or 48 MHz clock output to VCH.</b> Spread spectrum applies only when 66.6 MHz is selected. Select via SMBUS, byte 4 bit7.
34	CPU_STP#	VDD	<b>CPU0 stop clock control input.</b> Stops only CPU0 in a low state when asserted low. Using this pin to start and stop CPU0 clock insures synchronous (no short or long clocks) transitioning of this clock.
11	PCI_STP#	VDD	<b>PCI stop clock control input.</b> When this signal is at a logic low level (0), all PCI clocks (except PCI_F) stop at a logic low level. Using this pin to start and stop PCI clocks insures synchronous (no short or long clocks) transitioning of these clocks. This pin has no effect on the PCI_F clock.
28, 29	SEL(0,1)	VDD	<b>3.3V LVTTTL inputs for logic selection.</b> These pins have Internal pull-ups, typically 250k (range 200k to 800k).
30	SDATA	VDD	<b>Serial data input pin.</b> Conforms to the SMBUS specification of a Slave Receive/Transmit device. This pin is an input when receiving data. It is an open drain output when acknowledging or transmitting data. See 2-Wire SMBUS Control Interface on page 7.
31	SCLK	VDD	<b>Serial clock input pin.</b> Conforms to the SMBUS specification. See 2-Wire SMBUS Control Interface on page 7.
32	PD#	VDD	<b>3.3V LVTTTL-compatible input.</b> When held LOW, the device enters a power down mode. This pin has an Internal Pull-Up. See Power Management Functions on page 3.
33	TEST#	VDD	<b>3.3V LVTTTL compatible input for selecting test mode.</b> See <i>Table 1</i> .
38	DCLK	VDDS	<b>3.3V SDRAM feedback clock output.</b> See <i>Table 1</i> for frequency selection. See <i>Figure 4</i> for timing relationship.
39, 40, 42, 43, 45, 46	SDRAM(0:5)	VDDS	3.3V SDRAM clock outputs
54, 55	IOAPIC(0,1)	VDDI	2.5V IOAPIC clock outputs. See <i>Figure 4</i> for timing relationships.
37, 44	VDDS		3.3V Power for SDRAM and DCLK clock output buffers
17	VDDP		3.3V Power for PCI clock output buffers
53	VDDI		2.5V Power for IOAPIC clock output buffers
51	VDDC		2.5V Power for CPU clock output buffers
2, 10, 27, 35	VDD		3.3V Common power supply
22	AVDD		Analog power
23	AVSS		Analog ground
5, 6, 14, 21, 24, 41, 47, 48, 56	VSS		Common ground pins

**Note:**

3. A bypass capacitor (0.1μF) should be placed as close as possible to each positive power pin. If these bypass capacitors are not close to the pins their high-frequency filtering characteristic will be cancelled by the lead inductance of the traces.

**Table 2. Expanded Frequency Selection (MHz)<sup>[4, 5, 6]</sup>**

TEST#	ESEL	ESEL	SEL	SEL	CPU(0:2)	SDRAM(0:5), DCLK	3V66(0:2)	PCI_F, PCI(1:6)	Notes
1	0	0	0	0	66.7	100 <sup>[6]</sup>	66.6	33	0% extension (Default)
	0	0	0	1	100	100 <sup>[6]</sup>	66.6	33	
	0	0	1	0	133.3	133.3	66.6	33	
	0	0	1	1	133.3	100 <sup>[6]</sup>	66.6	33	
	0	1	0	0	70	105 <sup>[6]</sup>	70	35	5% extension
	0	1	0	1	105	105 <sup>[6]</sup>	70	35	
	0	1	1	0	140	140	70	35	
	0	1	1	1	140	105 <sup>[6]</sup>	70	35	
	1	0	0	0	73.3	110 <sup>[6]</sup>	73.3	36.6	10% extension
	1	0	0	1	110	110 <sup>[6]</sup>	73.3	36.6	
	1	0	1	0	146.7	146.7	73.3	36.6	
	1	0	1	1	146.7	110 <sup>[6]</sup>	73.3	36.6	
	1	1	0	0	80	120 <sup>[6]</sup>	80	40	20% extension
	1	1	0	1	120	120 <sup>[6]</sup>	80	40	
	1	1	1	0	160	160	80	40	
	1	1	1	1	160	120 <sup>[6]</sup>	80	40	

### Power Management Functions

Power management on this device is controlled by the PD#, CPU\_STP# and PCI\_STP# pins. When PD# is high (default) the device is in normal running mode and all signals are active.

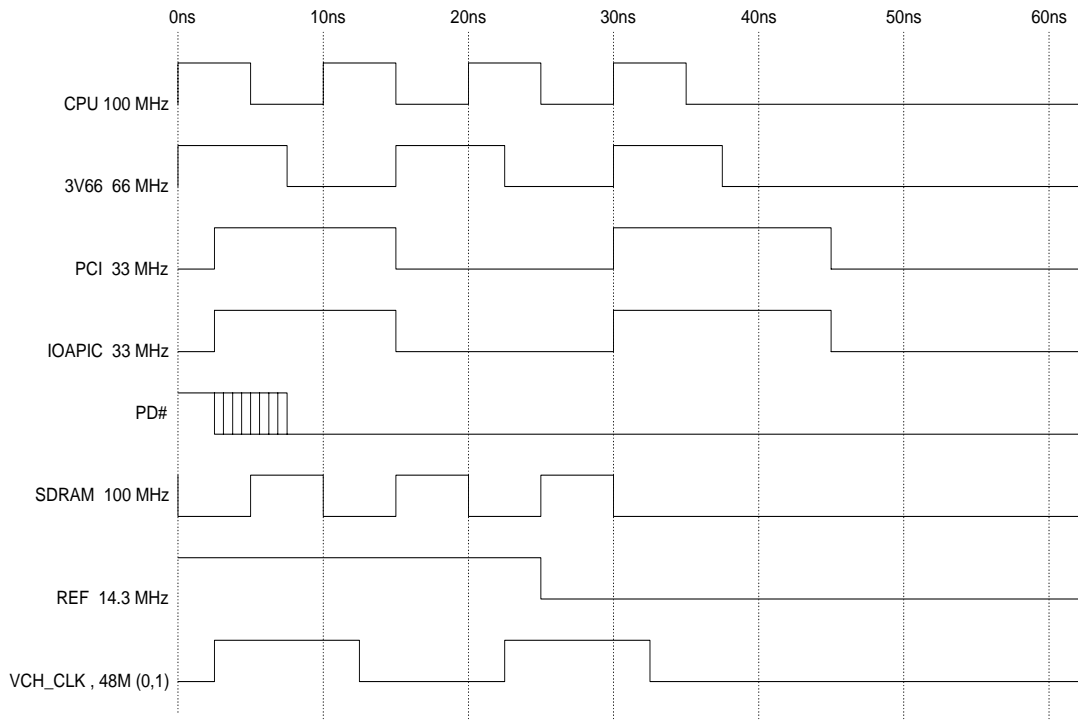
The PD# signal is used to bring all clocks to a low level in an orderly fashion prior to power (all except AVDD) being removed from the part. When PD# is asserted (forced) low, the device transitions to a shutdown (power down) mode and all power supplies (3.3V and 2.5V except for AVDD) may then be removed. When PD# is sampled low by two consecutive rising edges of the CPU clock, then all affected clocks are stopped

in a low state on their next high-to-low transition. The REF and USB clocks are stopped in a low state as soon as possible. When in power down (and before power is removed), all outputs are synchronously stopped in a low state (see *Figure 1*), all PLLs are shut off, and the crystal oscillator is disabled. When the device is shutdown, the I<sup>2</sup>C function is also disabled.

At power-up, using the PD# select pin, all clocks are started in such a manner as to guarantee a glitch-free operation, no partial clock pulses.

#### Notes:

4. Extended frequencies are only available via SMBUS interface. They are accessible via SMBUS Byte 5 bits 0,1.
5. 48M(0,1) clocks are constant at 48 MHz and REF is constant at 14.31818 MHz for all table selections.
6. Will be set to 133 MHz and boosted accordingly, when Byte3, Bit 0 is set to logic 1.

**Power Management Timing**

**Figure 1.**
**Table 3. Power Management Current**

Conditions	Maximum 2.5V Current Consumption ( $V_{DDC} = V_{DDI} = 2.625V$ )	Maximum 3.3V Current Consumption ( $V_{DD} = AV_{DD} = V_{DDS} = 3.465V$ )
Power-down (PD# = LOW)	≤ 1mA	≤ 1mA
CPU = 66 MHz @ max loads	60 mA	295 mA
CPU = 100 MHz @ max loads	75 mA	295 mA
CPU = 133 MHz @ max loads	90 mA	295 mA

When exiting the power-down mode, the application must supply power to the  $V_{DD}$  pins a minimum of 200 ms before releasing the PD# pin high to insure that an orderly startup will occur and that the initial clocks that the device produces are full and correctly compliant with data sheet specified phase relationships.

**CPU\_STP# Timing**

CPU\_STP# is an input to the clock generator. CPU\_STP# is asserted asynchronously by the external clock control logic and is internally synchronized to the external PCI\_F output. All other clocks will continue to run while the CPU0 clock is disabled. The CPU0 is always stopped in a low state and

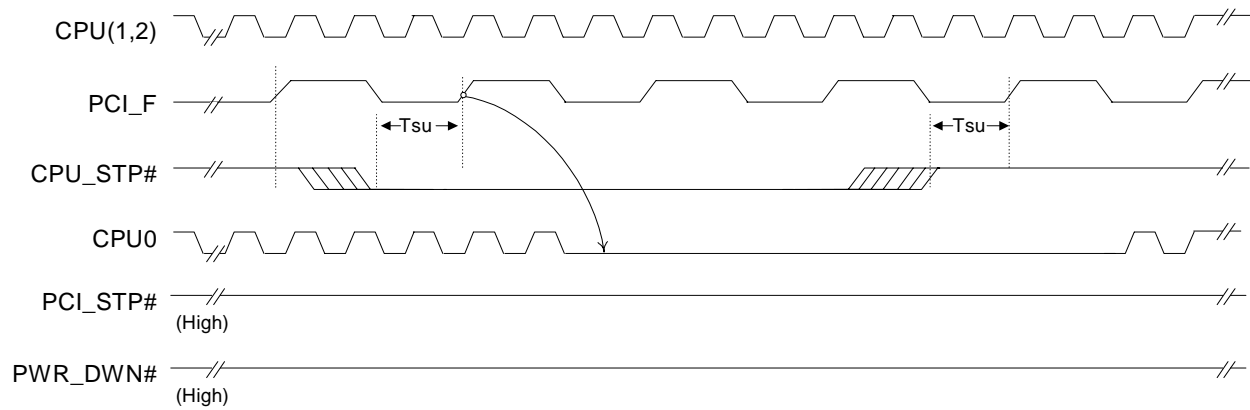
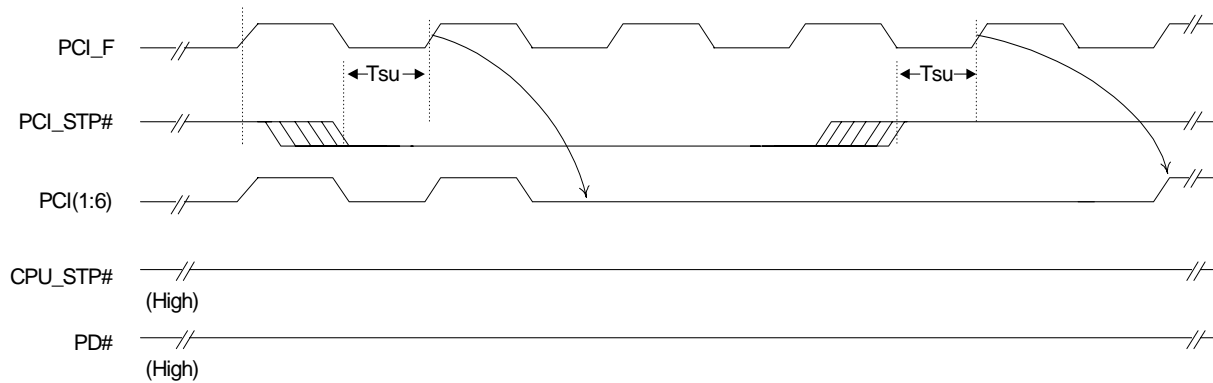
**Note:**

7. All internal timing is referenced to the CPU clock.
8. CPU\_STP# signal is an input signal that is made synchronous to free-running PCI\_F.
9. Diagrams shown with respect to 133 MHz. Similar operation when CPU is 100 MHz.

started in such a manner as to guarantee that the high pulse width is a full pulse. Only one rising edge of PCI\_F occurs after the clock control logic is switched for the CPU0 output to become enabled/disabled.

**PCI\_STP# Timing**

PCI\_STP# is an input to the clock generator and is made synchronous to the clock driver PCI\_F output. It is used to turn off the PCI clocks for low power operation. PCI clocks are stopped in a low state and started such that a full high pulse width is guaranteed. ONLY one rising edge of PCI\_F occurs after the clock control logic switched for the PCI outputs to become enabled/disabled.


**Figure 2. CPU\_STP# Timing Diagram**

**Figure 3. PCI\_STP# Timing Diagram**<sup>[[10,11,12,13,14]</sup>
**Note:**

10. All the internal timing is referenced to the CPU clock
11. PCI\_STP# signal is an input signal that must be made synchronous to PCI\_F output.
12. All other clocks continue to run undisturbed.
13. PD# is understood to in a high state.
14. Diagrams shown with respect to 133 MHz. Similar operation when CPU is 100 MHz

**Clock Phase**

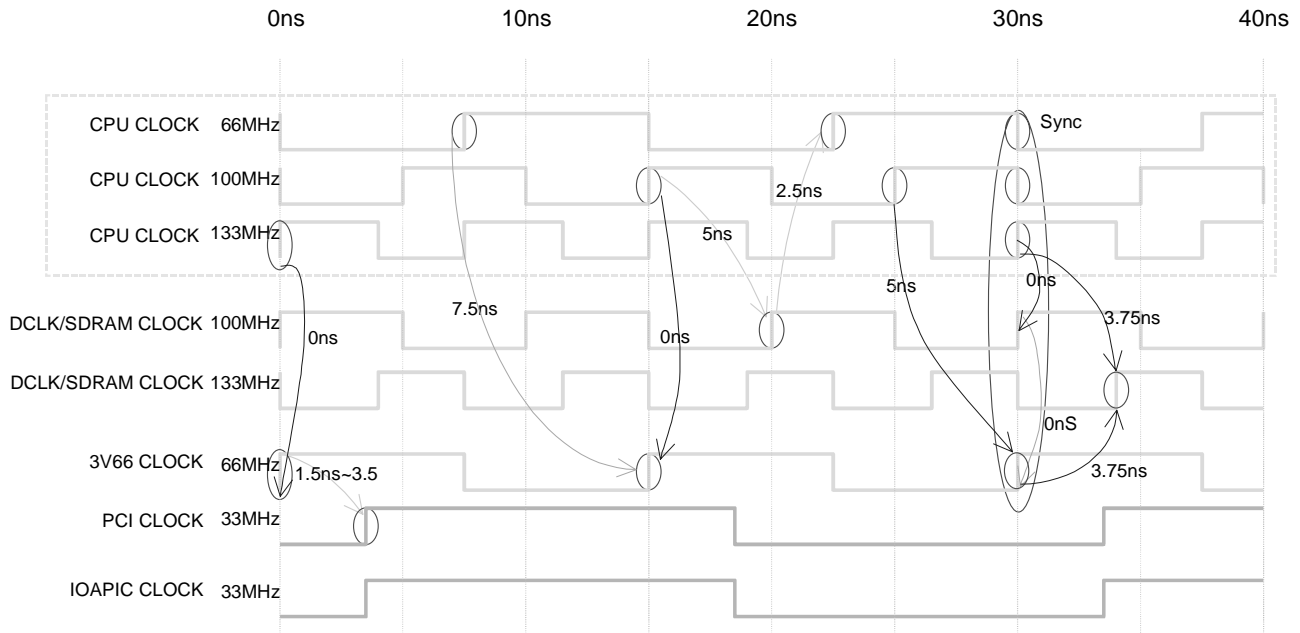


Figure 4.

Table 4. Group Timing Relationships and Tolerances

	CPU = 66.6 MHz, SDRAM = 100 MHz		
	Offset (ns)	Tolerance (ps)	Conditions
CPU to SDRAM/DCLK	2.5	500	
CPU to 3V66	7.5	500	180 degrees phase shift
SDRAM/DCLK to 3V66	0	500	When rising edges line up
3V66 to PCI	1.5–3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
48M (0,1)	Async	N/A	
	CPU = 100 MHz, SDRAM = 100 MHz		
	Offset (ns)	Tolerance (ps)	Conditions
CPU to SDRAM/DCLK	5	500	180 degrees phase shift
CPU to 3V66	5	500	CPU leads
SDRAM/DCLK to 3V66	0	500	When rising edges line up
3V66 to PCI	1.5–3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
48M (0,1)	Async	N/A	
	CPU = 133.3 MHz, SDRAM = 100 MHz		
	Offset(ns)	Tolerance(ps)	Conditions
CPU to SDRAM/DCLK	0	500	When rising edges line up
CPU to 3V66	0	500	
SDRAM/DCLK to 3V66	0	500	When rising edges line up
3V66 to PCI	1.5–3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
48M (0,1)	Async	N/A	

**Table 4. Group Timing Relationships and Tolerances** (continued)

	CPU = 66.6 MHz, SDRAM = 100 MHz		
	CPU = 133.3MHz, SDRAM = 133.3MHz		
	Offset(ns)	Tolerance(ps)	Conditions
CPU to SDRAM/DCLK	3.75	500	180 degrees phase shift
CPU to 3V66	0	500	
SDRAM/DCLK to 3V66	3.75	500	
3V66 to PCI	1.5–3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
48M (0,1)	Async	N/A	

## 2-Wire SMBUS Control Interface

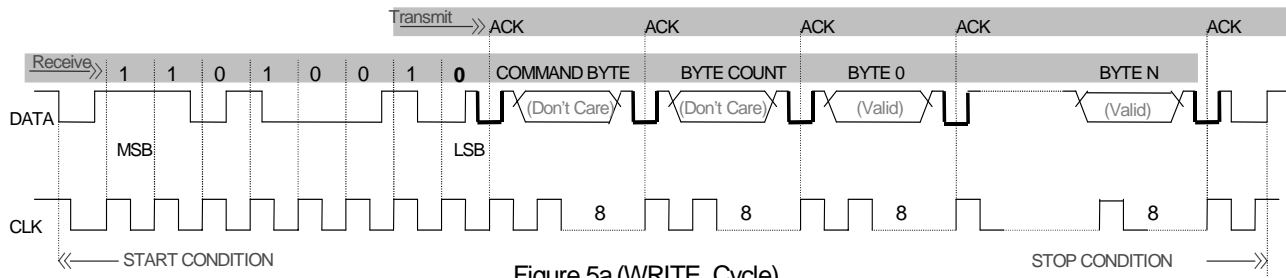
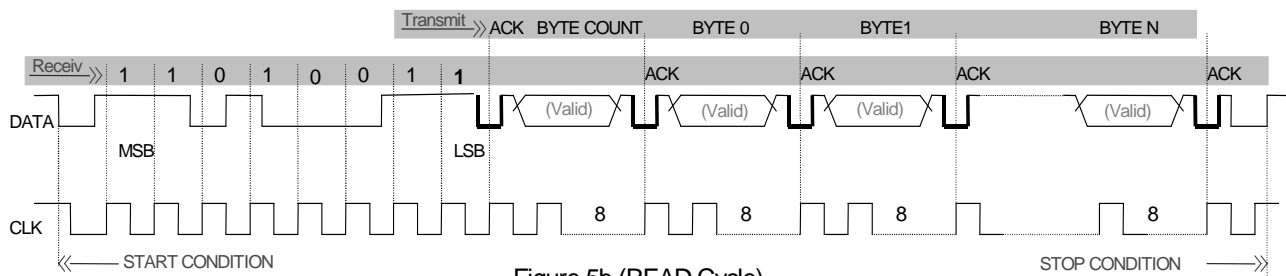
The 2-wire control interface implements a read/write slave only interface according to SMBus specification. (See Figure 5 below). The device can be read back by using standard SMBUS command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/s (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK

is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is an 8-bit address. The LSB address Byte = 0 in write mode.

The device will respond to transfers of 10 bytes (max) of data. The device will generate an acknowledge (low) signal on SDATA following reception of each byte. Data is transferred MSB first at a max rate of 100kbits/s. This device will also respond to a D3 address which sets it in a read mode. It will not respond to any other control interface conditions, and previously set control registers are retained.

When a clock driver is placed in power down mode, the SMBUS signals SDATA and SCLK must be tri-stated. In power down, the device retains all SMBUS programming information.


**Figure 5a (WRITE Cycle)**

**Figure 5b (READ Cycle)**
**Figure 5. SMBus Communications Waveforms**

## Serial Control Registers

Following the acknowledge of the Address Byte, two additional bytes must be sent:

- 1) "**Command Code**" byte
- 2) "**Byte Count**" byte.

Although the data (bits) in these two bytes are considered "don't care," they must be sent and will be acknowledged. After the Command Code and the Byte Count have been acknowledged, the sequence (Byte 0, Byte 1, and Byte 2) described below will be valid and acknowledged.

### Byte 0: CPU Clock Register (1 = Enable, 0 = Disable)

Bit	@Pup <sup>[15]</sup>	Pin# <sup>[16]</sup>	Description
7	1	36	VCH_CLK
6	1	49	CPU2
5	1	50	CPU1
4	1	52	CPU0
3	0	–	Spread Spectrum ( 1 = enabled)
2	1	26	48M1(DOT)
1	1	25	48M0(USB)
0	0	–	Reserved. Set to 0

### Byte 1: SDRAM Clock Register (1 = Enable, 0 = Disable)

Bit	@Pup <sup>[15]</sup>	Pin# <sup>[16]</sup>	Description
7	0	–	Reserved. Set to 0
6	0	–	Reserved. Set to 0
5	1	39	SDRAM5
4	1	40	SDRAM4
3	1	42	SDRAM3
2	1	43	SDRAM2
1	1	45	SDRAM1
0	1	46	SDRAM0

### Byte 2: 3C66 Clock Register (1 = Enable, 0 = Disable)

Bit	@Pup <sup>[15]</sup>	Pin# <sup>[16]</sup>	Description
7	1	9	3V66_2 (AGP)
6	1	8	3V66_1
5	1	7	3V66_0
4	0	–	Reserved. Set to 0
3	0	–	Reserved. Set to 0
2	0	–	Reserved. Set to 0
1	0	–	Reserved. Set to 0
0	0	–	Reserved. Set to 0

### Byte 3: PCI Register (1 = Enable, 0 = Disable)

Bit	@Pup <sup>[17]</sup>	Pin# <sup>[18]</sup>	Description
7	0	–	Reserved. Set to 0
6	1	20	PCI6
5	1	19	PCI5
4	1	18	PCI4
3	1	16	PCI3
2	1	15	PCI2
1	1	13	PCI1
0	0	–	SDRAM 133- MHz Mode Enable. Default is disabled = "0," enabled = "1"

**Notes:**

15. The @Pup column gives the default state at power-up.
16. The Pin# column lists the relevant pin number where applicable.

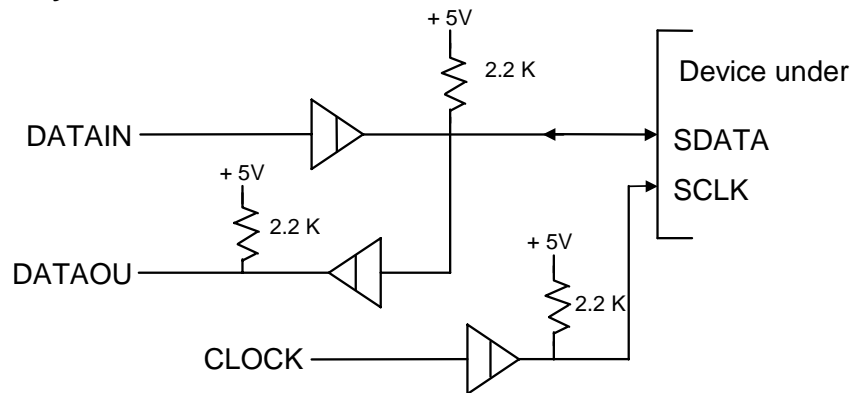


**Byte 4: VCH Clock Register (1 = Enable, 0 = Disable)**

Bit	@Pup <sup>[17]</sup>	Pin# <sup>[18]</sup>	Description
7	0	36	VCH_CLK SSC Mode Enable "0" = 48 MHz (non-SSCG) "1" = 66.6 MHz (SSCG applicable when Byte 0, Bit3 = 1)
6	0	–	Reserved. Set to 0
5	0	–	Reserved. Set to 0
4	0	–	Reserved. Set to 0
3	0	–	Reserved. Set to 0
2	0	–	Reserved. Set to 0
1	0	–	Reserved. Set to 0
0	0	–	Reserved. Set to 0

**Byte 5: SSCG Control Register (1 = Enable, 0 = Disable)**

Bit	@Pup <sup>[17]</sup>	Pin# <sup>[18]</sup>	Description
7	0	–	Spread Mode (0 = down, 1 = center)
6	0	–	Selects spread bandwidth. See Table 5.
5	0	–	Selects spread bandwidth. See Table 5.
4	0	–	Reserved. Set to 0
3	0	–	Reserved. Set to 0
2	0	–	Reserved. Set to 0
1	0	–	ESEL1 Expanded Freq. Selection MSB, See Table 2.
0	0	–	ESEL0 Expanded Freq. Selection LSB, See Table 2.

**SMBus Test Circuitry**

**Figure 6. SMBUS Test Circuitry<sup>[19]</sup>**
**Spread Spectrum Clock Generation (SSCG)**

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing EMI radiation generated by repetitive digital signals, mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore distributing an even amount of energy over a wider spectrum. This technique is achieved by modulating the clock either down or around the center (see Figure 7 below) of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting SMBUS Byte0, Bit3 = 1. The default of the device at

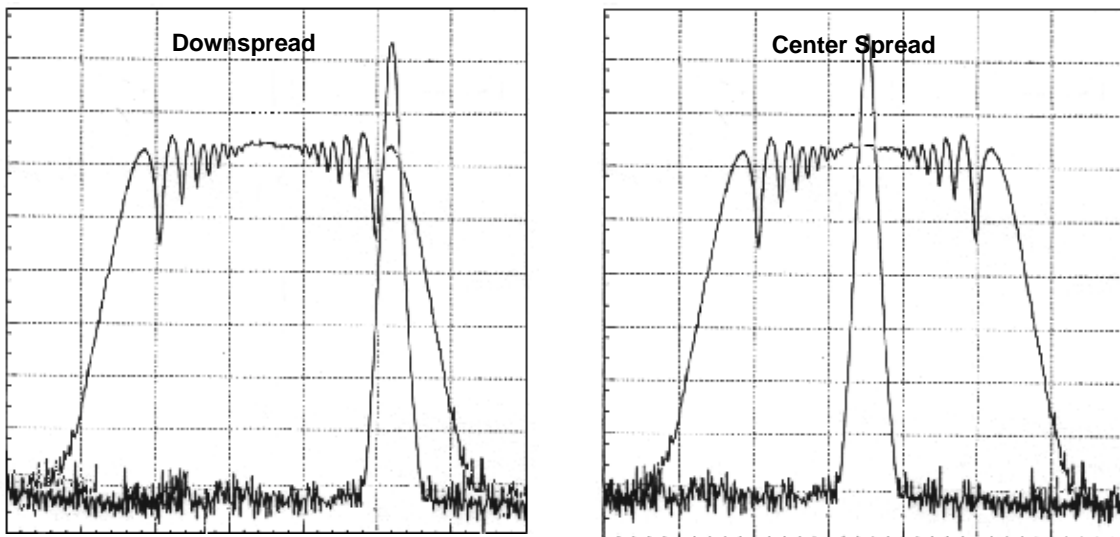
**Notes:**

17. The @Pup column gives the default state at power-up

18. The Pin# column lists the relevant pin number where applicable.

power up keeps the Spread Spectrum disabled, it is therefore, important to have SMBUS accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by SST(0:2) in SMBUS Byte 5, bits 5, 6, and 7. See Table 7 below.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by ½ of the total spread % (e.g., assuming the center frequency is 100 MHz in non-spread mode; when down spread of –0.5% is enabled, the center frequency shifts to 99.75 MHz.). In Center Spread Mode, the center frequency remains the same as in non-spread mode.


**Figure 7. Spread Spectrum**
**Spread Spectrum Selection Tables**
**Table 5. (I<sup>2</sup>C BYTE 5 Bit 7=0), Down Spread**

I <sup>2</sup> C Byte 5 Bit		Spread %
6	5	
0	0	-0.5
0	1	-0.7
1	0	-1.0
1	1	-1.5

**Table 6. (I<sup>2</sup>C BYTE 5 Bit 7=0), Center Spread**

I <sup>2</sup> C Byte 5 Bit		Spread %
6	5	
0	0	±0.25
0	1	±0.35
1	0	±0.5
1	1	±0.75

**Note:**

 19. Buffer is 7407 with V<sub>CC</sub>@ 5.0V.

## Maximum Ratings

Maximum Input Voltage Relative to  $V_{SS}$ : .....  $V_{SS} - 0.3V$   
 Maximum Input Voltage Relative to  $V_{DD}$ : .....  $V_{DD} + 0.3V$   
 Storage Temperature: .....  $-65^{\circ}C$  to  $+150^{\circ}C$   
 Operating Temperature: .....  $0^{\circ}C$  to  $+85^{\circ}C$   
 Maximum ESD Protection ..... 2 KV  
 Maximum Power Supply: ..... 5.5V

This device contains circuitry that protects the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range:

$$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

## DC Parameters $V_{DD} = V_{DDS} = 3.3V \pm 5\%$ , $V_{DDC} = V_{DDI} = 2.5V \pm 5\%$ , $T_A = 0^{\circ}C$ to $+70^{\circ}C$ <sup>[20]</sup>

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
VIL1	Input Low Voltage	Note 21			1.0	V
VIH1	Input High Voltage		2.0			V
VIL2	Input Low Voltage	Note 22			1.0	V
VIH2	Input High Voltage		2.2			V
IIL1	Input Low Current (@ $V_{IL} = V_{SS}$ )	For internal pull-up resistors <sup>[23]</sup>			-20	$\mu A$
IIH1	Input High Current (@ $V_{IH} = V_{DD}$ )				20	$\mu A$
Ioz	Three-state leakage Current				10	$\mu A$
Idd3.3V	Dynamic Supply Current				295	mA
Idd2.5V	Dynamic Supply Current	CPU @ 66 MHz			60	mA
		CPU @ 100 MHz			75	mA
		CPU @ 133 MHz			90	mA
Ipd3.3V	Power Down Supply Current	PD# = "0"			1	mA
Ipd2.5V	Power Down Supply Current	PD# = "0"			1	mA
Cin	Input pin capacitance				5	pF
Cout	Output pin capacitance				6	pF
Lpin	Pin inductance				7	nH
Cxtal	Crystal pin capacitance	Measured from Pin to Ground <sup>[24]</sup>	34	36	38	pF
$V_{BIAS}$	Crystal DC Bias Voltage		$0.3V_{DD}$	$V_{DD}/2$	$0.7V_{DD}$	V
Txs	Crystal Startup time	From stable 3.3V power supply.			40	$\mu s$

**Table 7. Maximum Output Load**

Clock Name	Max Load (in pF)
CPU(0:2), IOAPIC(0:1), REF, 48M0 (USB), VCH_CLK	20
PCI(0:6), SDRAM(0:5), DCLK, 3V66(0:2)	30
48M1 (DOT)	15

**Notes:**

20. All outputs loaded per Table 7.
21. Applicable to input signals : SEL(0:1), PD# (pull-up).
22. Applicable to SDATA and SCLK.
23. Internal pull-up and pull-down resistors affect this current.
24. See Applications data that is presented later in this datasheet on crystal interfacing.

**AC Parameters**

Parameter	Description	133 MHz Host		100 MHz Host		66 MHz Host		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>CPU</b>								
TPeriod	CPU(0:2) period <sup>[25,26]</sup>	7.5	8.0	10.0	10.5	15.0	15.5	ns
THIGH	CPU(0:2) high time <sup>[30]</sup>	1.87		3.0		5.2		ns
TLOW	CPU(0:2) low time <sup>[31]</sup>	1.67		2.8		5.0		ns
Tr / Tf	CPU(0:2) rise and fall times <sup>[27]</sup>	0.4	1.6	0.4	1.6	0.4	1.6	ns
TSKEW	CPU0 to any CPU Skew <sup>[26,29]</sup>		150		150		150	ps
TCCJ	CPU(0:2) Cycle to Cycle Jitter <sup>[26,29]</sup>		250		250		250	ps
<b>SDRAM</b>								
TPeriod	SDRAM(0:5) 100 MHz and DCLK period <sup>[25,26]</sup>	10.0	10.5	10.0	10.5	10.0	10.5	ns
THIGH	SDRAM(0:5) 100 MHz and DCLK high time <sup>[30]</sup>	3.0		3.0		3.0		ns
TLOW	SDRAM(0:5) 100 MHz and DCLK low time <sup>[31]</sup>	2.8		2.8		2.8		ns
Tr / Tf	SDRAM(0:5) 100 MHz and DCLK rise and fall times <sup>[27]</sup>	0.4	1.6	0.4	1.6	0.4	1.6	ns
TSKEW	SDRAM(0:5) 100 MHz and DCLK Skew <sup>[26,29]</sup>		250		250		250	ps
TCCJ	SDRAM(0:5) 100 MHz, DCLK Cycle to Cycle Jitter <sup>[26,29]</sup>		250		250		250	ps
<b>IOAPIC</b>								
TPeriod	IOAPIC(0,1) period <sup>[25,26]</sup>	30.0		30.0		30.0		ns
THIGH	IOAPIC(0,1) high time <sup>[30]</sup>	12.0		12.0		12.0		ns
TLOW	IOAPIC(0,1) low time <sup>[31]</sup>	12.0		12.0	N/S	12.0		ns
Tr / Tf	IOAPIC(0,1) rise and fall times <sup>[27]</sup>	0.4	1.6	0.4	1.6	0.4	1.6	ns
TSKEW	IOAPIC(0,1) Skew <sup>[26,29]</sup>		250		250		250	ps
TCCJ	IOAPIC(0,1) Cycle to Cycle Jitter <sup>[26,29]</sup>		500		500		500	ps
<b>3V66</b>								
TPeriod	3V66-(0:2) period <sup>[25,26]</sup>	15.0	16.0	15.0	16.0	15.0	16.0	ns
THIGH	3V66-(0:2) high time <sup>[30]</sup>	5.25		5.25		5.25		ns
TLOW	3V66-(0:2) low time <sup>[31]</sup>	5.05		5.05		5.05		ns
Tr / Tf	3V66-(0:2) rise and fall times <sup>[28]</sup>	0.5	2.0	0.5	2.0	0.5	2.0	ns
TSKEW	(Any 3V66) to (any 3V66) Skew <sup>[26,29]</sup>		175		175		175	ps
TCCJ	3V66-(0:2) Cycle to Cycle Jitter <sup>[26,29]</sup>		500		500		500	ps
<b>PCI_F</b>								
TPeriod	PCI(_F, 1:6) period <sup>[25,26]</sup>	30.0		30.0		30.0		ns
THIGH	PCI(_F, 1:6) high time <sup>[30]</sup>	12.0		12.0		12.0		ns

**Notes:**

25. This parameter is measured as an average over 1us duration, with a crystal center frequency of 14.31818 MHz.  
26. All outputs loaded per Table 6. Probes are placed on the pins and taken at 1.5V levels for 3.3V signals and at 1.25V for 2.5V signals (see Figure 8).  
27. Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 0.4V and 2.0V for 2.5V signals (see Figure 8).  
28. Measured from when both SEL1 and SEL0 are switched to high (enable).  
29. This measurement is applicable with Spread ON or Spread OFF.  
30. Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals (see Figure 8).  
31. Probes are placed on the pins, and measurements are acquired at 0.4V.

**AC Parameters** (continued)

Parameter	Description	133 MHz Host		100 MHz Host		66 MHz Host		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
TLOW	PCI(_F, 1:6) low time <sup>[31]</sup>	12.0		12.0		12.0		ns
Tr / Tf	PCI(_F, 1:6) rise and fall times <sup>[27]</sup>	0.5	2.0	0.5	2.0	0.5	2.0	ns
TSKEW	(Any PCI) to (Any PCI) Skew <sup>[26,29]</sup>		500		500		500	ps
TCCJ	PCI(_F, 1:6) Cycle to Cycle Jitter <sup>[26,29]</sup>		500		500		500	ps
<b>DOT and USB</b>								
TPeriod	DOT and USB (48M[0,1]) period (conforms to +167 ppm max) <sup>[25,26]</sup>	20.8299	20.8333	20.8299	20.8333	20.829	20.833	ns
Tr / Tf	DOT and USB rise and fall times <sup>[27]</sup>	1.0	4.0	1.0	4.0	1.0	4.0	ns
TCCJ	DOT and USB Cycle to Cycle Jitter <sup>[26,29]</sup>		500		500		500	ps
TCCJ	VCH_CLK Cycle to Cycle Jitter <sup>[26]</sup>		250		250		250	ps
<b>REF</b>								
TPeriod	REF period <sup>[25,26]</sup>	69.8413	71.0	69.8413	71.0	69.8413	71.0	ns
Tr / Tf	REF rise and fall times <sup>[27]</sup>	1.0	4.0	1.0	4.0	1.0	4.0	ns
TCCJ	REF Cycle to Cycle Jitter <sup>[26]</sup>		1000		1000		1000	ps
tpZL, tpZH	Output enable delay (all outputs) <sup>[28]</sup>	1.0	10.0	1.0	10.0	1.0	10.0	ns
tpLZ, tpHZ	Output disable delay (all outputs) <sup>[33]</sup>	1.0	10.0	1.0	10.0	1.0	10.0	ns
tstable	All clock stabilization from power-up <sup>[32]</sup>		3		3		3	ms
Tduty	Duty cycle for all outputs <sup>[34]</sup>	45	55	45	55	45	55	%

**Notes:**

32. The time specified is measured from when all V<sub>DD</sub>'s reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within the specifications.
33. Measured from when both SEL1 and SEL0 are switched to low (disable).
34. Device designed for Typical Duty Cycle of 50%.

**Output Buffer Characteristics**
**Table 8. CPU, IOAPIC**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
IOH <sub>1</sub>	Pull-up Current	Vout = VDDC - 0.5V (or VDDI - 0.5V)	-15	-31	-51	mA
IOH <sub>2</sub>	Pull-up Current	Vout = 1.2V	-26	-58	-101	mA
IOL <sub>1</sub>	Pull-down Current	Vout = 0.4V	12	24	40	mA
IOL <sub>2</sub>	Pull-down Current	Vout = 1.2V	27	56	93	mA
Z0	Output Impedance		13.5		45	Ω

**Table 9. PCI, 3V66, VCH**

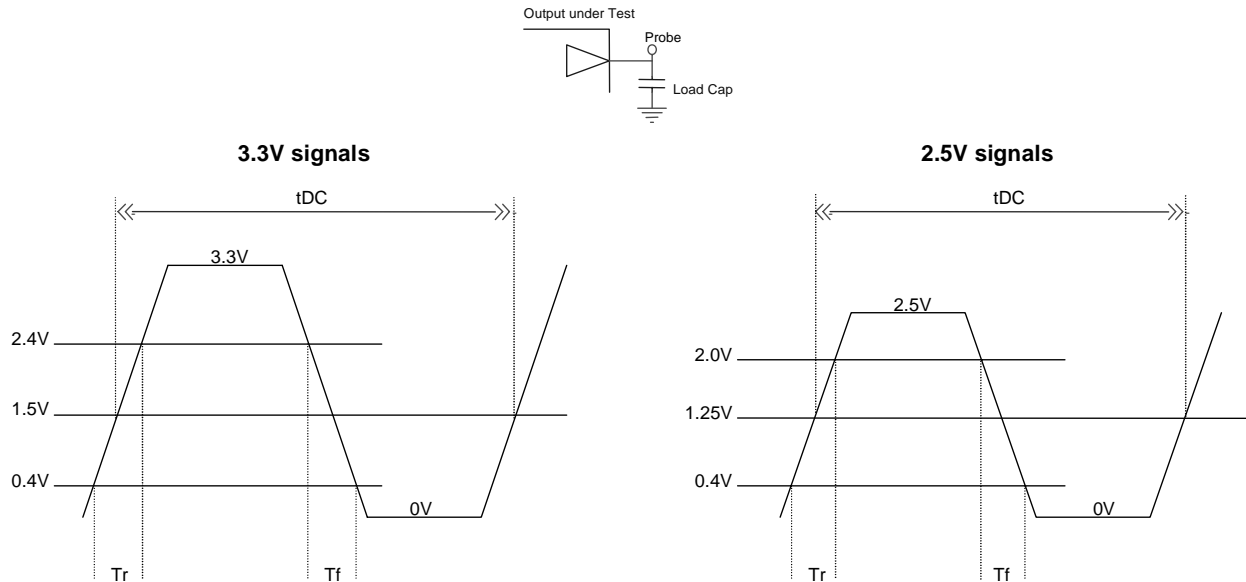
Parameter	Description	Conditions	Min.	Typ.	Max.	Units
IOH <sub>1</sub>	Pull-up Current	Vout = VDD - 0.5V	-20	-25	-33	mA
IOH <sub>2</sub>	Pull-up Current	Vout = 1.5V	-30	-54	-184	mA
IOL <sub>1</sub>	Pull-down Current	Vout = 0.4V	9.4	18	38	mA
IOL <sub>2</sub>	Pull-down Current	Vout = 1.5V	28	55	148	mA
Z0	Output Impedance		12		55	Ω

**Table 10. 48M0(USB), 481(DOT), REF**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
IOH <sub>1</sub>	Pull-up Current	Vout = VDD - 0.5V	-12	-16	-28	mA
IOH <sub>2</sub>	Pull-up Current	Vout = 1.5V	-27	-43	-92	mA
IOL <sub>1</sub>	Pull-down Current	Vout = 0.4V	9	13	27	mA
IOL <sub>2</sub>	Pull-down Current	Vout = 1.5V	26	39	79	mA
Z0	Output Impedance		20		60	Ω

**Table 11. SDRAM** (V<sub>DD</sub> = V<sub>DDS</sub> = 3.3V ± 5%, V<sub>DDC</sub> = V<sub>DDI</sub> = 2.5V ± 5%, T<sub>A</sub> = 0°C to 70°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
IOH <sub>1</sub>	Pull-up Current	Vout = VDD - 0.5V	-28	-40	-60	mA
IOH <sub>2</sub>	Pull-up Current	Vout = 1.5V	-67	-107	-184	mA
IOL <sub>1</sub>	Pull-down Current	Vout = 0.4V	23	34	53	mA
IOL <sub>2</sub>	Pull-down Current	Vout = 1.5V	64	98	159	mA
Z0	Output Impedance		10		24	Ω

**Test Measurement Condition**

**Figure 8.**
**Table 12. Suggested Oscillator Crystal Parameters**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F <sub>o</sub>	Frequency		14.17	14.31818	14.46	MHz
T <sub>C</sub>	Tolerance	Note 35			±100	PPM
T <sub>S</sub>	Frequency Stability	Stability (T <sub>A</sub> – 10 to +60C) <sup>[35]</sup>			±100	PPM
	Operating Mode	Parallel Resonant <sup>[35]</sup>				
C <sub>XTAL</sub>	Load Capacitance	The crystal's rated load <sup>[35]</sup>		20		pF
R <sub>ESR</sub>	Effective Series Resistance (ESR)	Note 36		40		Ohms

To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C<sub>XTAL</sub>. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C<sub>FTG</sub>), any circuit trace capacitance (C<sub>PCB</sub>) and any onboard discrete load capacitance (C<sub>DISC</sub>).

The following formula and schematic illustrates the application of the loading specification of a crystal (C<sub>XTAL</sub>) for a design.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{C_{XTAL}}$$

As an example and using a formula for this datasheet's device, a design that has no discrete loading capacitors (C<sub>DISC</sub>) and each of the crystal to device PCB traces has a capacitance (C<sub>PCB</sub>) to ground of 4pF (typical value) would calculate as:

**Notes:**

35. For best performance and accurate frequencies from this device, it is recommended but not mandatory that the chosen crystal meets or exceeds these specifications.
36. Larger values may cause this device to exhibit oscillator startup problems.

Where:

C<sub>XTAL</sub> = the load rating of the crystal.

C<sub>XOUTFTG</sub> ... = the clock generators XIN pin effective device internal capacitance to ground.

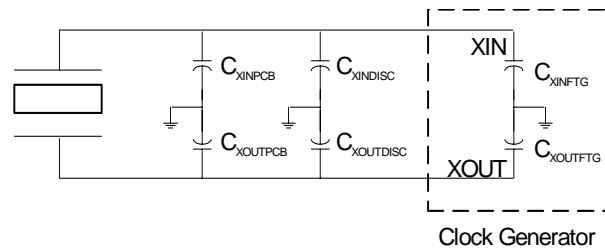
C<sub>XOUTFTG</sub> = the clock generators XOUT pin effective device internal capacitance to ground.

C<sub>XINPCB</sub> = the effective capacitance to ground of the crystal to device PCB trace.

C<sub>XOUTPCB</sub> = the effective capacitance to ground of the crystal to device PCB trace.

C<sub>XINDISC</sub> = any discrete capacitance that is placed between the X<sub>IN</sub> pin and ground.

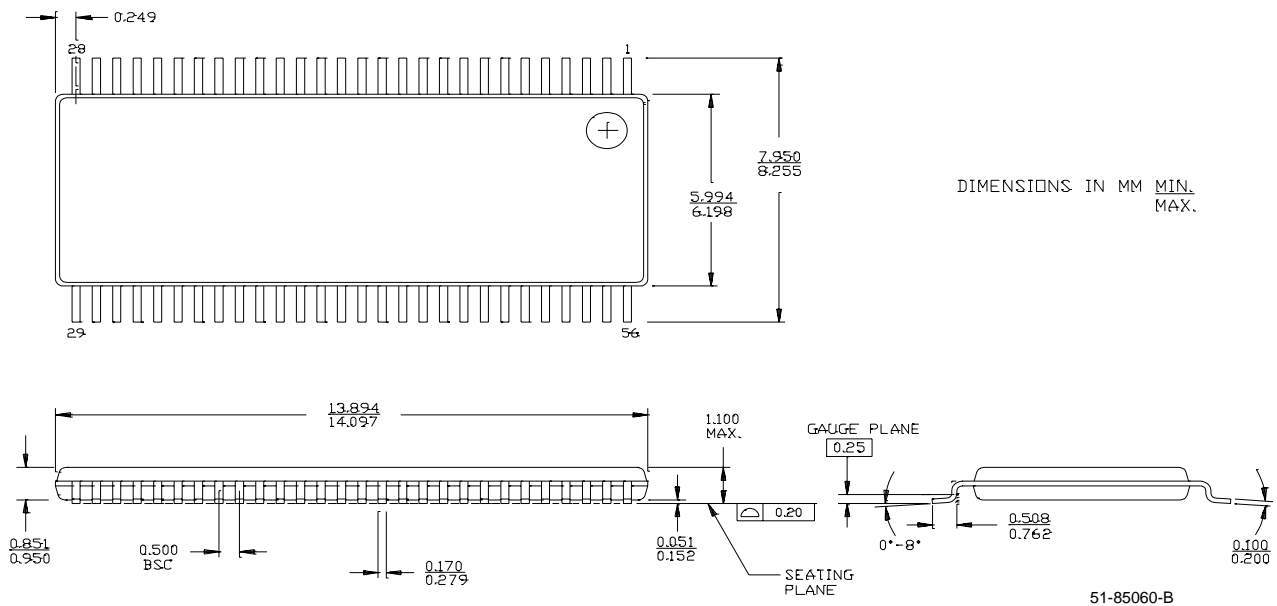
C<sub>XOUTDISC</sub> = any discrete capacitance that is placed between the X<sub>OUT</sub> pin and ground.


**Figure 9.**

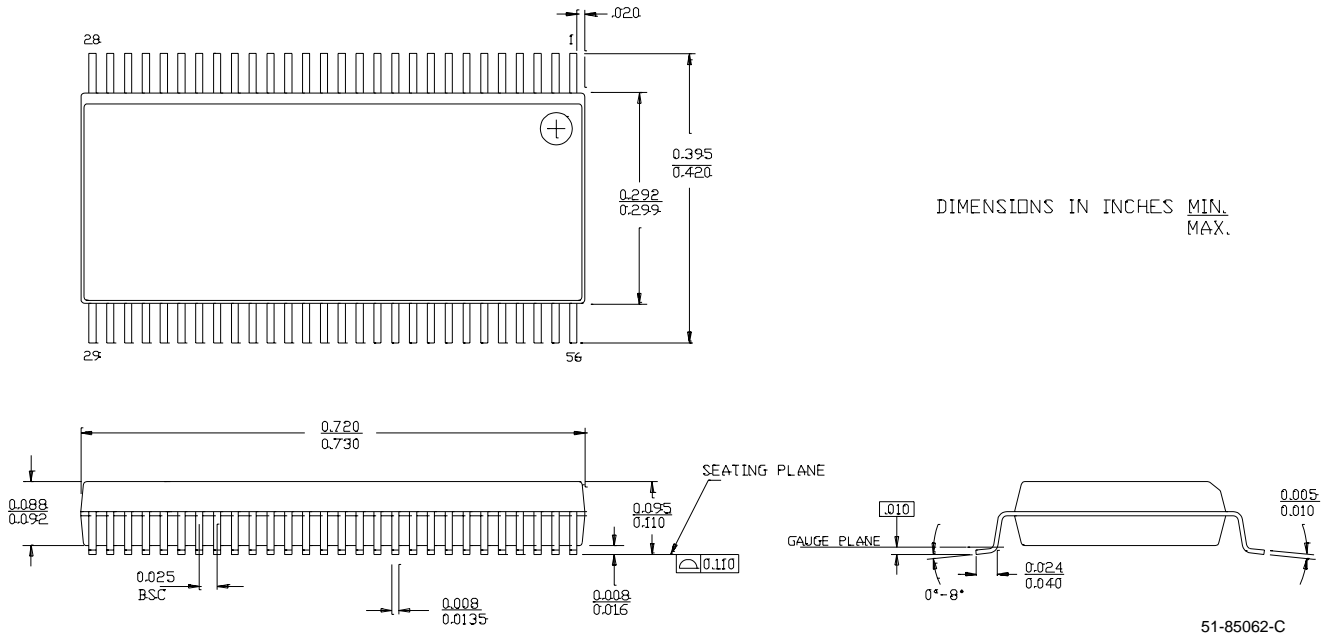
Therefore, to obtain output frequencies that are as close to this datasheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF.

**Ordering Information**

Part Number	Package Type	Product Flow
IMIC9835CY	56-pin Shrunken Small Outlie package (SSOP)	Commercial, 0° to 70°C
IMIC9835CYT	56-pin Shrunken Small Outlie package (SSOP)–Tape and Reel	Commercial, 0° to 70°C
IMIC9835CT	56-pin Thin Shrunken Small Outlie package (TSSOP)	Commercial, 0° to 70°C
IMIC9835CTT	56-pin Thin Shrunken Small Outlie package (TSSOP)–Tape and Reel	Commercial, 0° to 70°C

**Package Diagrams**
**56-lead Thin Shrunken Small Outline Package, Type II (6 mm x 12 mm) Z56**




**Package Diagrams (continued)**
**56-lead Shrunken Small Outline Package O56**


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**	113556	05/28/02	DMG	New Data Sheet (converted from IMI format)