



BUK7880-55A

N-channel TrenchMOS standard level FET

Rev. 01 — 1 November 2007

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP General Purpose Automotive (GPA) TrenchMOS technology.

1.2 Features

- Very low on-state resistance
- 150 °C rated
- Q101 compliant
- Standard level compatible

1.3 Applications

- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V and 24 V loads

1.4 Quick reference data

- $E_{DS(AL)S} \leq 53$ mJ
- $I_D \leq 7$ A
- $R_{DSon} = 68$ m Ω (typ)
- $P_{tot} \leq 8$ W

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	<p style="text-align: center;"><i>sol223_so</i></p> <p style="text-align: center;">SOT223 (SC-73)</p>	<p style="text-align: center;"><i>mbb076</i></p>
2	drain (D)		
3	source (S)		
4	solder point; connected to drain (D)		

3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
BUK7880-55A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

4. Limiting values

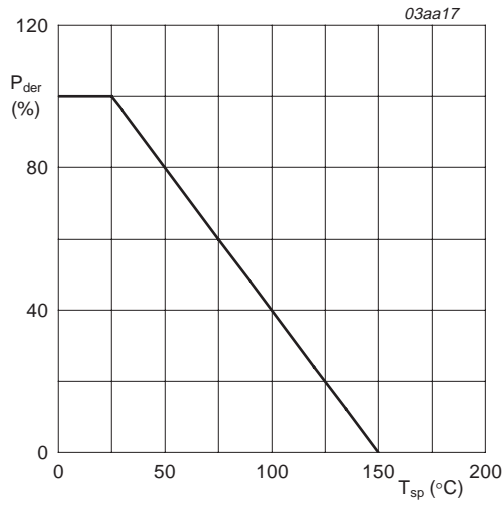
Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; see Figure 2 and 3	-	7	A
		$T_{sp} = 100 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; see Figure 2	-	5	A
I_{DM}	peak drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$; see Figure 3	-	30	A
P_{tot}	total power dissipation	$T_{sp} = 25 \text{ }^\circ\text{C}$; see Figure 1	-	8	W
T_{stg}	storage temperature		-55	+150	$^\circ\text{C}$
T_j	junction temperature		-55	+150	$^\circ\text{C}$
Source-drain diode					
I_{DR}	reverse drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$	-	7	A
I_{DRM}	peak reverse drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$	-	30	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 7 \text{ A}$; $V_{DS} \leq 55 \text{ V}$; $R_{GS} = 50 \text{ }\Omega$; $V_{GS} = 10 \text{ V}$; starting at $T_j = 25 \text{ }^\circ\text{C}$	-	53	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[1]	-	J

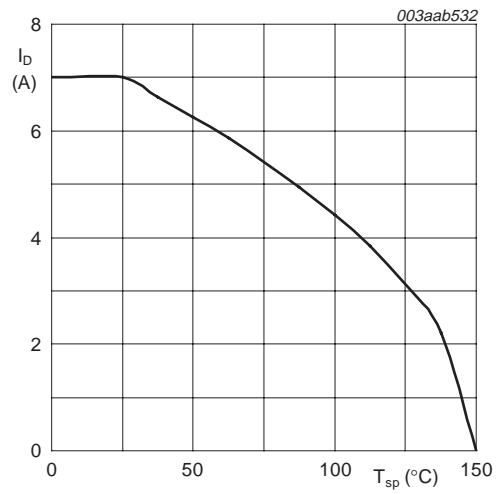
[1] Conditions:

- Maximum value not quoted. Repetitive rating defined in [Figure 16](#).
- Single-pulse avalanche rating limited by $T_{j(max)}$ of $150 \text{ }^\circ\text{C}$.
- Repetitive avalanche rating limited by an average junction temperature of $150 \text{ }^\circ\text{C}$.
- Refer to application note *AN10273* for further information.



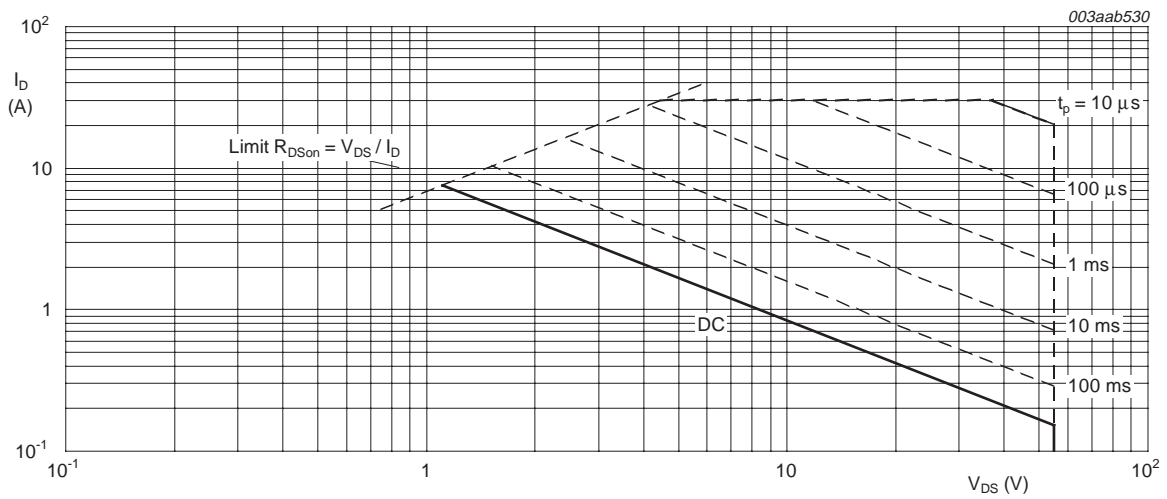
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$V_{GS} \geq 10\text{ V}$

Fig 2. Continuous drain current as a function of solder point temperature



$T_{sp} = 25^{\circ}C$; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	70	-	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	15	K/W

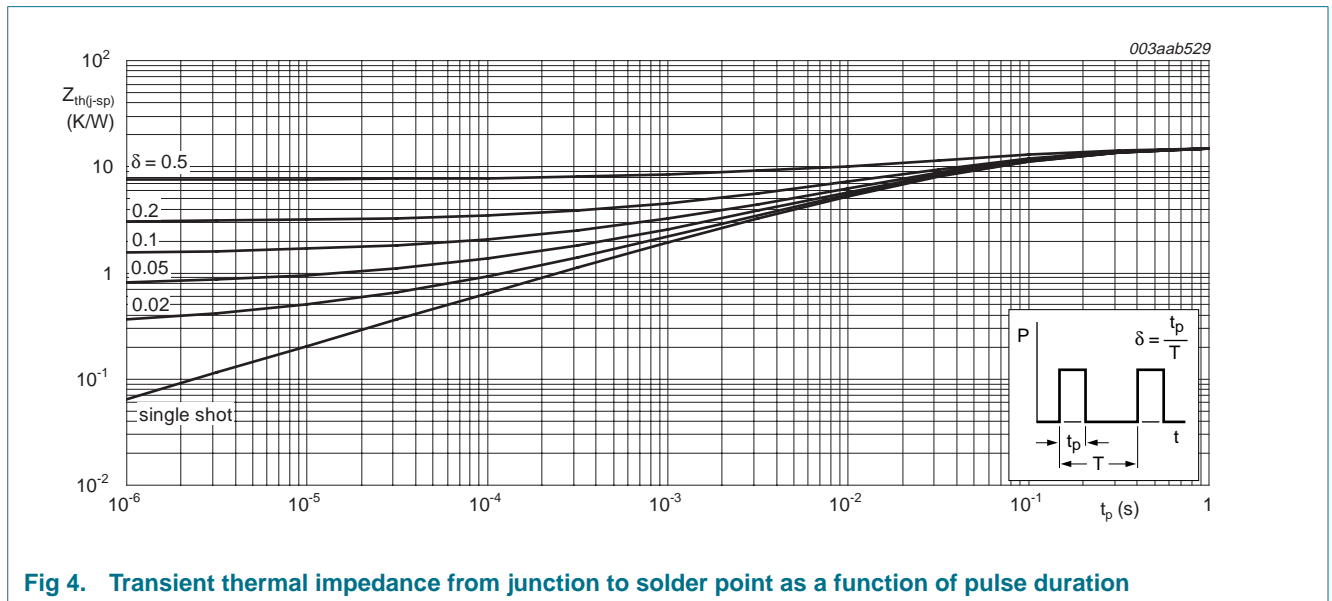


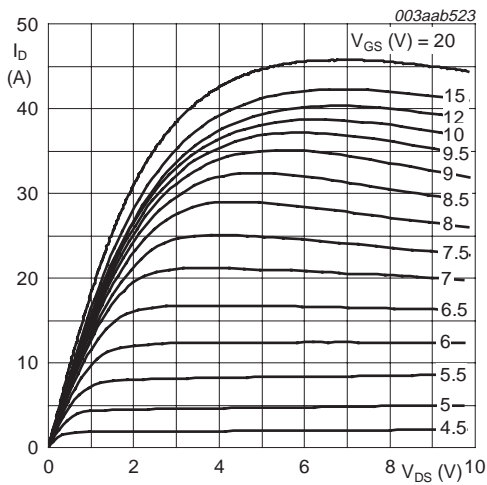
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5. Characteristics

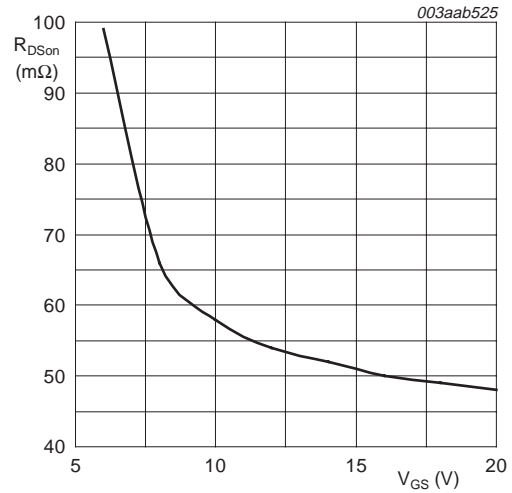
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	55	-	-	V
		$T_j = -55\text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$; see Figure 9				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 150\text{ °C}$	1.2	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
I_{DSS}	drain leakage current	$V_{DS} = 55\ \text{V}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	0.05	10	μA
		$T_j = 150\text{ °C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}; I_D = 10\ \text{A}$; see Figure 6 and 8				
		$T_j = 25\text{ °C}$	-	68	80	m Ω
		$T_j = 150\text{ °C}$	-	-	148	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10\ \text{A}; V_{DD} = 44\ \text{V}; V_{GS} = 10\ \text{V}$; see Figure 14	-	12	-	nC
Q_{GS}	gate-source charge		-	2.5	-	nC
Q_{GD}	gate-drain charge		-	5	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 25\ \text{V}; f = 1\ \text{MHz}$; see Figure 12	-	374	500	pF
C_{oss}	output capacitance		-	92	110	pF
C_{rss}	reverse transfer capacitance		-	62	85	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\ \text{V}; R_L = 1.2\ \Omega$;	-	8	-	ns
t_r	rise time	$V_{GS} = 10\ \text{V}; R_G = 10\ \Omega$	-	52	-	ns
$t_{d(off)}$	turn-off delay time		-	17	-	ns
t_f	fall time		-	9	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15\ \text{A}; V_{GS} = 0\ \text{V}$; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\ \text{A}; di_S/dt = -100\ \text{A}/\mu\text{s}$;	-	33	-	ns
Q_r	recovered charge	$V_{GS} = -10\ \text{V}; V_R = 30\ \text{V}$	-	31	-	nC



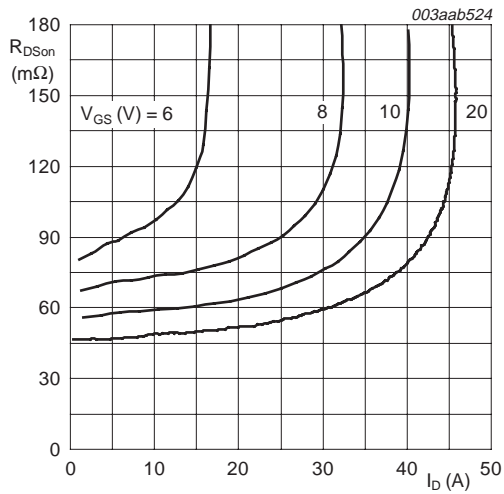
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



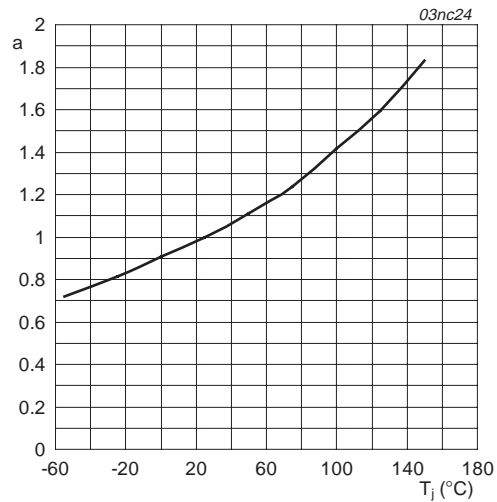
$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



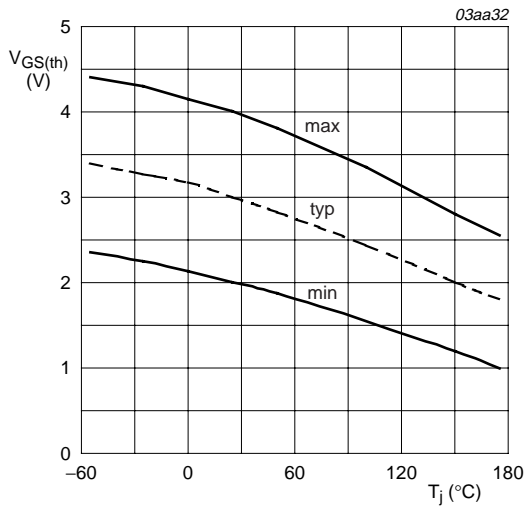
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



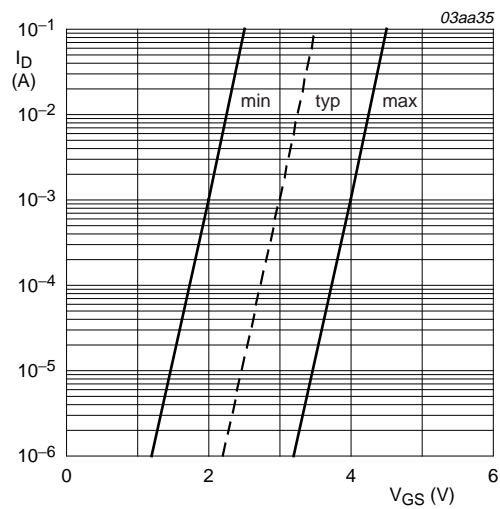
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



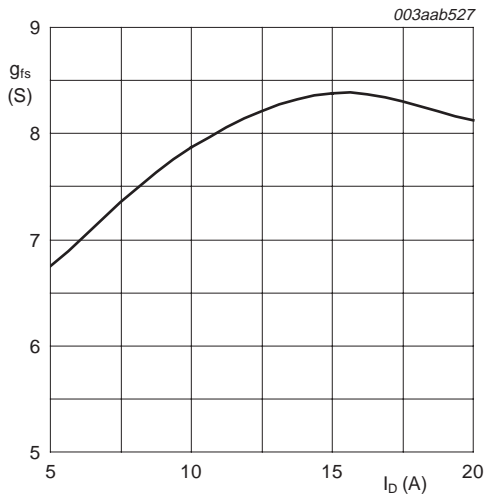
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



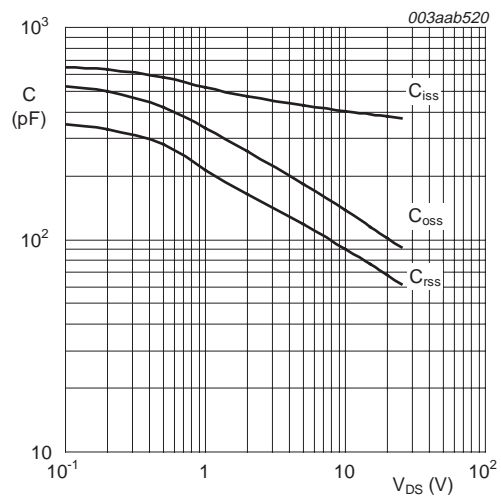
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



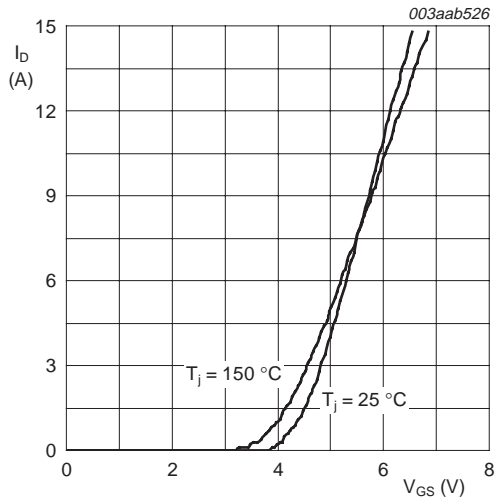
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 15 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values



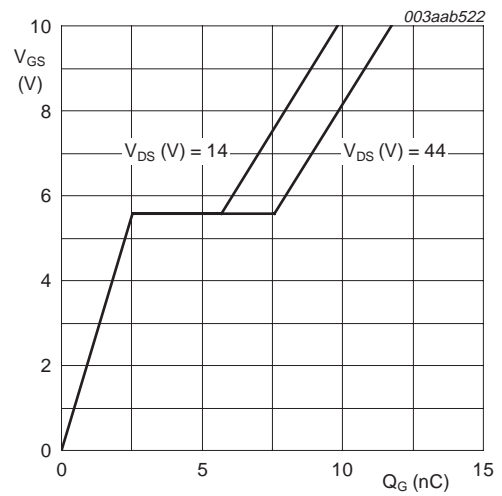
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



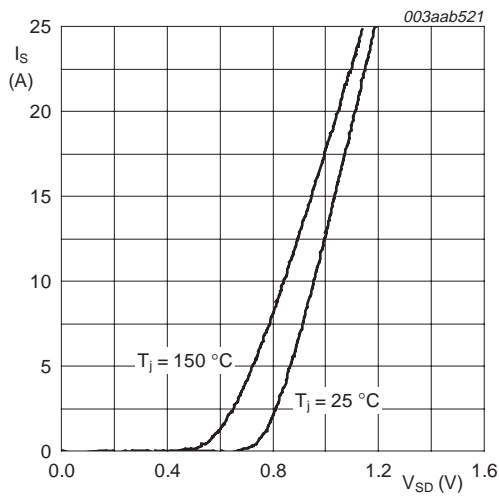
$V_{DS} = 15 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



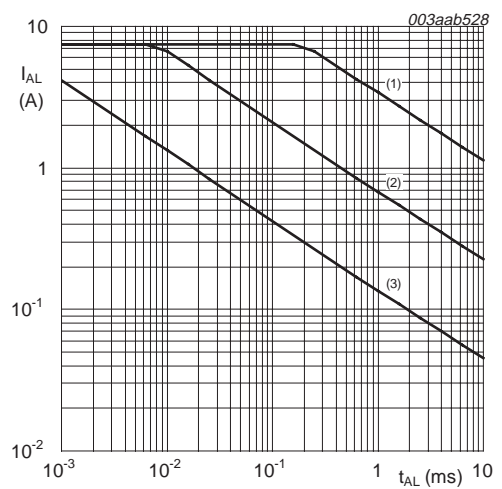
$T_j = 25 \text{ °C}; I_D = 10 \text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 \text{ V}$

Fig 15. Source current as a function of source-drain voltage; typical values



See [Table note 1](#) of [Table 3](#) Limiting values.

- (1) Single-pulse; $T_j = 25 \text{ °C}$.
- (2) Single-pulse; $T_j = 150 \text{ °C}$.
- (3) Repetitive.

Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

7. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

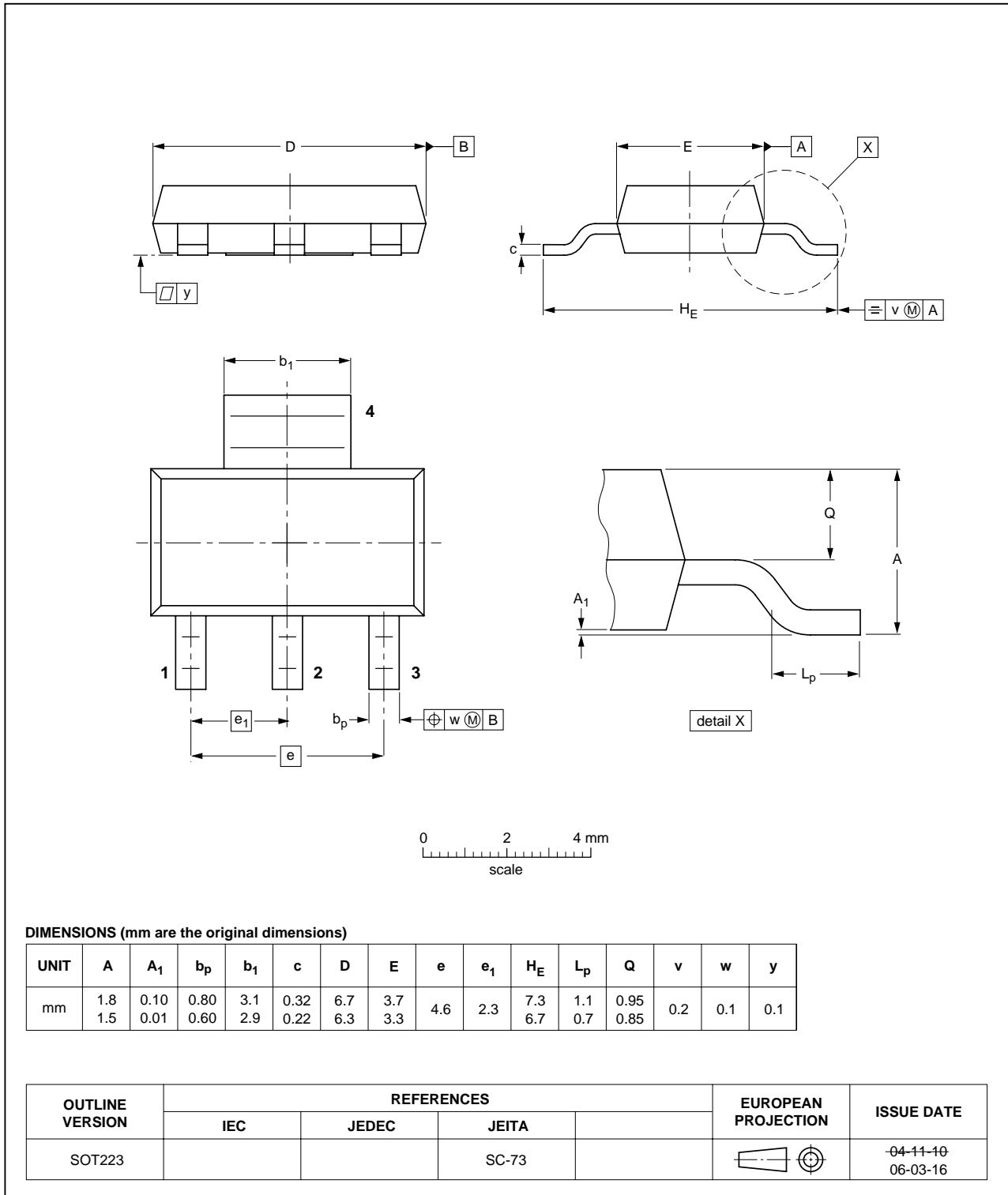


Fig 17. Package outline SOT223 (SC-73)

8. Soldering

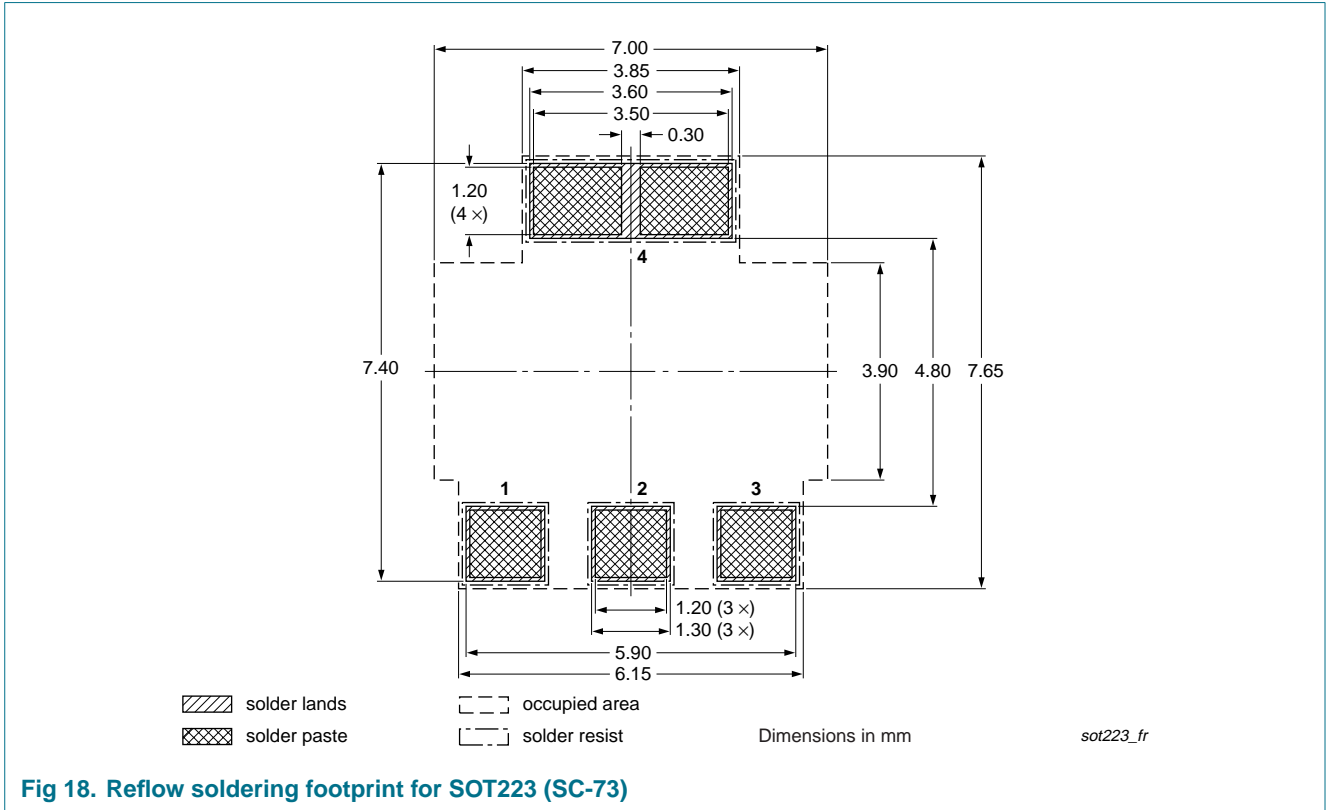


Fig 18. Reflow soldering footprint for SOT223 (SC-73)

9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7880-55A_1	20071101	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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