

PCM codec IC for digital cellular telephones

BU8733KV

The BU8733KV is a PCM codec IC developed for use with digital cellular telephones. The BU8733KV contains analog input / output features such as a 14-bit linear precision, μ / A-LAW codec, mic and speaker amplifiers, and a switching transistor for the ringer drive. Also, there is a built-in DSP interface circuit for support of multiple DSP formats making this IC perfect for use with PDC cellular telephones.

●Applications

Digital cellular telephones

●Features

- 1) +3V single power supply ($V_{DD} = 2.7V$ to $3.3V$).
- 2) Built-in 14-bit precision linear, μ / A-LAW codec.
- 3) Transmission filter for the codec unit conforms to ITU-T recommendations.
- 4) Built-in PLL circuit for system clock generation.
- 5) Tone signal generator contains DTMF signal, scale tone, and variable tone functions.
- 6) Analog input / output functions:
 - Built-in mic amplifier.
 - Built-in receiver speaker amplifier (32Ω BTL type).
- Built-in attenuator for wide gain adjustment range.
- Data signal I / O circuit allows for connection to external devices.
- For the external output and receiver output, soft-mute function reduces pop noise when the power is turned on and off.
- 7) Internal switching transistor for ringer drive.
- 8) Internal DSP interface circuit supports multiple DSP formats.

●Absolute maximum ratings ($T_a = 25^\circ C$)

| Parameter | Symbol | Limits | Unit |
|------------------------------|------------|--------------------------------------|------------|
| Digital power supply voltage | DV_{DD} | $-0.3 \sim +4.5$ | V |
| Analog power supply voltage | RXV_{DD} | $-0.3 \sim +4.5$ | V |
| | TXV_{DD} | $-0.3 \sim +4.5$ | V |
| Digital input voltage | V_{DIN} | $DV_{SS} - 0.3 \sim DV_{DD} + 0.3$ | V |
| Analog input voltage | V_{AIN} | $RXV_{SS} - 0.3 \sim RXV_{DD} + 0.3$ | V |
| | | $TXV_{SS} - 0.3 \sim TXV_{DD} + 0.3$ | V |
| Input current | I_{IN} | $-10 \sim +10$ | mA |
| Power dissipation | P_d | 400^{*1} | mW |
| Operating temperature | T_{stg} | $-50 \sim +125$ | $^\circ C$ |
| Storage temperature | T_{opr} | $-30 \sim +85$ | $^\circ C$ |

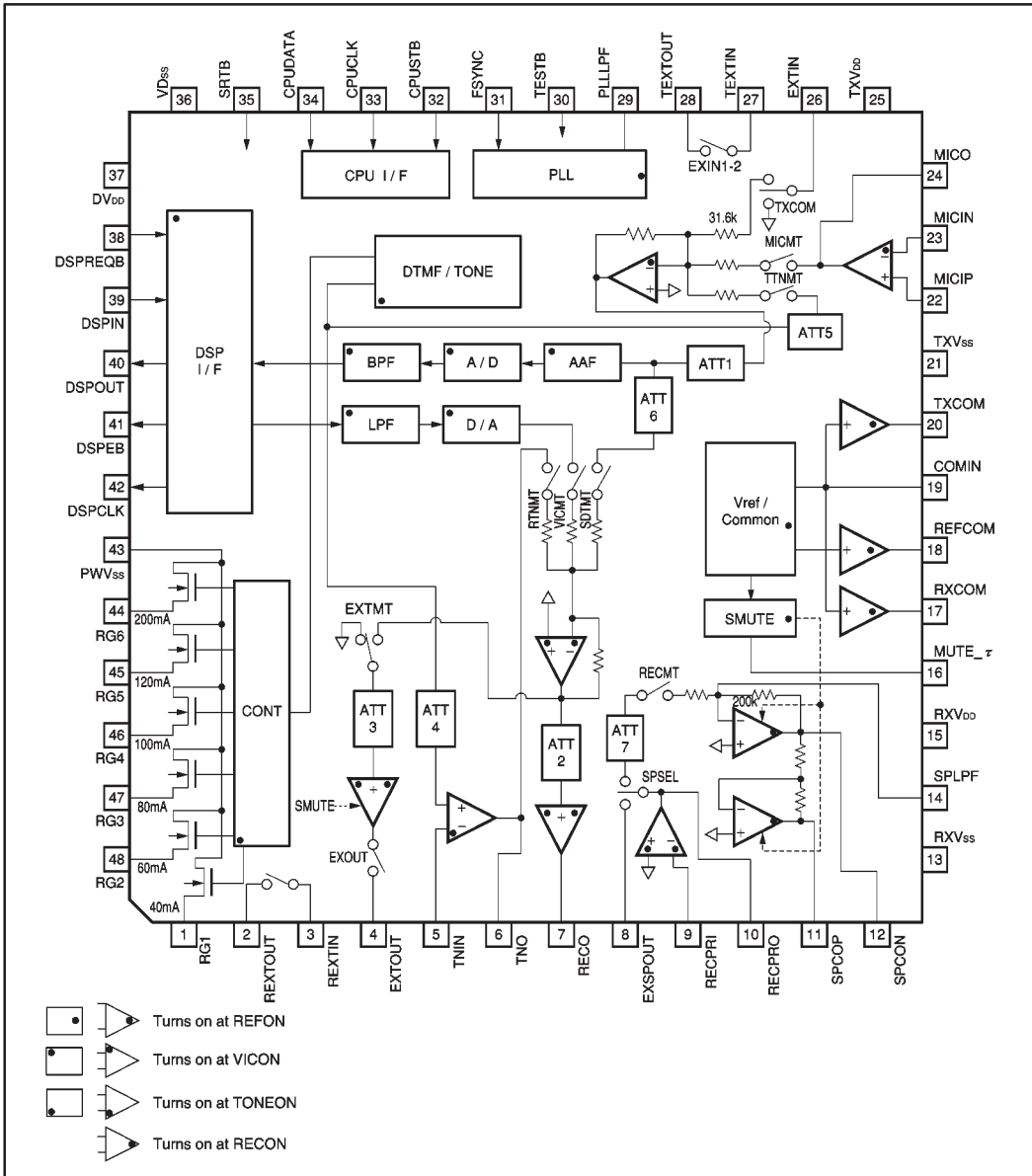
*1 Reduced by 4.0 mW for each increase in T_a of $1^\circ C$ over $25^\circ C$.

● Recommended operating conditions (Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|------------------------------|-------------------|------|------|------|------|
| Digital power supply voltage | DV _{DD} | 2.7 | — | 3.3 | V |
| Analog power supply voltage | RXV _{DD} | 2.7 | — | 3.3 | V |
| | TXV _{DD} | 2.7 | — | 3.3 | V |
| PLL sync signal frequency | FSY | — | 8 | — | kHz |

© Not designed for radiation resistance.

● Block diagram



● Pin descriptions

| Pin No. | I/O | Pin name | Function | Minimum load resistance (Ω) | Maximum load capacitance (F) |
|---------|-----|-------------------|--|--------------------------------------|------------------------------|
| 1 | O | RG1 | Ringer 40mA output | 75 | — |
| 2 | O | REXTOUT | Reception data output | — | — |
| 3 | I | REXTIN | Reception data input | — | — |
| 4 | O | EXTOUT | Reception external output | 50k | 20p |
| 5 | I | TNIN | TONE output gain control amplifier inverse input | — | — |
| 6 | O | TNO | TONE output gain control amplifier output | 50k | 20p |
| 7 | O | RECO | Reception signal output | 50k | 20p |
| 8 | O | EXSPOUT | Output for external receiver | 50k | 20p |
| 9 | I | RECPRI | Receiver gain control amplifier inverse input | — | — |
| 10 | O | RECPRO | Receiver gain control amplifier output | 50k | 20p |
| 11 | O | SPCOP | Receiver amplifier inverse output | 32 (BTL) | — |
| 12 | O | SPCON | Receiver amplifier non-inverse output | 32 (BTL) | — |
| 13 | — | RXV _{ss} | Analog ground for reception | — | — |
| 14 | I | SPLPF | Receiver amplifier filter input | — | — |
| 15 | — | RXV _{DD} | Analog power supply for reception | — | — |
| 16 | O | MUTE_ τ | For connecting capacitor for soft mute | — | — |
| 17 | O | RXCOM | Analog reference voltage output for reception | — | — |
| 18 | O | REFCOM | Reference voltage output for internal reference | — | — |
| 19 | I | COMIN | Analog reference voltage input | — | — |
| 20 | O | TXCOM | Analog reference voltage output for transmission | — | — |
| 21 | — | TXV _{ss} | Analog ground for transmission | — | — |
| 22 | I | MICIP | Mic amplifier non-inverse input | — | — |
| 23 | I | MICIN | Mic amplifier inverse input | — | — |
| 24 | O | MICO | Mic amplifier output | 50k | 20p |
| 25 | — | TXV _{DD} | Analog power supply for transmission | — | — |
| 26 | I | EXTIN | Transmission external input | — | — |
| 27 | I | TEXTIN | Transmission data input | — | — |
| 28 | O | TEXTOUT | Transmission data output | — | — |
| 29 | O | PLLLPF | Filter output for PLL | — | — |
| 30 | I | TESTB | Test input (\rightarrow DV _{DD}) | — | — |
| 31 | I | FSYNC | PLL reference 8kHz clock input | — | — |
| 32 | I | CPUSTB | CPU I/F strobe input | — | — |
| 33 | I | CPUCLK | CPU I/F shift clock input | — | — |
| 34 | I | CPUDATA | CPU I/F address data input | — | — |
| 35 | I | RSTB | System reset input (L: reset) | — | — |
| 36 | — | DV _{ss} | Digital ground | — | — |
| 37 | — | DV _{DD} | Digital power supply | — | — |
| 38 | I | SDPREQB | DSP serial data request input | — | — |
| 39 | I | DSPIN | DSP serial data input (50k Ω pull-down) | — | — |

| Pin No. | I / O | Pin name | Function | Minimum load resistance (Ω) | Maximum load capacitance (F) |
|---------|-------|----------|-------------------------------|--------------------------------------|------------------------------|
| 40 | O | DSPOUT | DSP serial data output | — | — |
| 41 | O | DSPEB | DSP serial data enable output | — | — |
| 42 | O | DSPCLK | DSP serial data clock output | — | — |
| 43 | — | PWVss | Ringer ground | — | — |
| 44 | O | RG6 | Ringer 200mA output | 15 | — |
| 45 | O | RG5 | Ringer 120mA output | 25 | — |
| 46 | O | RG4 | Ringer 100mA output | 30 | — |
| 47 | O | RG3 | Ringer 80mA output | 38 | — |
| 48 | O | RG2 | Ringer 60mA output | 50 | — |

- Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $DV_{DD} = RXV_{DD} = TXV_{DD} = 3.0\text{V}$, $FSYNC = 8\text{kHz}$, gain of each attenuator = 0dB)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions | |
|------------------------------------|-----------|-------------------|------|------------------|---------------|-----------------------------------|------------------------|
| 〈DC characteristics〉 | | | | | | | |
| Current consumption*1 | I_{DD0} | — | — | 20 | μA | Complete power down | $FSYNC = \text{fixed}$ |
| | I_{DD1} | — | 2.7 | 3.9 | mA | Only reference on | $FSYNC = 8\text{kHz}$ |
| | I_{DD2} | — | 3.2 | 4.5 | mA | Reference and tone on | $FSYNC = 8\text{kHz}$ |
| | I_{DD3} | — | 4.1 | 5.8 | mA | Reference and audio on | $FSYNC = 8\text{kHz}$ |
| | I_{DD4} | — | 4.4 | 6.2 | mA | Reference, tone, and audio on | $FSYNC = 8\text{kHz}$ |
| | I_{DD5} | — | 5.4 | 7.6 | mA | All power on | $FSYNC = 8\text{kHz}$ |
| Digital input high level voltage | V_{IH} | 0.8 DV_{DD} | — | — | V | — | — |
| Digital input low level voltage | V_{IL} | — | — | 0.2 DV_{DD} | V | — | — |
| Digital input high level current 1 | I_{IH1} | — | — | 10 | μA | $V_{IH} = DV_{DD}$ | *2 |
| Digital input high level current 2 | I_{IH2} | 30 | 60 | 120 | μA | $V_{IH} = DV_{DD}$ | DSPIN pin |
| Digital input low level current | I_{IL} | -10 | — | — | μA | $V_{IL} = 0\text{V}$ | — |
| Digital output high level voltage | V_{OH} | DV_{DD} -0.5 | — | — | V | $I_{OH} = -1\text{mA}$ | — |
| Digital output low level voltage | V_{OL} | — | — | 0.5 | V | $I_{OL} = 1\text{mA}$ | — |
| 〈Ringer drive〉 | | | | | | | |
| Level output voltage 1 | V_{OL1} | — | — | 0.5 | V | $I_o = 40\text{mA}$, RG1 | |
| Level output voltage 2 | V_{OL2} | — | — | 0.5 | V | $I_o = 60\text{mA}$, RG2 | |
| Level output voltage 3 | V_{OL3} | — | — | 0.5 | V | $I_o = 80\text{mA}$, RG3 | |
| Level output voltage 4 | V_{OL4} | — | — | 0.6 | V | $I_o = 100\text{mA}$, RG4 | |
| Level output voltage 5 | V_{OL5} | — | — | 0.6 | V | $I_o = 120\text{mA}$, RG5 | |
| Level output voltage 6 | V_{OL6} | — | — | 0.8 | V | $I_o = 200\text{mA}$, RG6 | |
| OFF leak current | I_{OH} | — | — | 3 | μA | $V_o = DV_{DD}$, RG1 ~ RG6 = OFF | |

*1 The power supply voltage (DV_{DD} , RXV_{DD} , and TXV_{DD}) is 3V. There is no load on the digital and analog output pins. Digital input pins other than the FSYNC pin are connected to DV_{DD} or DV_{SS} .

Analog input pins are connected to TXCOM or RXCOM with the proper resistance.

*2 Digital input pins other than DSPIN.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions | | |
|---|------------------|------|-------|------|------------------|-------------------------------------|--------------------------|--------------------------------------|
| 〈Transmission characteristics〉 | | | | | | | | |
| Signal to total power distortion ratio (A→D) EXTIN→DSPOUT | S _{DT} | 24 | — | — | dB | 1020Hz reference | —45dBm0 | C-Wgt |
| | | 29 | — | — | | | —40dBm0 | |
| | | 35 | — | — | | | 0, —30dBm0 | |
| Signal to total power distortion ratio (D→A) DSPIN→RECO | S _{DR} | 24 | — | — | dB | 1020Hz reference | —45dBm0 | C-Wgt |
| | | 29 | — | — | | | —40dBm0 | |
| | | 35 | — | — | | | 0, —30dBm0 | |
| Transmission level characteristics (A→D) EXTIN→DSPOUT | G _{TX} | —0.9 | — | 0.9 | dB | 1020Hz reference | —55dBm0 | Reference level =—10dBm0 C-Wgt |
| | | —0.6 | — | 0.6 | | | —50dBm0 | |
| | | —0.3 | — | 0.3 | | | 0, —40dBm0 | |
| Transmission level characteristics (D→A) DSPIN→RECO | G _{TR} | —0.9 | — | 0.9 | dB | 1020Hz reference | —55dBm0 | Reference level =—10dBm0 C-Wgt |
| | | —0.6 | — | 0.6 | | | —50dBm0 | |
| | | —0.3 | — | 0.3 | | | 0, —40dBm0 | |
| Transmission output level | V _{OTX} | — | 0.501 | — | V _{rms} | 1020Hz, 0dBm0 input reference | MICO→ DSPOUT | MICO level is set to 0dB |
| | | — | 0.158 | — | V _{rms} | | EXTIN →DSPOUT | — |
| Reception output level | V _{ORX} | — | 0.501 | — | V _{rms} | 1020Hz, 3dBm0 input reference | DSPIN→ EXTOUT | — |
| | | — | 0.501 | — | V _{rms} | | DSPIN →SPCOP SPCON | When RECO→ RECPRO—6dB |
| Transmission loss frequency characteristics (A→D) EXTIN→DSPOUT | G _{RX} | 24 | — | — | dB | 1020Hz, 0dBm0 input reference | 0.06kHz | — |
| | | 0 | — | 2.5 | | | 0.2kHz | |
| | | —0.3 | — | 0.3 | | | 0.3~3.0kHz | |
| | | —0.3 | — | 0.9 | | | 3.4kHz | |
| | | 0 | — | — | | | 3.6kHz | |
| | | 6.5 | — | — | | | 3.78kHz | |
| Transmission loss frequency characteristics (D→A) DSPIN→RECO | G _{RR} | —0.3 | — | 0.3 | dB | 1020Hz, 0dBm0 input reference | 0.0~3.0kHz | — |
| | | —0.3 | — | 0.9 | | | 3.4kHz | |
| | | 0 | — | — | | | 3.6kHz | |
| | | 6.5 | — | — | | | 3.78kHz | |

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions | | | | |
|-------------------|-----------|---------------|-------|-------|------------|-------------------|-------------|-------------------------|---|--|
| 〈Tone generator〉 | | | | | | | | | | |
| Tone output level | High | V_{TNH} | -11.1 | -9.6 | -8.1 | dBm | Set at 2kHz | →RECO | 30kHz LPF 0dBm=0.775V _{rms} | |
| | | | -11.1 | -9.6 | -8.1 | | | →DSPOUT | | |
| | Low | V_{TNL} | -13.3 | -11.8 | -10.3 | dBm | | →RECO | | |
| Tone distortion | S_{DTN} | — | — | -29 | dB | HTONE set at 2kHz | →RECO | 30kHz LPF | | |
| 〈Attenuator〉 | | | | | | | | | | |
| Gain error | ATT1 | $\Delta ATT1$ | -1 | — | +1 | dB | 1kHz input | →DSPOUT | -21~+10dB | |
| | ATT2 | $\Delta ATT2$ | -1 | — | +1 | dB | | →RECO | -31~0dB | |
| | ATT3 | $\Delta ATT3$ | -1 | — | +1 | dB | | →EXTOUT | -31~0dB | |
| | ATT4 | $\Delta ATT4$ | -1 | — | +1 | dB | Set at 2kHz | →RECO | -31~0dB | |
| | ATT5 | $\Delta ATT5$ | -1 | — | +1 | dB | | →DSPOUT | -31~0dB | |
| | ATT6 | $\Delta ATT6$ | -1 | — | +1 | dB | 1kHz input | →RECO | -41~-10dB | |
| | ATT7 | $\Delta ATT7$ | -1 | — | +1 | dB | | →SPCON | -5~+10dB | |
| 〈PLL block〉 | | | | | | | | | | |
| PLL lead-in time | T_{PL} | — | 5 | 100 | ms | — | — | Guaranteed design value | | |
| 〈Speaker〉 | | | | | | | | | | |
| Gain resistance | R_{SG} | 140 | 200 | 260 | k Ω | — | — | — | | |
| Output power | P_{SP} | 6.4 | 40 | — | mW | Load 32 Ω | — | — | | |

● Digital AC characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|------------|------|------|------|---------|
| 〈Serial data interface / timing〉 | | | | | |
| DSPCLK frequency | f_{sck} | — | 256 | — | kHz |
| DSPREQB input setup time | t_{sur} | 3.0 | — | — | μs |
| DSPREQB input hold time | t_{htr} | 3.0 | — | — | μs |
| DSPIN input setup time | t_{sus} | 100 | — | — | ns |
| DSPIN input hold time | t_{hns} | 100 | — | — | ns |
| DSPPEB low pulse width | t_{wen} | 5.0 | — | — | μs |
| DSPREQB scan internal clock frequency | f_{rex} | — | 8 | — | kHz |
| 〈Register write timing〉 | | | | | |
| CPUCLK frequency | f_{clk} | — | — | 3 | MHz |
| CPUDATA input setup time | t_{suda} | 100 | — | — | ns |
| CPUDATA input hold time | t_{hnda} | 100 | — | — | ns |
| Input setup time (CPUCLK high vs. CPUSTR high) | t_{sud} | 333 | — | — | ns |
| Input hold time (CPUCLK high vs. CPUSTR low) | t_{hnd} | 1000 | — | — | ns |
| CPUSTR strobe pulse width | f_{pwd} | 667 | — | — | ns |

● Measurement circuit

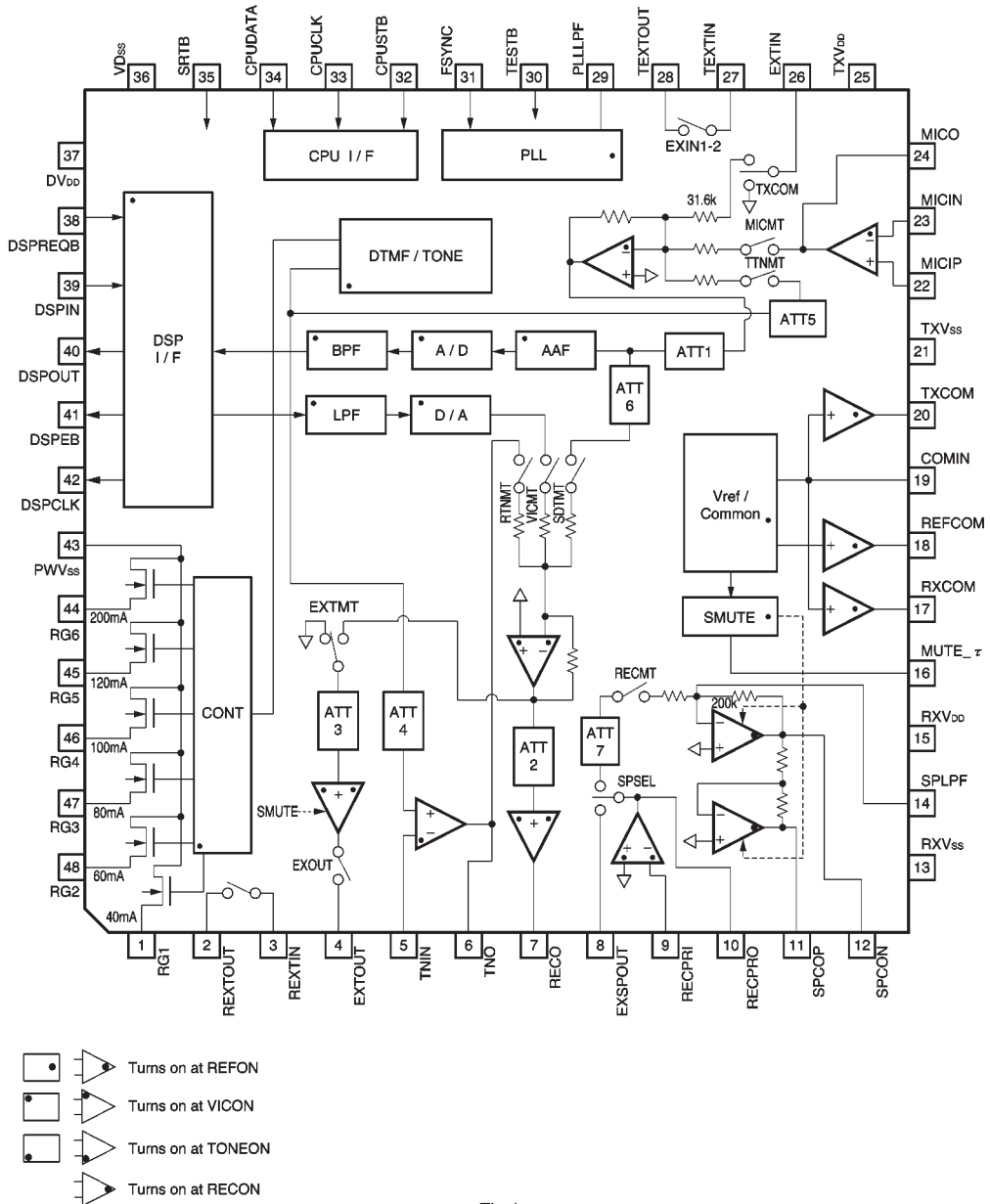


Fig.1

●Application example

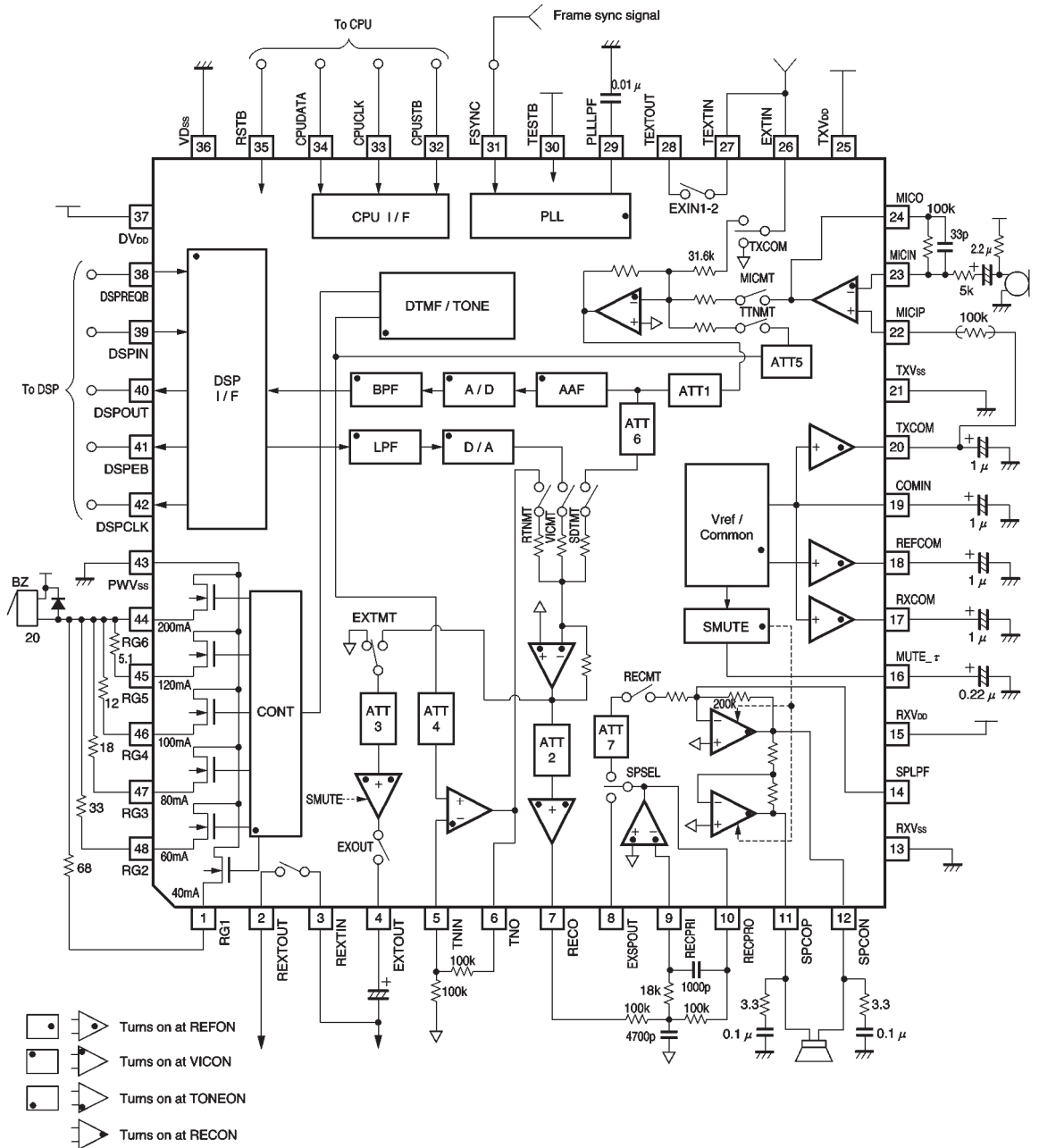


Fig.2

● External dimensions (Units: mm)

