DATA SHEET

BT132 series D
Triacs
logic level

Product specification

January 1998

Triacs logic level

BT132 series D

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

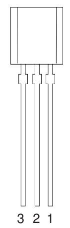
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT132-	500D	600D	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	1	1	A
I_{TSM}	Non-repetitive peak on-state current	16	16	A

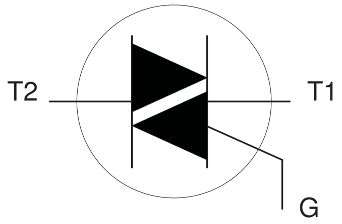
PINNING - TO92

PIN	DESCRIPTION
1	main terminal 2
2	gate
3	main terminal 1

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500	-600	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 51$ ˚C	-	1		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; T_j = 25 ˚C prior to surge				
		t = 20 ms	-	16		A
		t = 16.7 ms	-	17.6		A
I^2t	I^2t for fusing	t = 10 ms	-	1.28		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 1.5 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}lead}$	Thermal resistance junction to lead	full cycle	-	-	60	K/W
		half cycle	-	-	80	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted;lead length = 4mm	-	150	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.0	5	mA
		T2+ G-	-	2.5	5	mA
		T2- G-	-	2.5	5	mA
		T2- G+	-	5.0	10	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.6	10	mA
		T2+ G-	-	4.5	15	mA
		T2- G-	-	1.2	10	mA
		T2- G+	-	2.2	15	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.2	10	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	5	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	2	-	μs

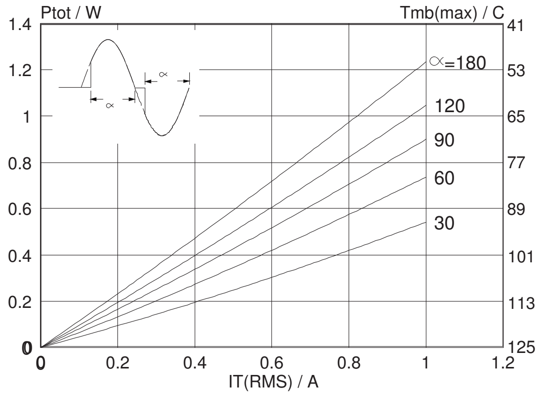


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

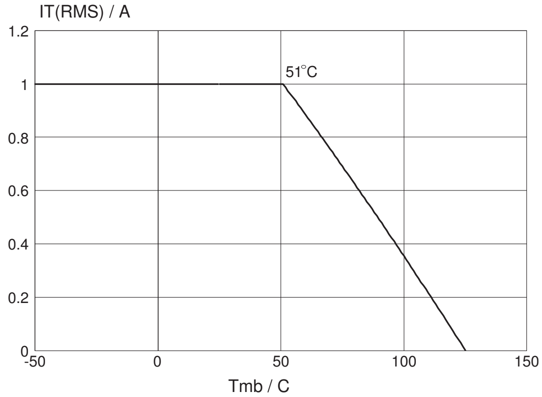


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature T_{lead}.

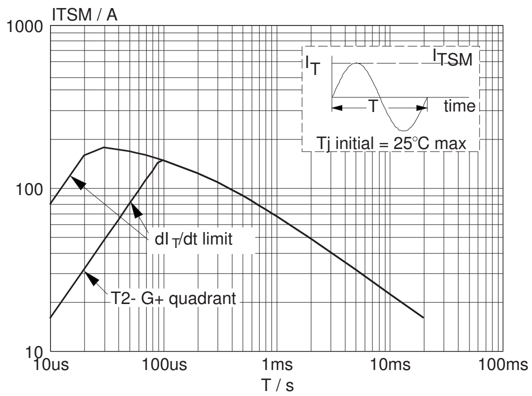


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

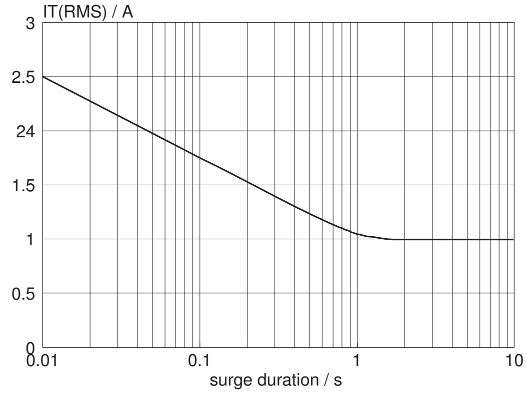


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 51˚C$.

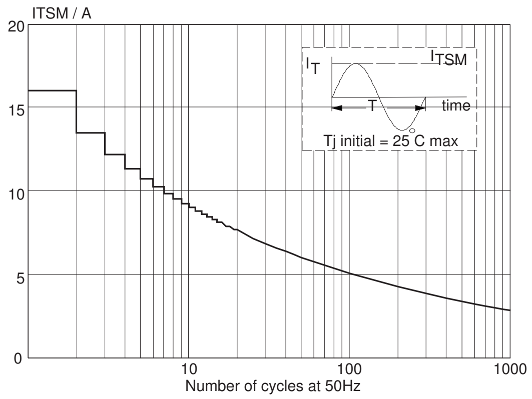


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

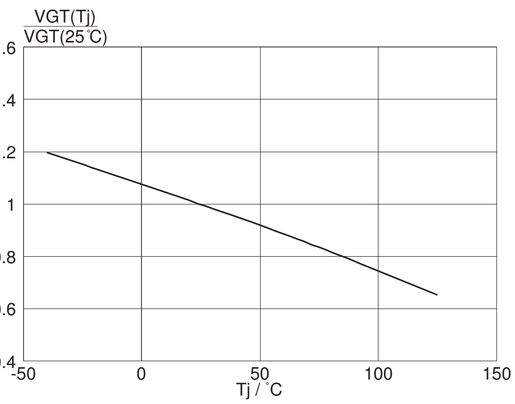


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ $V_{GT}(25˚C)$, versus junction temperature T_j.

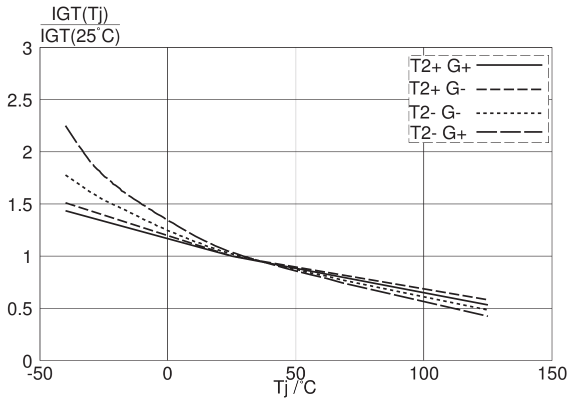


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

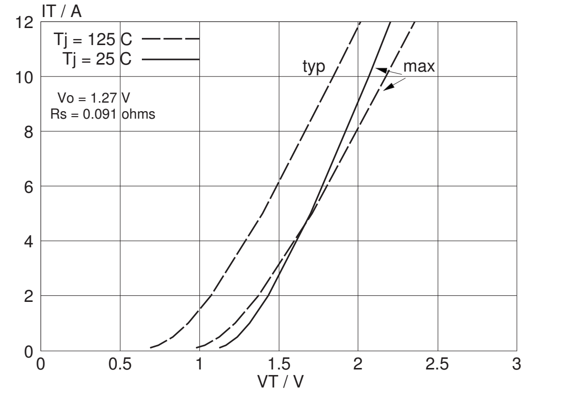


Fig.10. Typical and maximum on-state characteristic.

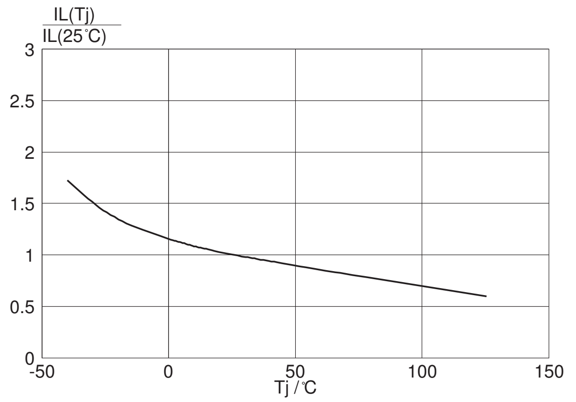


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

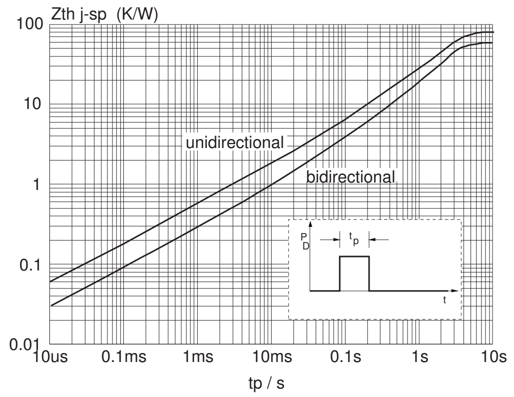


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width t_p.

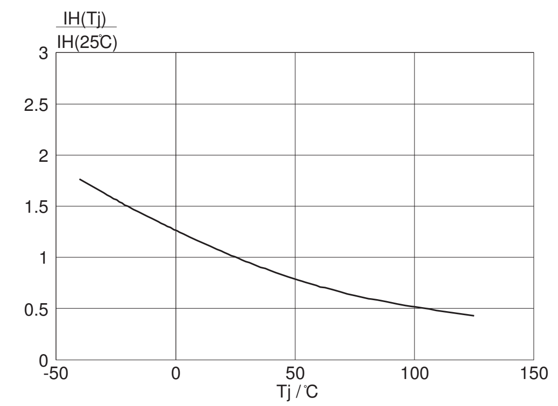


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

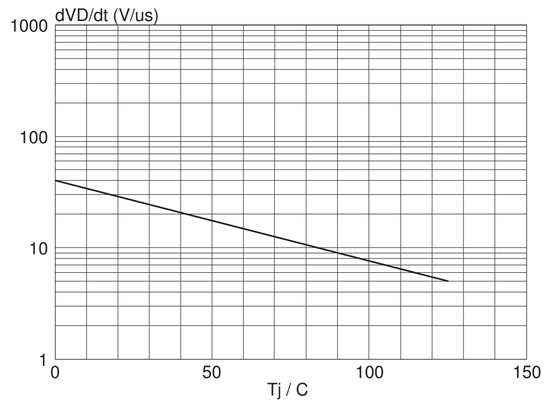


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MECHANICAL DATA

Dimensions in mm

Net Mass: 0.2 g

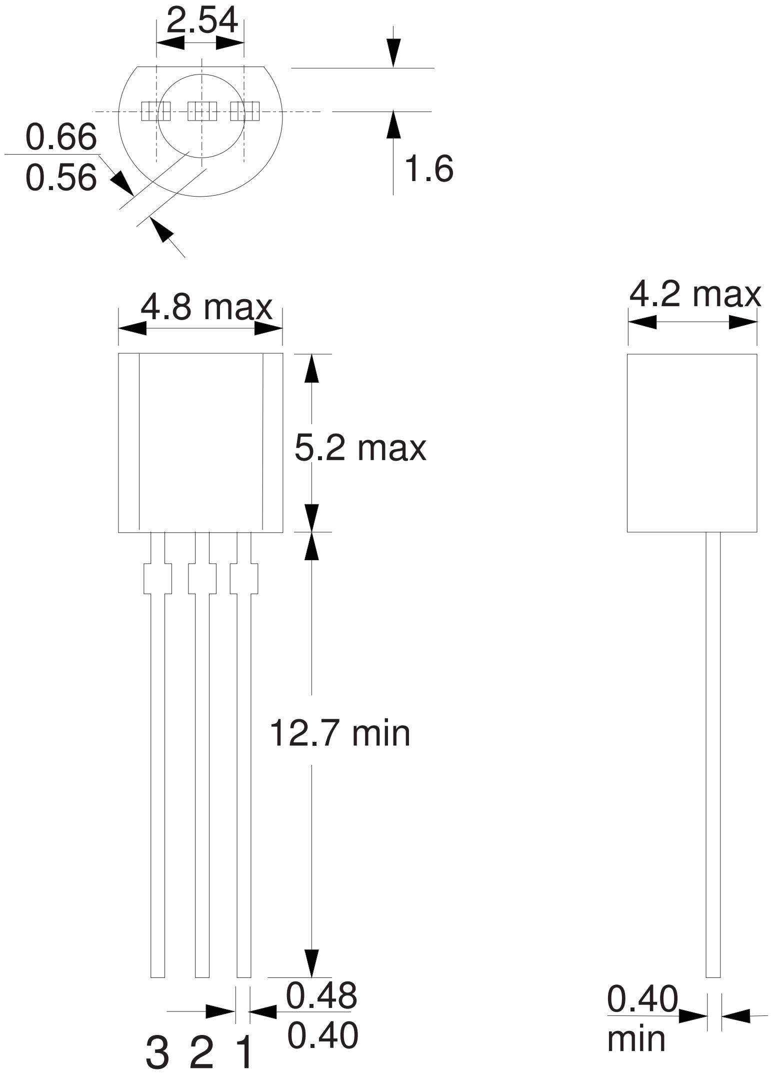


Fig.13. TO92 Variant; plastic envelope.

Notes

1. Epoxy meets UL94 V0 at 1/8".

Legal information

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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