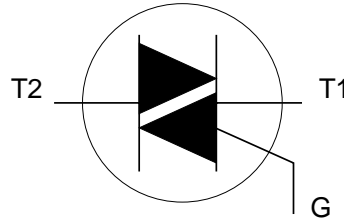


KERSEMI ELECTRONIC CO.,LTD.
GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

SYMBOL

SOT223

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
V_{DRM}	BT131W- Repetitive peak off-state voltages	500 500	600 600	V
$I_{T(RMS)}$	RMS on-state current	1	1	A
I_{TSM}	Non-repetitive peak on-state current	10	10	A

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500 500 ¹	-600 600 ¹	
V_{DRM}	Repetitive peak off-state voltages		-	-500 500 ¹	-600 600 ¹	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 108^\circ\text{C}$	-	1		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25^\circ\text{C}$ prior to surge $t = 20\text{ ms}$	-	10		A
		$t = 16.7\text{ ms}$	-	11		A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	0.5		A ² s
di_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 1.5\text{ A}; I_G = 0.2\text{ A};$ $di_G/dt = 0.2\text{ A}/\mu\text{s}$				
		T2+ G+	-	50		A/ μs
		T2+ G-	-	50		A/ μs
		T2- G-	-	50		A/ μs
		T2- G+	-	10		A/ μs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		$^\circ\text{C}$
T_j	Operating junction temperature		-	125		$^\circ\text{C}$

¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/ μs .

THERMAL RESISTANCES

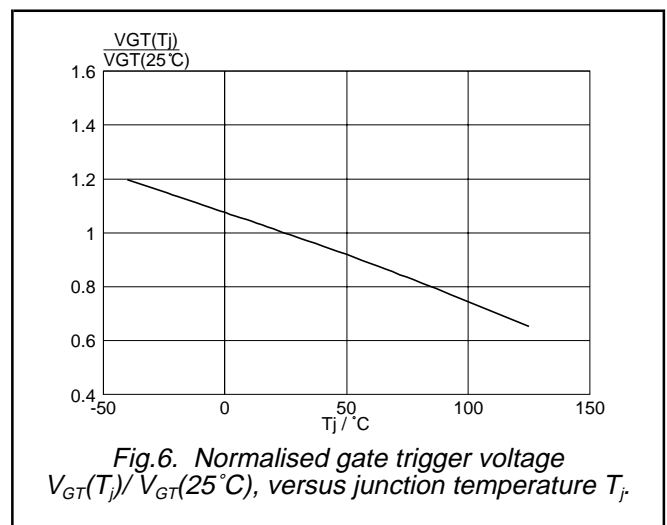
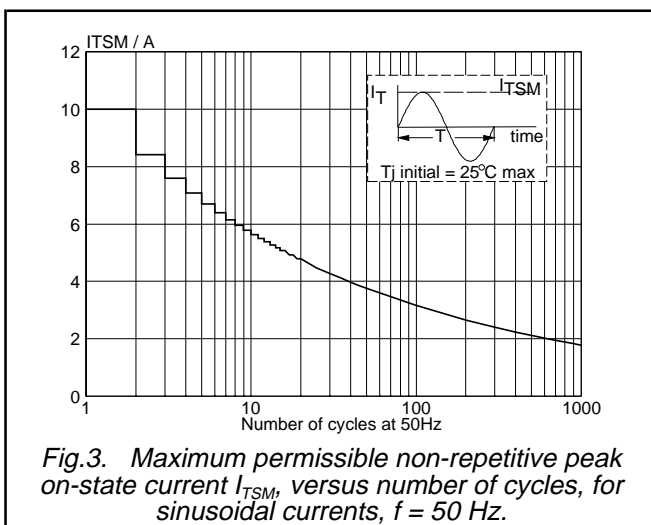
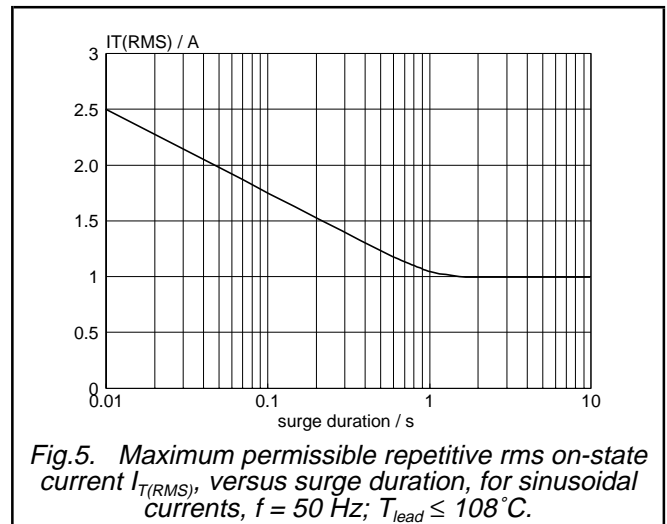
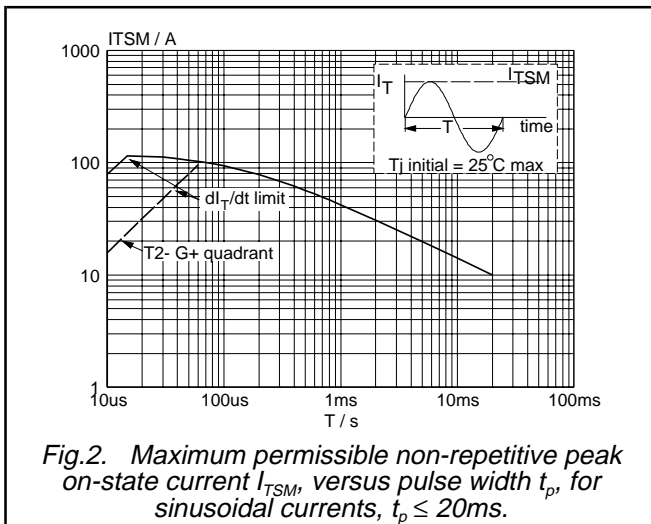
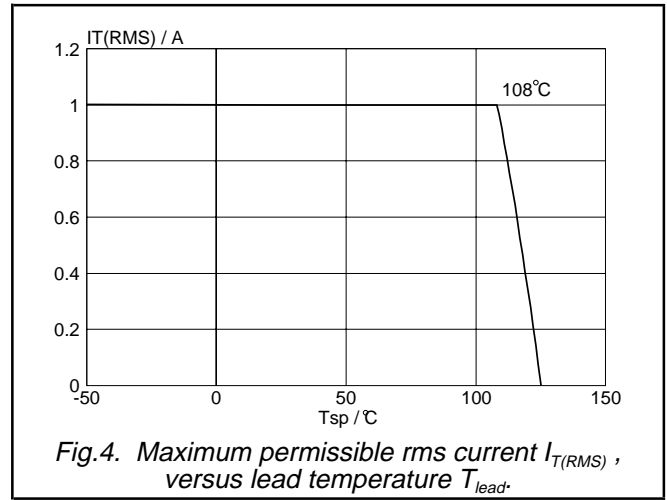
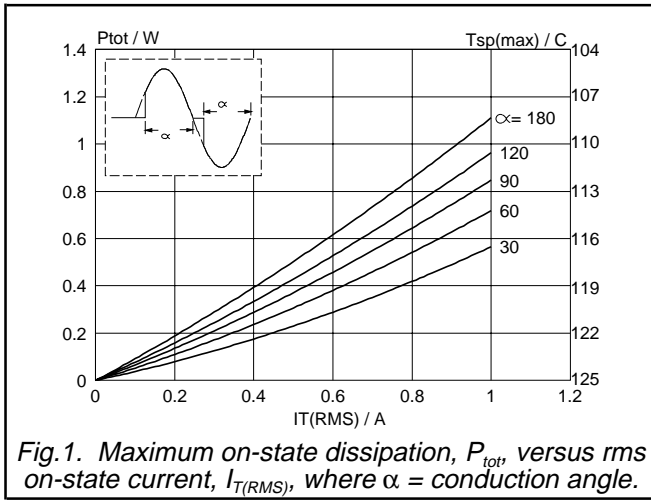
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point	full or half cycle	-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint pcb mounted; pad area as in fig:14	- -	156 70	- -	K/W K/W

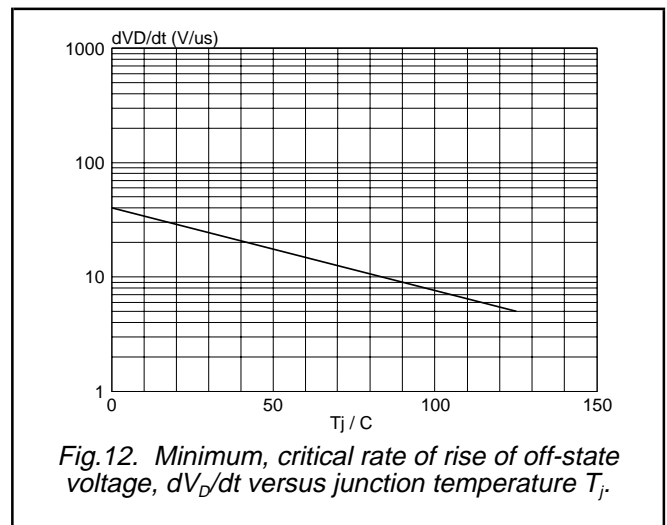
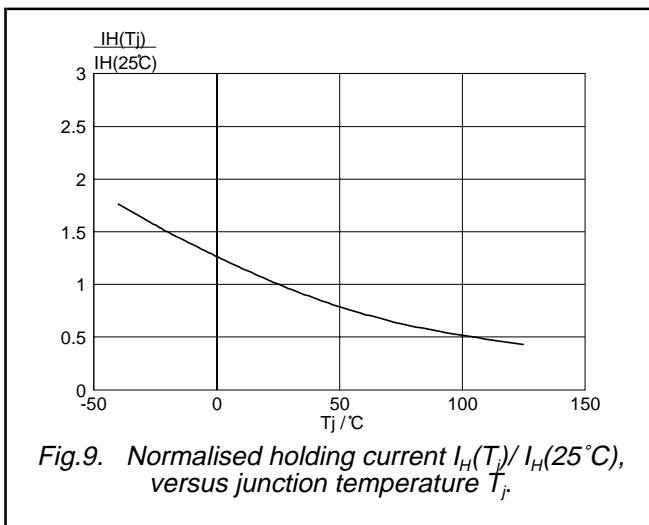
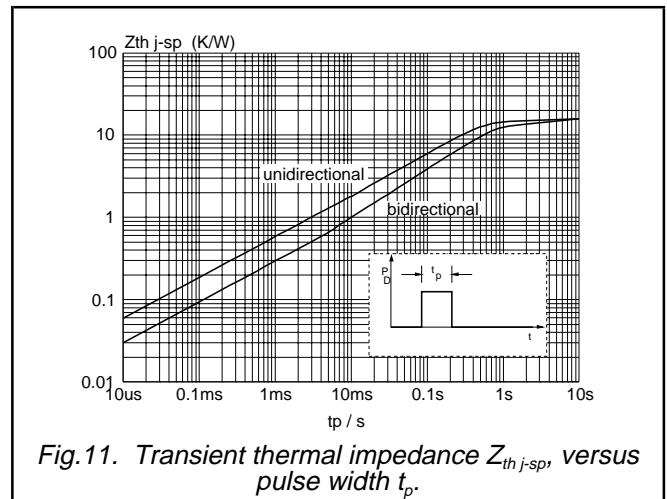
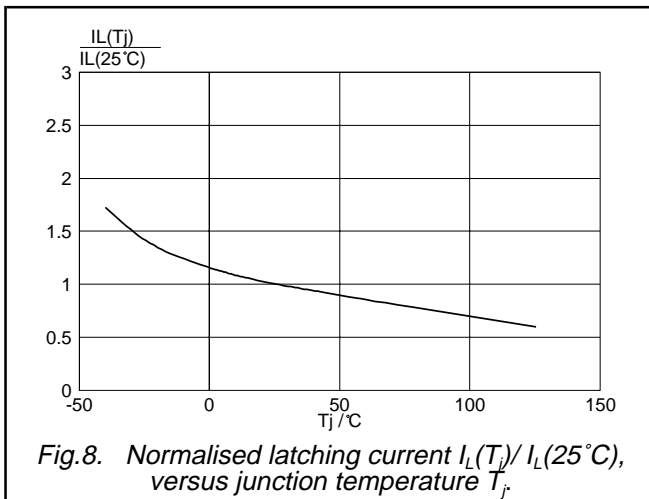
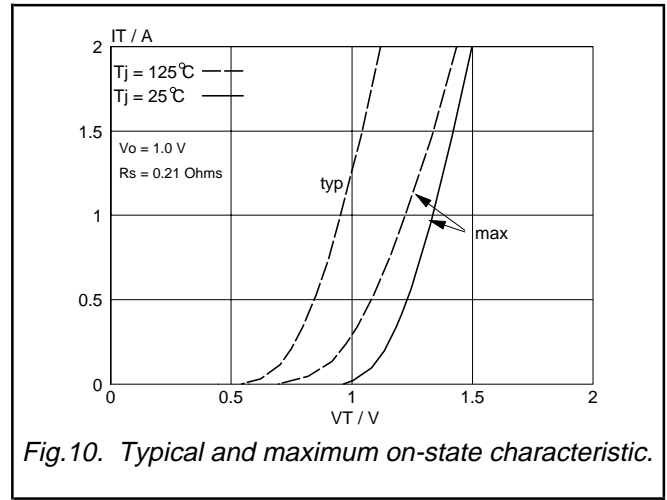
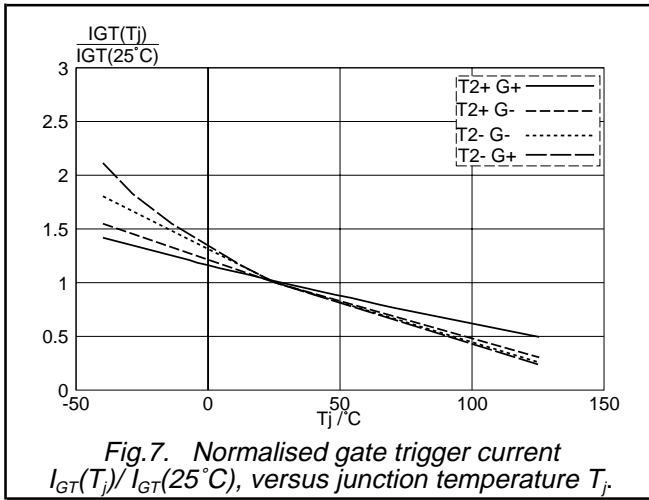
STATIC CHARACTERISTICS
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$				
		T2+ G+	-	0.4	3	mA
		T2+ G-	-	1.3	3	mA
		T2- G-	-	1.4	3	mA
		T2- G+	-	3.8	7	mA
I_L	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$				
		T2+ G+	-	1.2	5	mA
		T2+ G-	-	4.0	8	mA
		T2- G-	-	1.0	5	mA
		T2- G+	-	2.5	8	mA
I_H	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	1.3	5	mA
V_T	On-state voltage	$I_T = 2\text{ A}$	-	1.2	1.5	V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.7	1.5	V
I_D	Off-state leakage current	$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125\text{ }^\circ\text{C}$ $V_D = V_{DRM(max)}; T_j = 125\text{ }^\circ\text{C}$	0.2 -	0.3 0.1	- 0.5	V mA

DYNAMIC CHARACTERISTICS
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of change of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ }^\circ\text{C};$ exponential waveform; $R_{GK} = 1\text{ k}\Omega$	5	15	-	V/ μs
t_{gt}	Gate controlled turn-on time	$I_{TM} = 1.5\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $di_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μs





MOUNTING INSTRUCTIONS

Dimensions in mm.

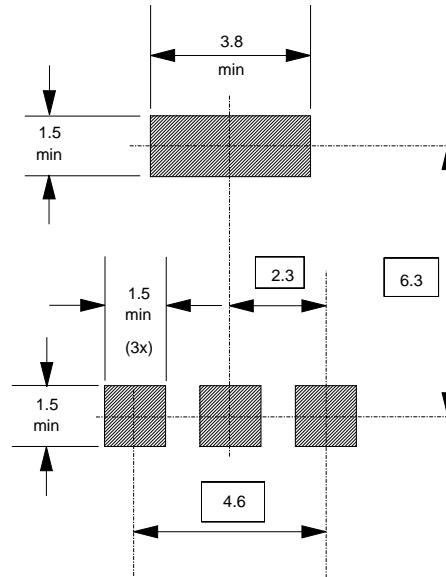
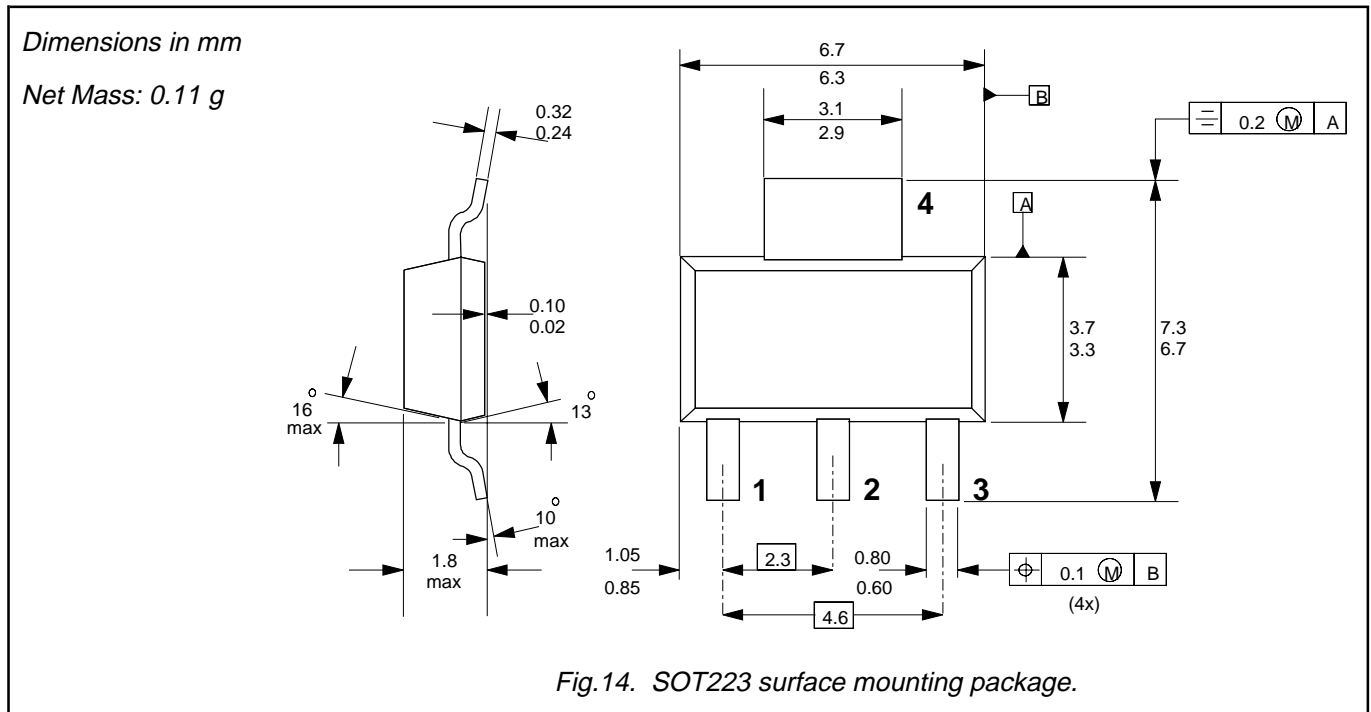


Fig.13. soldering pattern for surface mounting SOT223.

MECHANICAL DATA

Notes

1. For further information, refer to Philips publication SC18 " SMD Footprint Design and Soldering Guidelines".
 Order code: 9397 750 00505.
2. Epoxy meets UL94 V0 at 1/8".