

### ■ FEATURES

- Wide Vcc operation voltage :
  - C-grade: 1.8V~3.6V
  - I-grade: 1.9V~3.6V
  - (Vcc\_min.=1.65V at 25°C)
- Ultra low power consumption :
  - Vcc = 2.0V C-grade: 8mA (Max.) operating current  
I -grade: 10mA (Max.) operating current  
0.20uA (Typ.) CMOS standby current
  - Vcc = 3.0V C-grade: 11mA (Max.) operating current  
I -grade: 13mA (Max.) operating current  
0.30uA (Typ.) CMOS standby current
- High speed access time :
  - 85 85ns (Max.)
  - 10 100ns (Max.)
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation

- Easy expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- I/O Configuration x8/x16 selectable by LB and  $\overline{UB}$  pin
- Data retention supply voltage as low as 1.0V

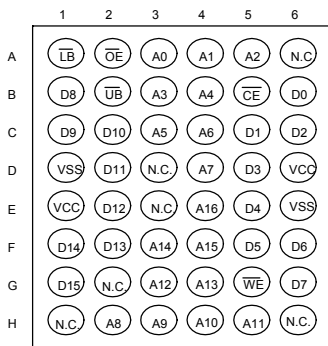
### ■ DESCRIPTION

The BS616UV2019 is a high performance, ultra low power CMOS Static Random Access Memory organized as 131,072 words by 16 bits and operates from a wide range of 1.8V to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.2uA at 2.0V/25°C and maximum access time of 85ns at 85°C. Easy memory expansion is provided by active LOW chip enable ( $\overline{CE}$ ), active LOW output enable ( $\overline{OE}$ ) and three-state output drivers. The BS616UV2019 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The BS616UV2019 is available in DICE form, JEDEC standard 48-pin TSOP Type I package and 48-ball BGA package.

### ■ PRODUCT FAMILY

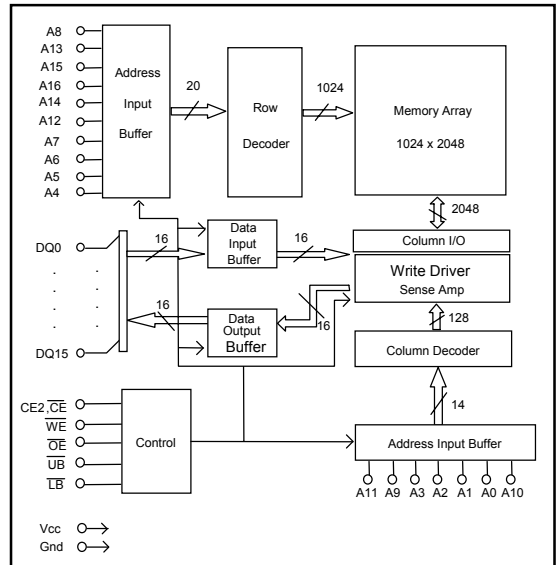
PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED ( ns )	POWER DISSIPATION				PKG TYPE
				STANDBY ( IccSB1, Max )		Operating ( Icc, Max )		
				Vcc=3.0V	Vcc=2.0V	Vcc=3.0V	Vcc=2.0V	
BS616UV2019DC	+0 °C to +70 °C	1.8V ~3.6V	85/100	3.0uA	2.0uA	11mA	8mA	DICE
BS616UV2019TC								TSOP1-48
BS616UV2019AC								BGA-48-0608
BS616UV2019DI	-40 °C to +85 °C	1.9V ~ 3.6V	85/100	5.0uA	3.0uA	13mA	10mA	DICE
BS616UV2019TI								TSOP1-48
BS616UV2019AI								BGA-48-0608

### ■ PIN CONFIGURATIONS



48-ball BGA top view

### ■ BLOCK DIAGRAM



**■ PIN DESCRIPTIONS**

Name	Function
<b>A0-A16 Address Input</b>	These 17 address inputs select one of the 131,072 x 16-bit words in the RAM.
<b><math>\overline{CE}</math> Chip Enable 1 Input CE2 Chip Enable 2 Input</b>	$\overline{CE}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected. (48B BGA ignore CE2 pin)
<b><math>\overline{WE}</math> Write Enable Input</b>	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
<b><math>\overline{OE}</math> Output Enable Input</b>	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
<b><math>\overline{LB}</math> and <math>\overline{UB}</math> Data Byte Control Input</b>	Lower byte and upper byte data input/output control pins.
<b>DQ0 - DQ15 Data Input/Output Ports</b>	These 16 bi-directional ports are used to read data from or write data into the RAM.
<b>Vcc</b>	Power Supply
<b>Gnd</b>	Ground

**■ TRUTH TABLE**

MODE	$\overline{CE}$	CE2 <sup>(1)</sup>	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	D0~D7	D8~D15	Vcc CURRENT
Not selected (Power Down)	H	X	X	X	X	X	High Z	High Z	$I_{CCSB}$ , $I_{CCSB1}$
	X	L	X	X	X	X	High Z	High Z	$I_{CCSB}$ , $I_{CCSB1}$
	X	X	X	X	H	H	High Z	High Z	$I_{CCSB}$ , $I_{CCSB1}$
Output Disabled	L	H	H	H	X	X	High Z	High Z	$I_{CC}$
Read	L	H	H	L	L	L	Dout	Dout	$I_{CC}$
					H	L	High Z	Dout	$I_{CC}$
					L	H	Dout	High Z	$I_{CC}$
Write	L	H	L	X	L	L	Din	Din	$I_{CC}$
					H	L	X	Din	$I_{CC}$
					L	H	Din	X	$I_{CC}$

1. 48B BGA ignore CE2 condition.

**■ ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

SYMBOL	PARAMETER	RATING	UNITS
V TERM	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T BIAS	Temperature Under Bias	-40 to +85	°C
T STG	Storage Temperature	-60 to +150	°C
P T	Power Dissipation	1.0	W
I OUT	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**■ OPERATING RANGE**

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0 °C to +70 °C	1.8V ~ 3.6V
Industrial	-40 °C to +85 °C	1.9V ~ 3.6V

**■ CAPACITANCE <sup>(1)</sup> (TA = 25°C, f = 1.0 MHz)**

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CDQ	Input/Output Capacitance	V/I/O=0V	8	pF

1. This parameter is guaranteed and not 100% tested.

**■ DC ELECTRICAL CHARACTERISTICS ( TA = -40 to + 85°C )**

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
VIL	Guaranteed Input Low Voltage <sup>(2)</sup>		Vcc=2.0V	-0.3 <sup>(6)</sup>	--	0.6
			Vcc=3.0V		0.8	
VIH	Guaranteed Input High Voltage <sup>(2)</sup>		Vcc=2.0V	1.4	--	Vcc+0.3
			Vcc=3.0V			
IIL	Input Leakage Current	Vcc = Max, VIN = 0V to Vcc	--	--	1	uA
ILO	Output Leakage Current	Vcc = Max, CE = VIH, or CE2 <sup>(4)</sup> = VIL, or OE = VIH, VIO = 0V to Vcc	--	--	1	uA
VOL	Output Low Voltage	IOL = 0.1mA ; Vcc=Max	Vcc=2.0V	--	--	0.2
		IOL = 2.0mA ; Vcc=Max	Vcc=3.0V	--	--	0.4
VOH	Output High Voltage	Ioh = -0.1mA ; Vcc=Min	Vcc=2.0V	Vcc-0.2	--	--
		Ioh = -1.0mA ; Vcc=Min	Vcc=3.0V	2.4	--	--
ICC	Operating Power Supply Current	CE = VIL <sup>(4)</sup> , Idd = 0mA, F = Fmax <sup>(3)</sup>	Vcc=2.0V	--	--	10
			Vcc=3.0V	--	--	13
ICCSB	Standby Current TTL	CE = VIH or CE2 = VIL <sup>(4)</sup> , Idd = 0mA	Vcc=2.0V	--	--	0.1
			Vcc=3.0V	--	--	0.5
ICCSB1 <sup>(5)</sup>	Standby Current CMOS	CE ≥ Vcc-0.2V, or CE2 ≤ 0.2V <sup>(4)</sup> VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V	Vcc=2.0V	--	0.20	3.0
			Vcc=3.0V	--	0.30	5.0

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3. Fmax = 1/tRC.

4. 48B BGA ignore CE2 condition.

5. ICCSB1 is 2.0uA/3.0uA at Vcc=2.0V/3.0V and TA=70°C.

6. VIL = -1.5V for pulse width less than 30ns

**■ DATA RETENTION CHARACTERISTICS ( TA = -40 to + 85°C )**

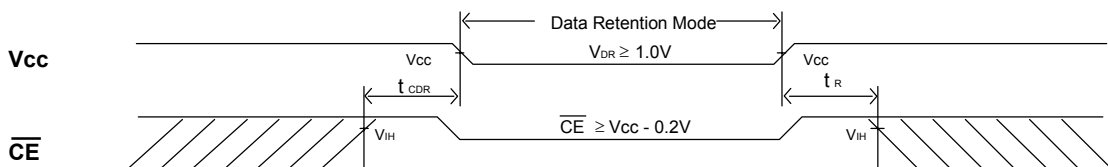
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
VDR	Vcc for Data Retention	CE ≥ Vcc - 0.2V or CE2 ≤ 0.2V <sup>(3)</sup> VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V	1.0	--	--	V
ICCDR <sup>(4)</sup>	Data Retention Current	CE ≥ Vcc - 0.2V or CE2 ≤ 0.2V <sup>(3)</sup> VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V	--	0.1	1.0	uA
tCDR	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
tR	Operation Recovery Time		TRC <sup>(2)</sup>	--	--	ns

1. Vcc = 1.0V, TA = + 25°C

2. tRC = Read Cycle Time

3. 48B BGA ignore CE2 condition.



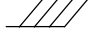


4. ICCDR is 0.7uA at TA=70°C.

**■ LOW  $V_{CC}$  DATA RETENTION WAVEFORM (  $\overline{CE}$  Controlled )**

**■ AC TEST CONDITIONS**

(Test Load and Input/Output Reference)

Input Pulse Levels	$V_{CC} / 0V$
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5V <sub>CC</sub>
Output Load	$C_L = 100pF + 1TTL$ $C_L = 30pF + 1TTL$

**■ KEY TO SWITCHING WAVEFORMS**

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

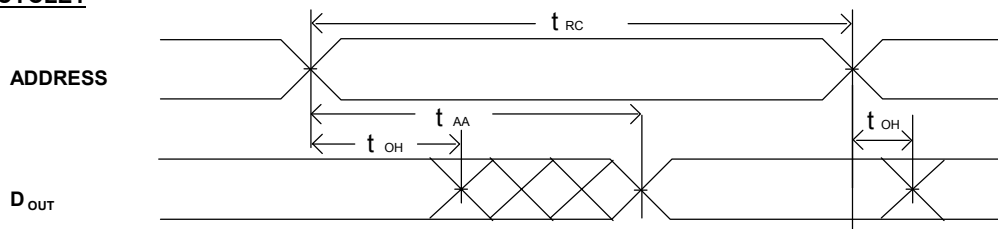
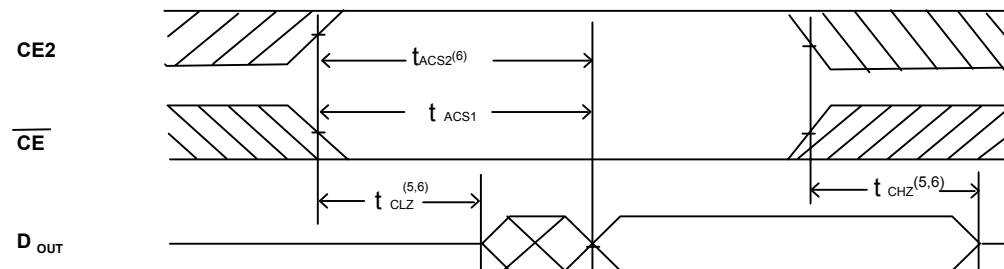
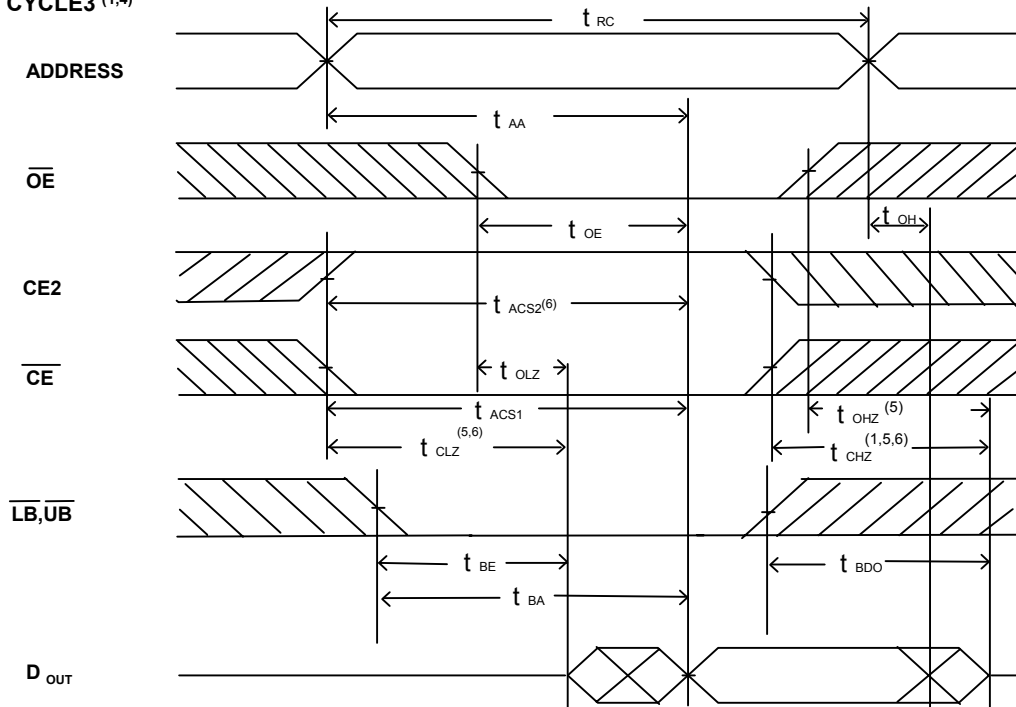
**■ AC ELECTRICAL CHARACTERISTICS (  $T_A = -40$  to  $+85^\circ C$  )**

READ CYCLE ( 48B BGA ignore CE2 condition)

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 100ns ( $V_{CC} = 1.9-3.6V$ )			CYCLE TIME : 85ns ( $V_{CC} = 1.9-3.6V$ )			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{RC}$	Read Cycle Time	100	--	--	85	--	--	ns
$t_{AVQV}$	$t_{AA}$	Address Access Time	--	--	100	--	--	85	ns
$t_{ELQV}$	$t_{ACS1,2}$	Chip Select Access Time ( $\overline{CE}, CE2$ )	--	--	100	--	--	85	ns
$t_{BA}$	$t_{BA}^{(1)}$	Data Byte Control Access Time ( $\overline{LB}, \overline{UB}$ )	--	--	50	--	--	40	ns
$t_{GLQV}$	$t_{OE}$	Output Enable to Output Valid	--	--	50	--	--	40	ns
$t_{E1LQX}$	$t_{CLZ}$	Chip Select to Output Low Z ( $\overline{CE}, CE2$ )	15	--	--	15	--	--	ns
$t_{BE}$	$t_{BE}$	Data Byte Control to Output Low Z ( $\overline{LB}, \overline{UB}$ )	15	--	--	15	--	--	ns
$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output in Low Z	15	--	--	15	--	--	ns
$t_{EHQZ}$	$t_{CHZ}$	Chip Deselect to Output in High Z ( $\overline{CE}, CE2$ )	--	--	40	--	--	35	ns
$t_{BDO}$	$t_{BDO}$	Data Byte Control to Output High Z ( $\overline{LB}, \overline{UB}$ )	--	--	40	--	--	35	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	--	--	35	--	--	30	ns
$t_{AXOX}$	$t_{OH}$	Data Hold from Address Change	15	--	--	15	--	--	ns

NOTE :

 1.  $t_{BA}$  is 50ns/40ns (@speed=100ns/85ns) with address toggle. ;  $t_{BA}$  is 100ns/85ns (@speed=100ns/85ns) without address toggle.

**■ SWITCHING WAVEFORMS (READ CYCLE)**
**READ CYCLE1 (1,2,4)**

**READ CYCLE2 (1,3,4)**

**READ CYCLE3 (1,4)**

**NOTES:**

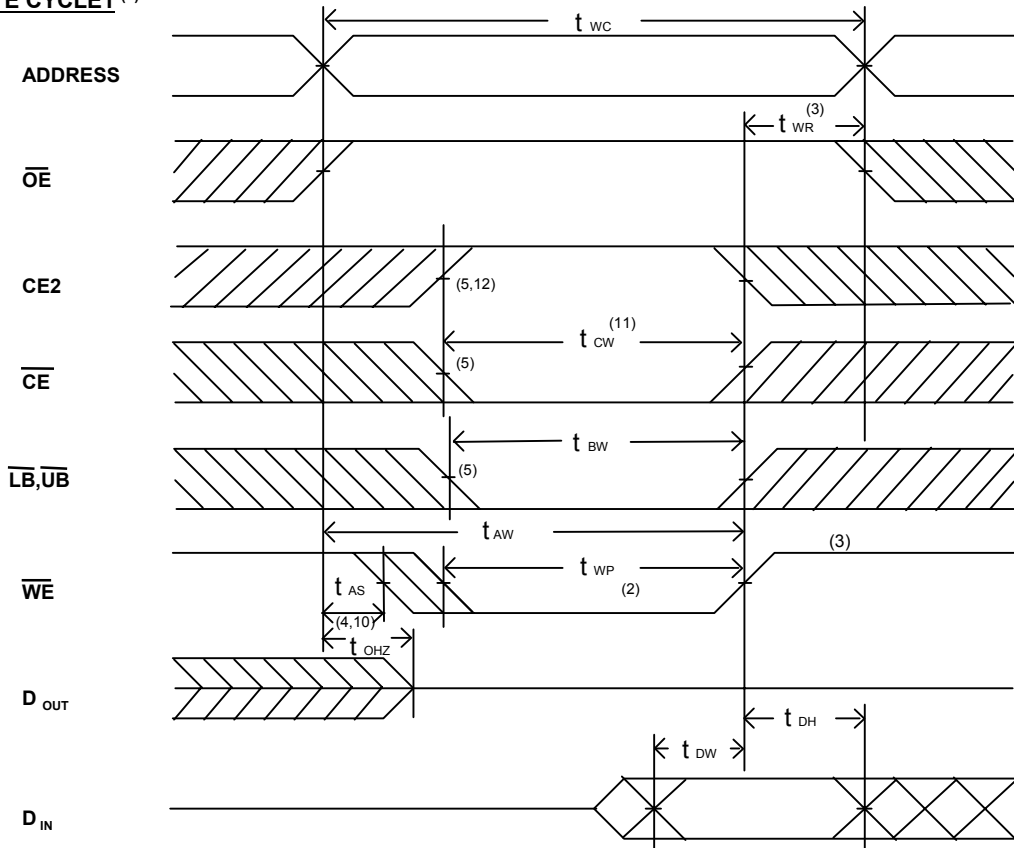
1. WE is high in read Cycle.
2. Device is continuously selected when  $\overline{CE} = V_{IL}$  and  $CE2 = V_{IH}$ .
3. Address valid prior to or coincident with CE transition low.
4.  $OE = V_{IL}$ .
5. The parameter is guaranteed but not 100% tested.
6. 48B BGA ignore this parameters related to CE2.

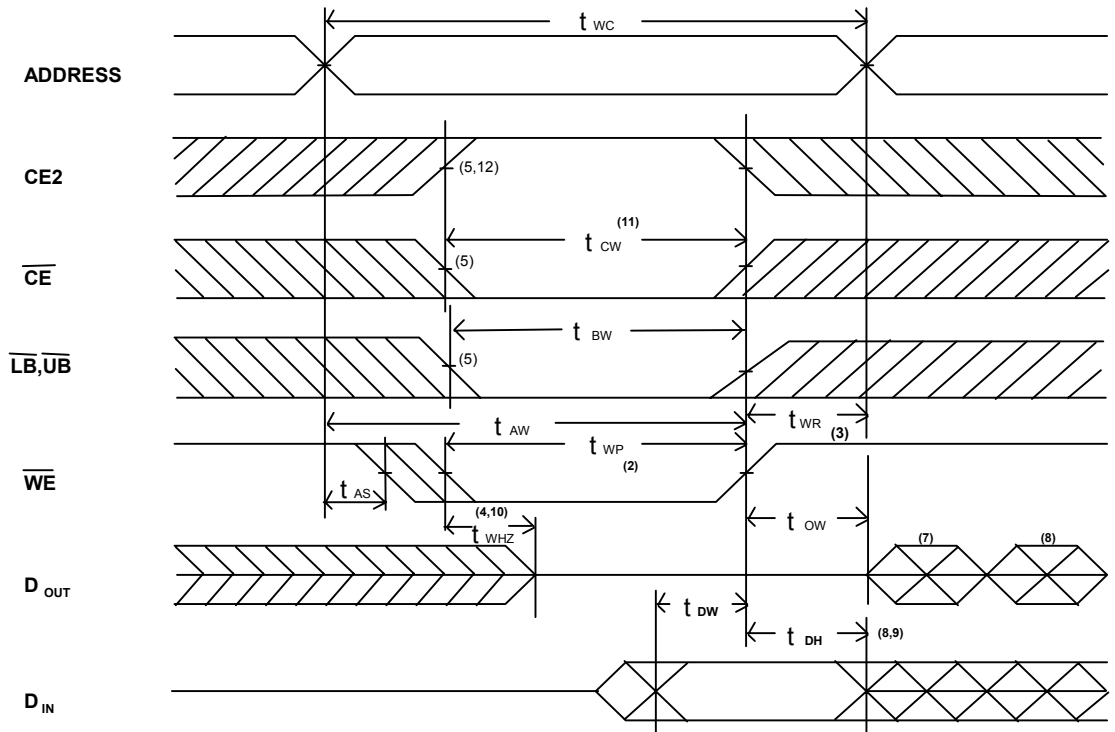
**■ AC ELECTRICAL CHARACTERISTICS ( TA = -40 to + 85°C )**
**WRITE CYCLE ( 48B BGA ignore CE2 condition)**

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 100ns (Vcc = 1.9-3.6V)			CYCLE TIME : 85ns (Vcc = 1.9-3.6V)			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{WC}$	Write Cycle Time	100	--	--	85	--	--	ns
$t_{E1LWH}$	$t_{CW}$	Chip Select to End of Write ( $\overline{CE}, \overline{CE2}$ )	100	--	--	85	--	--	ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	0	--	--	0	--	--	ns
$t_{AVWH}$	$t_{AW}$	Address Valid to End of Write	100	--	--	85	--	--	ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	50	--	--	40	--	--	ns
$t_{WHAX}$	$t_{WR}$	Write recovery Time ( $\overline{CE}, \overline{CE2}, \overline{WE}$ )	0	--	--	0	--	--	ns
$t_{BW}$	$t_{BW}^{(1)}$	Date Byte Control to End of Write ( $\overline{LB}, \overline{UB}$ )	40	--	--	35	--	--	ns
$t_{WLQZ}$	$t_{WHZ}$	Write to Output in High Z	--	--	40	--	--	35	ns
$t_{DVWH}$	$t_{DW}$	Data to Write Time Overlap	40	--	--	35	--	--	ns
$t_{WHDX}$	$t_{DH}$	Data Hold from Write Time	0	--	--	0	--	--	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	--	--	40	--	--	35	ns
$t_{WHOX}$	$t_{ow}$	End of Write to Output Active	10	--	--	10	--	--	ns

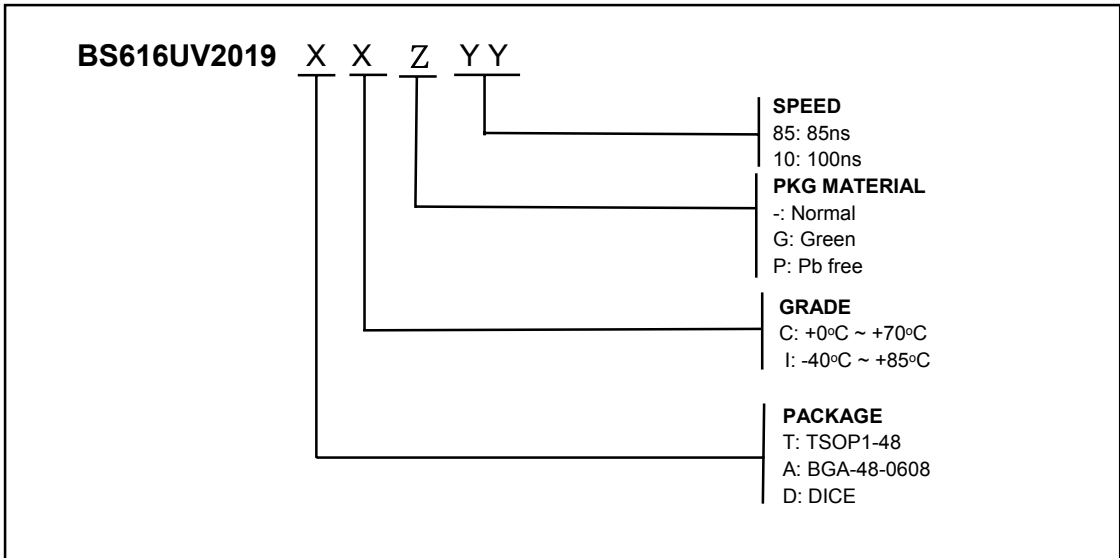
NOTE :

 1.  $t_{BW}$  is 40ns/35ns (@speed=100ns/85ns) with address toggle. ;  $t_{BW}$  is 100ns/85ns (@speed=100ns/85ns) without address toggle.

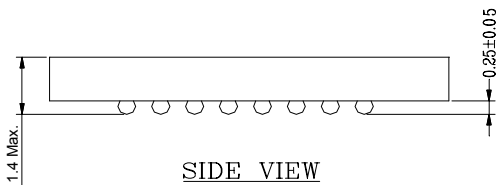
**■ SWITCHING WAVEFORMS (WRITE CYCLE)**
**WRITE CYCLE1<sup>(1)</sup>**


**WRITE CYCLE2 (1,6)**

**NOTES:**

1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE2,  $\overline{CE}$  and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $t_{WR}$  is measured from the earlier of CE2 going low, or  $\overline{CE}$  or  $\overline{WE}$  going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE2 high transition or  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, output remain in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7. DOUT is the same phase of write data of this write cycle.
8. DOUT is the read data of next address.
9. If CE2 is high or  $\overline{CE}$  is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. The parameter is guaranteed but not 100% tested.
11.  $t_{CW}$  is measured from the later of CE2 going high or  $\overline{CE}$  going low to the end of write.
12. 48B BGA ignore this parameters related to CE2.

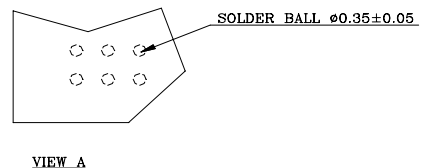
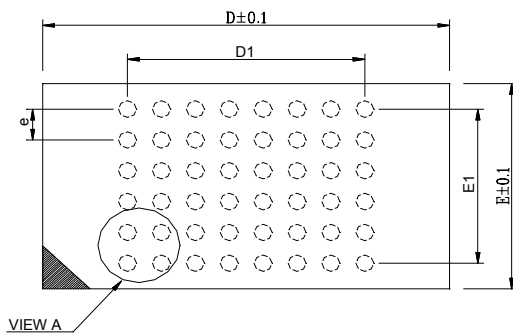
**■ ORDERING INFORMATION**


Note:  
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**■ PACKAGE DIMENSIONS**


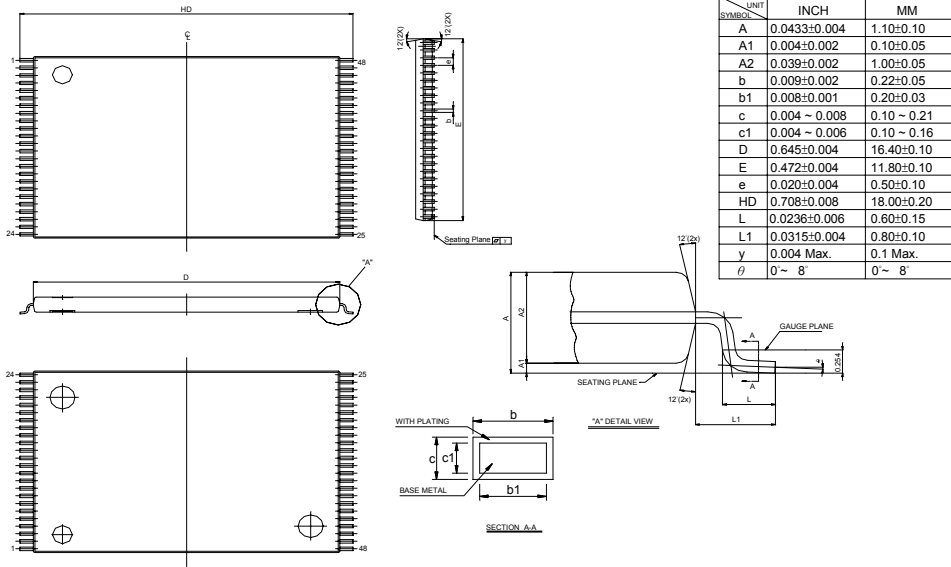
- NOTES:
- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
  - 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
  - 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75



*48 mini-BGA (6 x 8)*



**■ PACKAGE DIMENSIONS**

**TSOP1-48PIN**