



# Very Low Power/Voltage CMOS SRAM 128K X 16 bit

## BS616LV2012

### FEATURES

- Very low operation voltage : 2.7 ~ 3.6V
- Very low power consumption :
  - V<sub>cc</sub> = 3.0V C-grade: 30mA (Max.) operating current
  - I-grade: 35mA (Max.) operating current
  - 0.15uA (Typ.) CMOS standby current
- High speed access time :
  - 70 70ns (Max.) at V<sub>cc</sub> = 3.0V
  - 10 100ns (Max.) at V<sub>cc</sub> = 3.0V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- I/O Configuration x8/x16 selectable by  $\overline{LB}$  and  $\overline{UB}$  pin

### DESCRIPTION

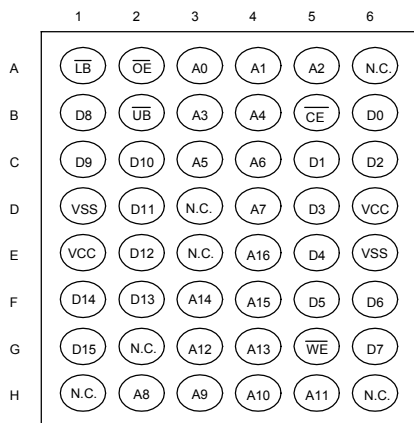
The BS616LV2012 is a high performance, very low power CMOS Static Random Access Memory organized as 131,072 words by 16 bits and operates from a wide range of 2.7V to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.15uA and maximum access time of 70/100ns in 3V operation. Easy memory expansion is provided by active LOW chip enable( $\overline{CE}$ ), active LOW output enable( $\overline{OE}$ ) and three-state output drivers.

The BS616LV2012 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The BS616LV2012 is available in DICE form, JEDEC standard 48-pin TSOP Type I package and 48-pin BGA type.

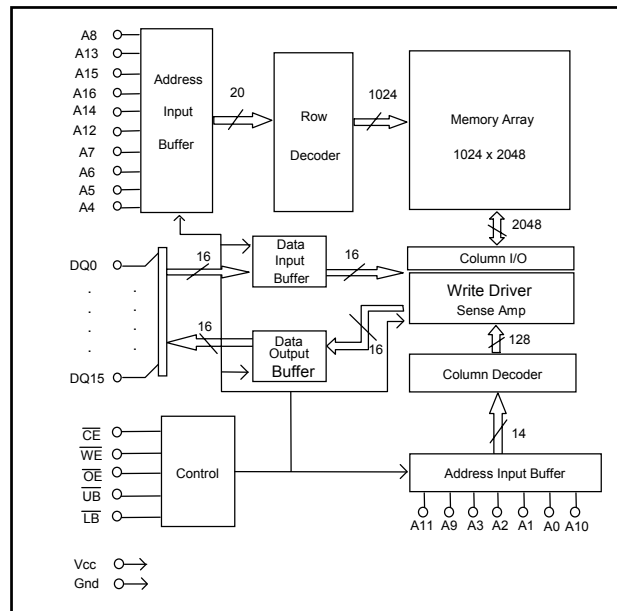
### PRODUCT FAMILY

PRODUCT FAMILY	OPERATING TEMPERATURE	V <sub>cc</sub> RANGE	SPEED (ns) V <sub>cc</sub> =3.0V	POWER DISSIPATION		PKG TYPE
				STANDBY (I <sub>ccsB1, Max</sub> ) V <sub>cc</sub> =3.0V	Operating (I <sub>cc, Max</sub> ) V <sub>cc</sub> =3.0V	
BS616LV2012DC	+0 °C to +70 °C	2.7V ~ 3.6V	70 / 100	8uA	30mA	DICE
BS616LV2012TC						TSOP1-48
BS616LV2012AC						BGA-48-0608
BS616LV2012DI	-40 °C to +85 °C	2.7V ~ 3.6V	70 / 100	12uA	35mA	DICE
BS616LV2012TI						TSOP1-48
BS616LV2012AI						BGA-48-0608

### PIN CONFIGURATIONS



### BLOCK DIAGRAM



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**■ PIN DESCRIPTIONS**

Name	Function
<b>A0-A16 Address Input</b>	These 17 address inputs select one of the 131,072 x 16-bit words in the RAM.
<b><math>\overline{CE}</math> Chip Enable Input</b>	$\overline{CE}$ is active LOW. Chip enables must be active when data read from or write to the device. If chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
<b><math>\overline{WE}</math> Write Enable Input</b>	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
<b><math>\overline{OE}</math> Output Enable Input</b>	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
<b><math>\overline{LB}</math> and <math>\overline{UB}</math> Data Byte Control Input</b>	Lower byte and upper byte data input/output control pins.
<b>DQ0 - DQ15 Data Input/Output Ports</b>	These 16 bi-directional ports are used to read data from or write data into the RAM.
<b>Vcc</b>	Power Supply
<b>Gnd</b>	Ground

**■ TRUTH TABLE**

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ0~DQ7	DQ8~DQ15	Vcc CURRENT
Not selected (Power Down)	H	X	X	X	X	High Z	High Z	$I_{CCSB}$ , $I_{CCSB1}$
Output Disabled	L	H	H	X	X	High Z	High Z	$I_{CC}$
Read	L	H	L	L	L	Dout	Dout	$I_{CC}$
				H	L	High Z	Dout	$I_{CC}$
				L	H	Dout	High Z	$I_{CC}$
Write	L	L	X	L	L	Din	Din	$I_{CC}$
				H	L	X	Din	$I_{CC}$
				L	H	Din	X	$I_{CC}$

**■ ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

SYMBOL	PARAMETER	RATING	UNITS
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>BIAS</sub>	Temperature Under Bias	-40 to +125	°C
T <sub>STG</sub>	Storage Temperature	-60 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**■ OPERATING RANGE**

RANGE	AMBIENT TEMPERATURE	V <sub>CC</sub>
Commercial	0 °C to +70 °C	2.7V ~ 3.6V
Industrial	-40 °C to +85 °C	2.7V ~ 3.6V

**■ CAPACITANCE <sup>(1)</sup> (TA = 25°C, f = 1.0 MHz)**

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	6	pF
C <sub>DQ</sub>	Input/Output Capacitance	V <sub>I/O</sub> =0V	8	pF

1. This parameter is guaranteed and not tested.

**■ DC ELECTRICAL CHARACTERISTICS ( TA = 0 to + 70°C )**

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
V <sub>IL</sub>	Guaranteed Input Low Voltage <sup>(2)</sup>	V <sub>CC</sub> =3.0V	-0.5	--	0.8	V
V <sub>IH</sub>	Guaranteed Input High Voltage <sup>(2)</sup>	V <sub>CC</sub> =3.0V	2.0	--	V <sub>CC</sub> +0.2	V
I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0V to V <sub>CC</sub>	--	--	1	uA
I <sub>OL</sub>	Output Leakage Current	V <sub>CC</sub> = Max, $\overline{CE} = V_{IH}$ , or $\overline{OE} = V_{IH}$ , V <sub>I/O</sub> = 0V to V <sub>CC</sub>	--	--	1	uA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Max, I <sub>OL</sub> = 2mA	--	--	0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1mA	2.4	--	--	V
I <sub>CC</sub>	Operating Power Supply Current	$\overline{CE} = V_{IL}$ , I <sub>DQ</sub> = 0mA, F = F <sub>max</sub> <sup>(3)</sup>	--	--	30	mA
I <sub>CCSB</sub>	Standby Current-TTL	$\overline{CE} = V_{IH}$ , I <sub>DQ</sub> = 0mA	--	--	1	mA
I <sub>CCSB1</sub>	Standby Current-CMOS	$\overline{CE} \geq V_{CC}-0.2V$ , V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$	--	0.15	8	uA

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

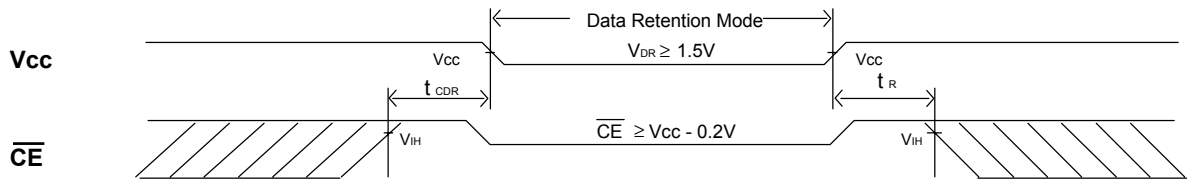
3. F<sub>max</sub> = 1/t<sub>RC</sub>.

**■ DATA RETENTION CHARACTERISTICS ( TA = 0 to + 70°C )**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	$\overline{CE} \geq V_{CC} - 0.2V$ V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$	1.5	--	--	V
I <sub>CCDR</sub>	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$	--	0.1	5	uA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t <sub>R</sub>	Operation Recovery Time		T <sub>RC</sub> <sup>(2)</sup>	--	--	ns

1. V<sub>CC</sub> = 1.5V, T<sub>A</sub> = + 25°C

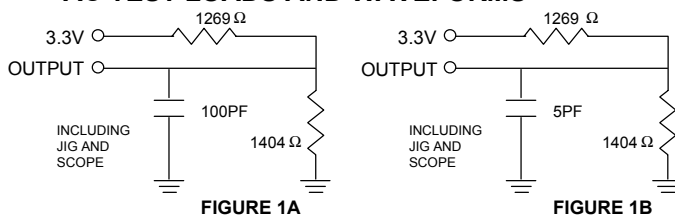
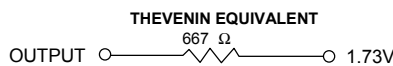
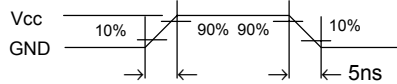
2. t<sub>RC</sub> = Read Cycle Time

**■ LOW  $V_{CC}$  DATA RETENTION WAVEFORM (  $\overline{CE}$  Controlled )**

**■ AC TEST CONDITIONS**

Input Pulse Levels	$V_{CC}/0V$
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	$0.5V_{CC}$

**■ KEY TO SWITCHING WAVEFORMS**

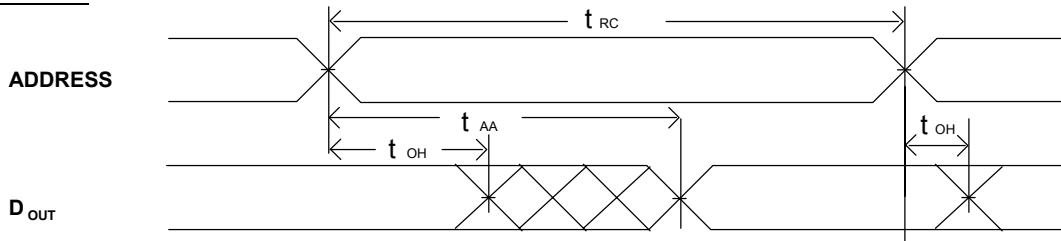
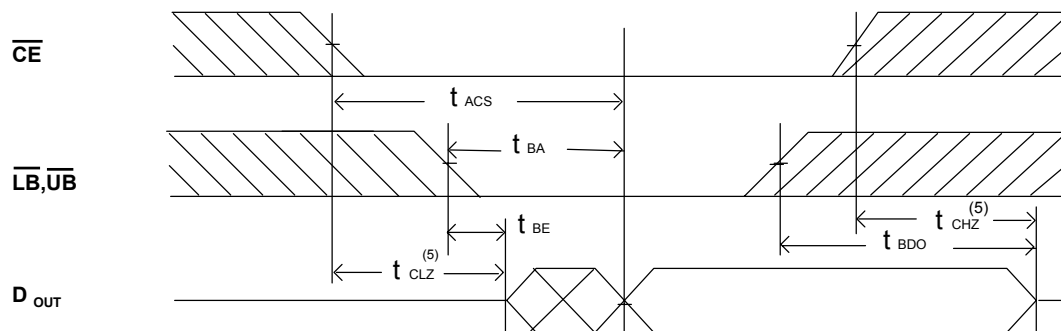
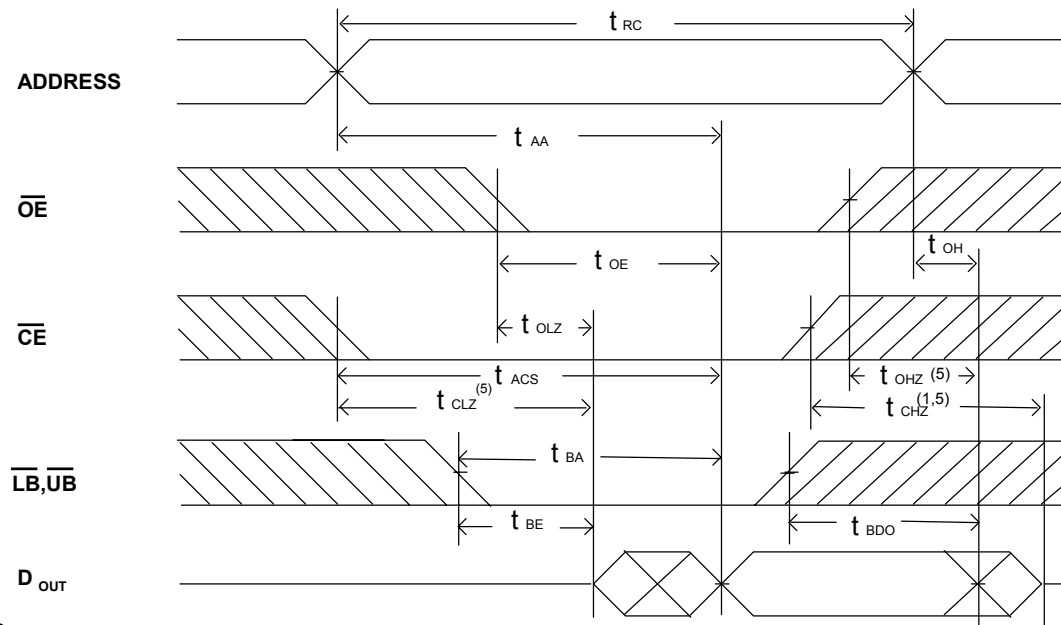
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

**■ AC TEST LOADS AND WAVEFORMS**

**FIGURE 1A**
**FIGURE 1B**

**THEVENIN EQUIVALENT**

**FIGURE 2**
**■ AC ELECTRICAL CHARACTERISTICS (  $T_A = 0$  to  $+70^\circ C$  ,  $V_{CC} = 3.0V$  )**
**READ CYCLE**

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616LV2012-70			BS616LV2012-10			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{RC}$	Read Cycle Time	70	--	--	100	--	--	ns
$t_{AVQV}$	$t_{AA}$	Address Access Time	--	--	70	--	--	100	ns
$t_{ELQV}$	$t_{ACS}$	Chip Select Access Time ( $\overline{CE}$ )	--	--	70	--	--	100	ns
$t_{BA}$	$t_{BA}^{(1)}$	Data Byte Control Access Time ( $\overline{LB}, \overline{UB}$ )	--	--	35	--	--	50	ns
$t_{GLQV}$	$t_{OE}$	Output Enable to Output Valid	--	--	35	--	--	50	ns
$t_{E1LQX}$	$t_{CLZ}$	Chip Select to Output Low Z ( $\overline{CE}$ )	10	--	--	15	--	--	ns
$t_{BE}$	$t_{BE}$	Data Byte Control to Output Low Z ( $\overline{LB}, \overline{UB}$ )	10	--	--	15	--	--	ns
$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output in Low Z	10	--	--	15	--	--	ns
$t_{EHQZ}$	$t_{CHZ}$	Chip Deselect to Output in High Z ( $\overline{CE}$ )	0	--	35	0	--	40	ns
$t_{BDO}$	$t_{BDO}$	Data Byte Control to Output High Z ( $\overline{LB}, \overline{UB}$ )	0	--	35	0	--	40	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	0	--	30	0	--	35	ns
$t_{AXOX}$	$t_{OH}$	Output Disable to Address Change	10	--	--	15	--	--	ns

NOTE :

 1.  $t_{BA}$  is 35ns/50ns (@speed=70ns/100ns) with address toggle. ;  $t_{BA}$  is 70ns/100ns (@speed=70ns/100ns) without address toggle.

**■ SWITCHING WAVEFORMS (READ CYCLE)**
**READ CYCLE1 (1,2,4)**

**READ CYCLE2 (1,3,4)**

**READ CYCLE3 (1,4)**

**NOTES:**

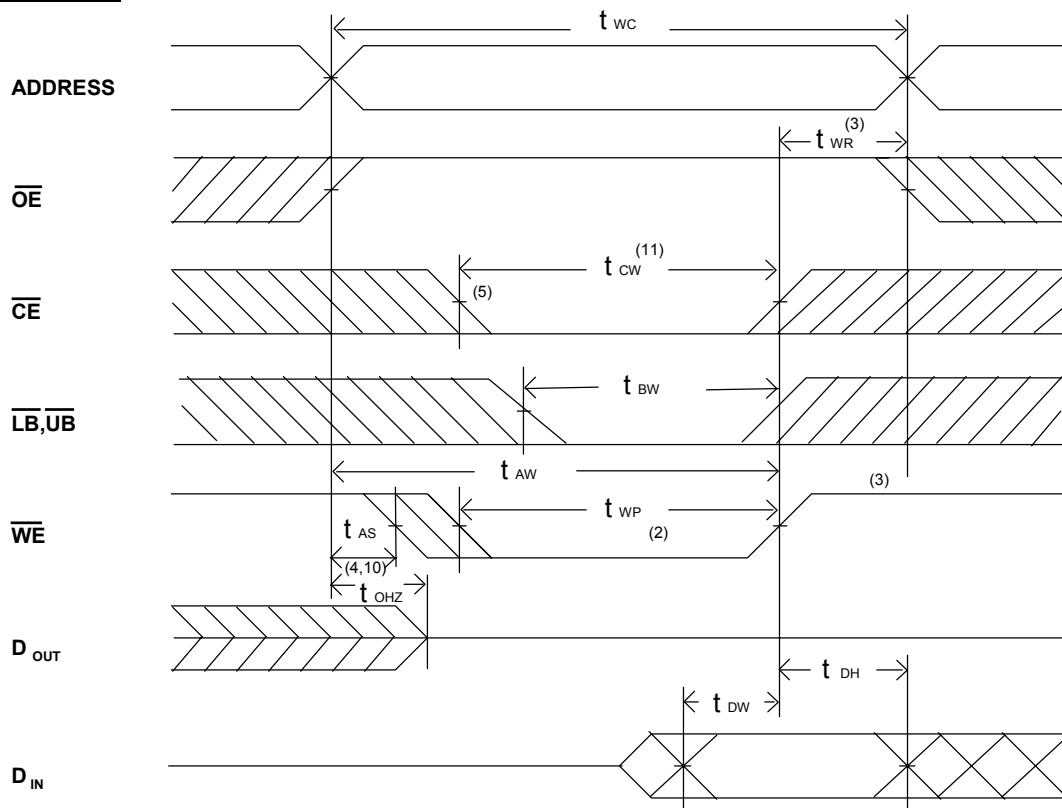
1. WE is high for read Cycle.
2. Device is continuously selected when  $\overline{CE} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CE}$  transition low.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$  as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

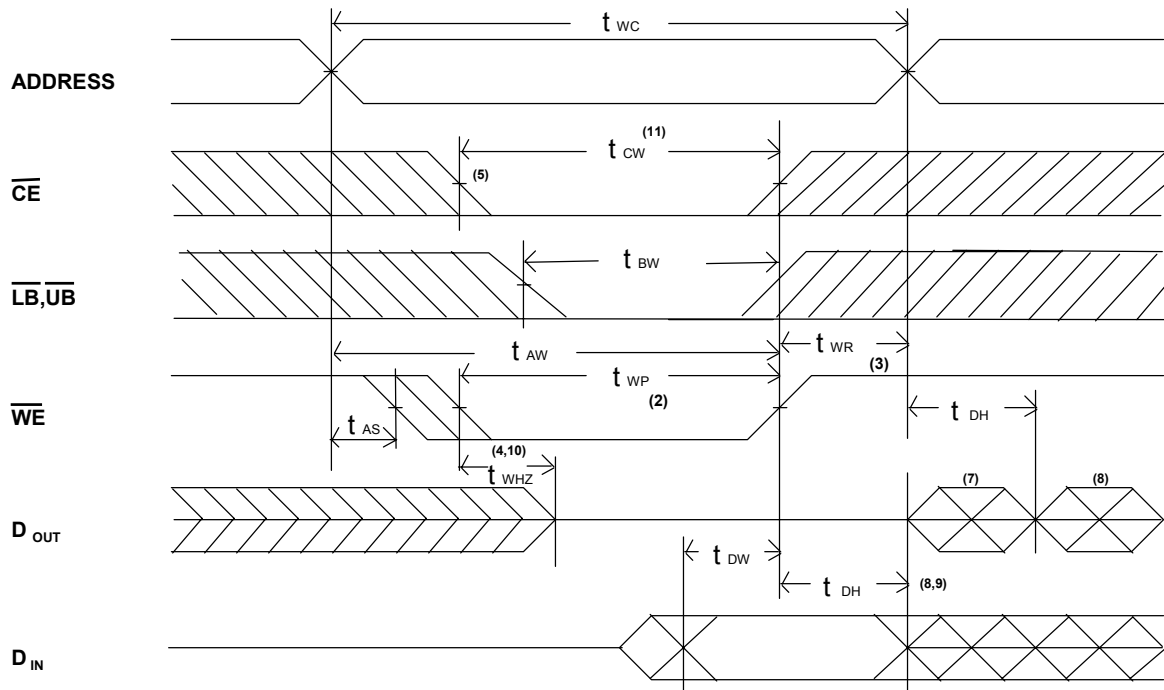
**■ AC ELECTRICAL CHARACTERISTICS ( TA = 0 to + 70°C , Vcc = 3.0V )**
**WRITE CYCLE**

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616LV2012-70			BS616LV2012-10			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{WC}$	Write Cycle Time	70	--	--	100	--	--	ns
$t_{E1LWH}$	$t_{CW}$	Chip Select to End of Write	70	--	--	100	--	--	ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	0	--	--	0	--	--	ns
$t_{AVWH}$	$t_{AW}$	Address Valid to End of Write	70	--	--	100	--	--	ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	35	--	--	50	--	--	ns
$t_{WHAX}$	$t_{WR}$	Write recovery Time ( $\overline{CE}, \overline{WE}$ )	0	--	--	0	--	--	ns
$t_{BW}$	$t_{BW}^{(1)}$	Data Byte Control to End of Write ( $\overline{LB}, \overline{UB}$ )	30	--	--	40	--	--	ns
$t_{WLQZ}$	$t_{WHZ}$	Write to Output in High Z	0	--	30	0	--	40	ns
$t_{DVWH}$	$t_{DW}$	Data to Write Time Overlap	30	--	--	40	--	--	ns
$t_{WHDX}$	$t_{DH}$	Data Hold from Write Time	0	--	--	0	--	--	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	0	--	30	0	--	40	ns
$t_{WHOX}$	$t_{OW}$	End of Write to Output Active	5	--	--	10	--	--	ns

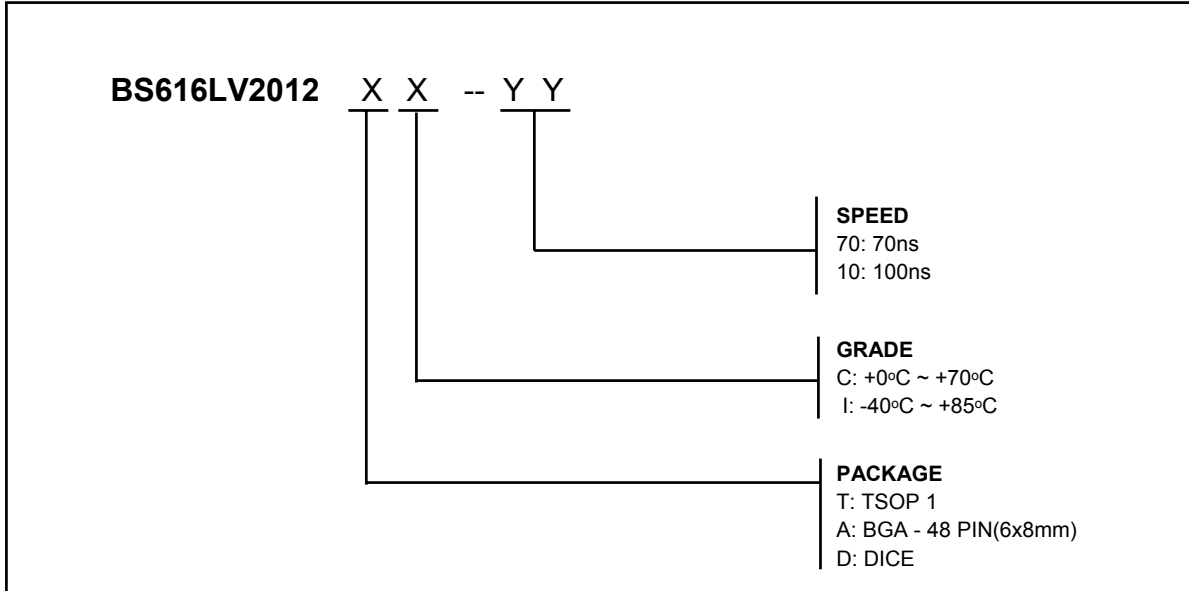
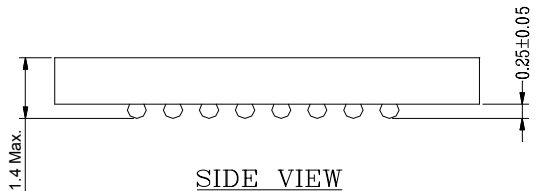
NOTE :

 1.  $t_{BW}$  is 30ns/40ns (@speed=70ns/100ns) with address toggle. ;  $t_{BW}$  is 70ns/100ns (@speed=70ns/100ns) without address toggle.

**■ SWITCHING WAVEFORMS (WRITE CYCLE)**
**WRITE CYCLE1<sup>(1)</sup>**


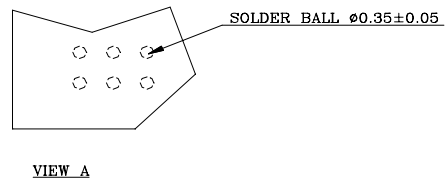
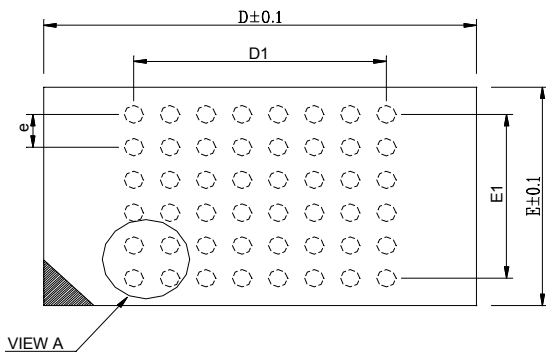
**WRITE CYCLE2 (1,6)**

**NOTES:**

1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, output remain in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7.  $D_{OUT}$  is the same phase of write data of this write cycle.
8.  $D_{OUT}$  is the read data of next address.
9. If  $\overline{CE}$  is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$  as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11.  $t_{CW}$  is measured from the later of  $\overline{CE}$  going low to the end of write.

**ORDERING INFORMATION**

**PACKAGE DIMENSIONS**

**NOTES:**

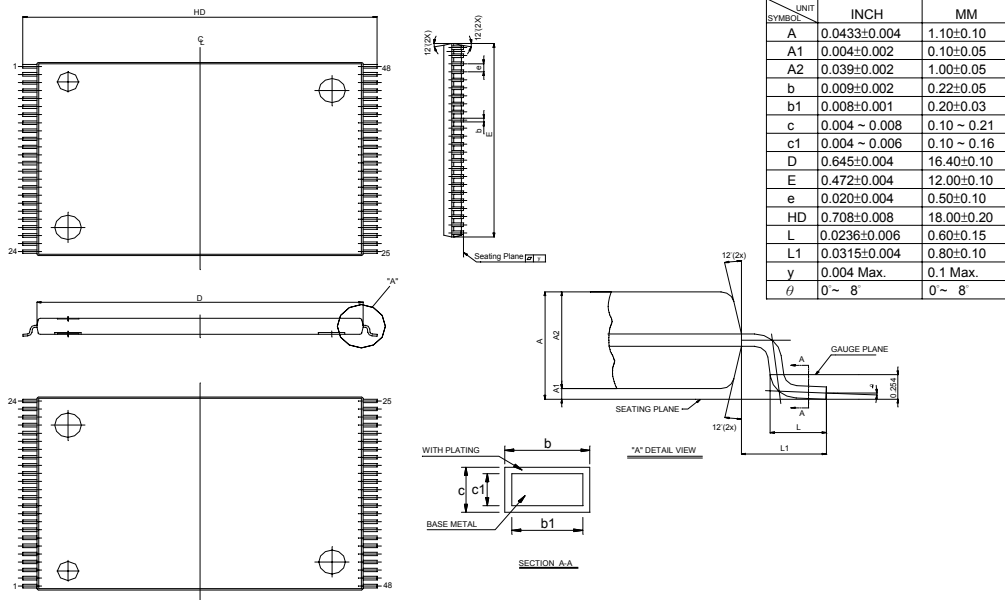
- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
- 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75



*48 mini-BGA (6 x 8)*



**■ PACKAGE DIMENSIONS**

**TSOP1-48PIN**


***REVISION HISTORY***

<b>Revision</b>	<b>Description</b>	<b>Date</b>	<b>Note</b>
<b>2.2</b>	<b>2001 Data Sheet release</b>	<b>Apr. 15, 2001</b>	
<b>2.3</b>	<b>Modify CSP Pin Configuration Pin number : E3 “ VSS ” rename to “ N.C. “</b>	<b>Sep.12, 2001</b>	
<b>2.4</b>	<b>Modify some AC parameters</b>	<b>April,12,2002</b>	