Very Low Power/Voltage CMOS SRAM
1M x 16 or 2M x 8 bit switchable

BS616LV1623

■ FEATURES

- Vcc operation voltage : 2.7 ~ 3.6V
- Very low power consumption :
  - Vcc = 3.0V C-grade: 45mA (@55ns) operating current
  - I -grade: 46mA (@55ns) operating current
  - C-grade: 36mA (@70ns) operating current
  - I -grade: 37mA (@70ns) operating current
  - 3.0uA (Typ.) CMOS standby current
- High speed access time :
  - -55 55ns
  - -70 70ns
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- I/O Configuration x8/x16 selectable by CIO, $\overline{LB}$ and $\overline{UB}$ pin

■ DESCRIPTION

The BS616LV1623 is a high performance, very low power CMOS Static Random Access Memory organized as 1,048,676 words by 16 bits or 2,097,152 bytes by 8 bits selectable by CIO pin and operates in a Vcc range of 2.7V to 3.6V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 3.0uA at 3.0V/25°C and maximum access time of 55ns at 3.0V/85°C . This device provide three control inputs and three states output drivers for easy memory expansion.

The BS616LV1623 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The BS616LV1623 is available in 48-pin 12mmx20mm TSOP1 package.

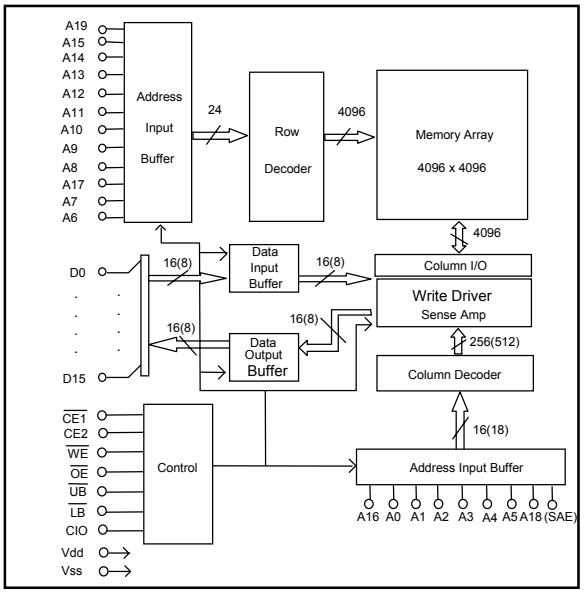
■ PRODUCT FAMILY

PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION			PKG TYPE
				STANDBY (I_{CCSB1}, Max)	Operating (I_{CC}, Max)		
			55ns : 3.0~3.6V 70ns : 2.7~3.6V	Vcc=3V	Vcc=3V 55ns	Vcc=3V 70ns	
BS616LV1623TC	+0°C to +70°C	2.7V ~ 3.6V	55 / 70	10 uA	45mA	36mA	TSOP1-48(12mmx20mm)
BS616LV1623TI	-40°C to +85°C	2.7V ~ 3.6V	55 / 70	20 uA	46mA	37mA	TSOP1-48(12mmx20mm)

■ PIN CONFIGURATIONS

48-pin 12mmx20mm TSOP1 top view

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Function
A0-A19 Address Input	These 20 address inputs select one of the 1,048,576 x 16-bit words in the RAM.
SAE Address Input	This address input incorporates with the above 20 address inputs select one of the 2,097,152 x 8-bit bytes in the RAM if the CIO is LOW. Don't use when CIO is HIGH.
CIO x8/x16 select input	This input selects the organization of the SRAM. 1,048,576 x 16-bit words configuration is selected if CIO is HIGH. 2,097,152 x 8-bit bytes configuration is selected if CIO is LOW.
$\overline{CE1}$ Chip Enable 1 Input **CE2 Chip Enable 2 Input**	$\overline{CE1}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
$\overline{LB}$ and $\overline{UB}$ Data Byte Control Input	Lower byte and upper byte data input/output control pins. The chip is deselected when both $\overline{LB}$ and $\overline{UB}$ pins are HIGH.
D0 - D15 Data Input/Output Ports	These 16 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	CIO	$\overline{LB}$	$\overline{UB}$	SAE	D0~7	D8~15	VCC Current
Fully Standby	H	X	X	X	X	X	X	X	High-Z	High-Z	I_{CCSB}, I_{CCSB1}
	X	L				X	X				
Output Disable	L	H	H	H	X	X	X	X	High-Z	High-Z	I_{CC}
Read from SRAM (WORD mode)	L	H	L	H	H	L	H	X	Dout	High-Z	I_{CC}
						H	L		High-Z	Dout	
						L	L		Dout	Dout	
Write to SRAM (WORD mode)	L	H	X	L	H	L	H	X	Din	X	I_{CC}
						H	L		X	Din	
						L	L		Din	Din	
Read from SRAM (BYTE Mode)	L	H	L	H	L	X	X	A-1	Dout	High-Z	I_{CC}
Write to SRAM (BYTE Mode)	L	H	X	L	L	X	X	A-1	Din	X	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +85	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	$0^{O}C$ to $+70^{O}C$	2.7V ~ 3.6V
Industrial	$-40^{O}C$ to $+85^{O}C$	2.7V ~ 3.6V

■ CAPACITANCE (1) (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	10	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	12	pF

1. This parameter is guaranteed and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = -40°C to + 85°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS			MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(3)			Vcc=3V	-0.5	--	0.8	V
V_{IH}	Guaranteed Input High Voltage(3)			Vcc=3V	2.0	--	Vcc+0.3	V
I_{IL}	Input Leakage Current	Vcc = Max, V_{IN} = 0V to Vcc			--	--	1	uA
I_{LO}	Output Leakage Current	Vcc = Max, $\overline{CE1}$ = V_{IH}, or CE2 = V_{IL}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to Vcc			--	--	1	uA
V_{OL}	Output Low Voltage	Vcc = Max, I_{OL}= 2mA		Vcc=3V	--	--	0.4	V
V_{OH}	Output High Voltage	Vcc = Min, I_{OH}= -1mA		Vcc=3V	2.4	--	--	V
I_{CC} (4)	Operating Power Supply Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} , I_{DQ} = 0mA, F = Fmax(2)	55ns	Vcc=3V	--	--	46	mA
			70ns		--	--	37	
I_{CCSB}	Standby Current-TTL	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} , I_{DQ} = 0mA		Vcc=3V	--	--	1.3	mA
I_{CCSB1} (5)	Standby Current-CMOS	$\overline{CE1}$ ≧ Vcc-0.2V, or CE2 ≦ 0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V		Vcc=3V	--	3	20	uA

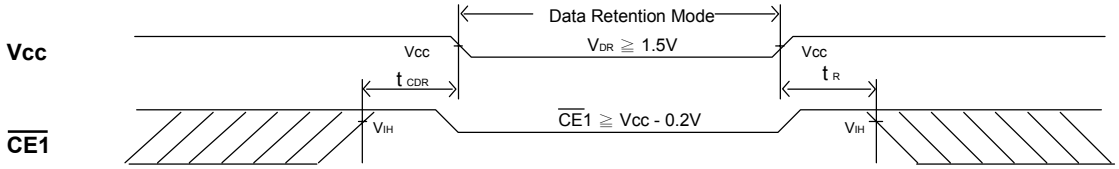
1. Typical characteristics are at TA = 25°C. 2. Fmax = $1/t_{RC}$.
3. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
4. $I_{CC\_Max.}$ is 45mA(@55ns) / 36mA(@70ns) during 0~70°C operation. 5. I_{CCSB1} is 10uA at Vcc=3.0V and T_A=70°C.

■ DATA RETENTION CHARACTERISTICS (TA = -40°C to +85°C)

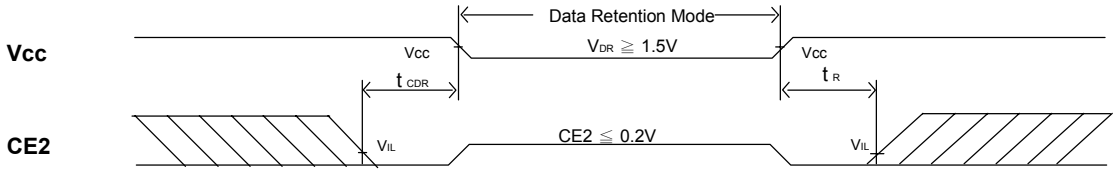
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE1} \geqq$ Vcc - 0.2V or CE2 $\leqq$ 0.2V or $\overline{LB} \geqq$ Vcc - 0.2V and $\overline{UB} \geqq$ Vcc - 0.2V $V_{IN} \geqq$ Vcc - 0.2V or $V_{IN} \leqq$ 0.2V	1.5	--	--	V
I_{CCDR} (3)	Data Retention Current	$\overline{CE1} \geqq$ Vcc - 0.2V or CE2 $\leqq$ 0.2V or $\overline{LB} \geqq$ Vcc - 0.2V and $\overline{UB} \geqq$ Vcc - 0.2V $V_{IN} \geqq$ Vcc - 0.2V or $V_{IN} \leqq$ 0.2V	--	1.5	5	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		T_{RC} (2)	--	--	ns

1. Vcc = 1.5V, T_A = + 25°C
2. t_{RC} = Read Cycle Time
3. I_{CCDR}(Max.) is 2.5uA at TA=70°C.

■ LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)



■ LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)

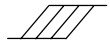
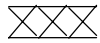
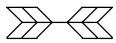


■AC TEST CONDITIONS

(Test Load and Input/Output Reference)

Input Pulse Levels	Vcc / 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5Vcc
Output Load	C_L = 30pF+1TTL C_L = 100pF+1TTL

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF "STATE

■ AC ELECTRICAL CHARACTERISTICS (TA = -40ºC to +85ºC)

READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 70ns Vcc = 2.7~3.6V MIN.	TYP.	MAX.	CYCLE TIME : 55ns Vcc = 3.0~3.6V MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	70	--	--	55	--	--	ns
t_{AVQV}	t_{AA}	Address Access Time	--	--	70	--	--	55	ns
t_{ELQV}	t_{ACS1}	Chip Select Access Time ($\overline{CE1}$)	--	--	70	--	--	55	ns
t_{ELQV}	t_{ACS2}	Chip Select Access Time (CE2)	--	--	70	--	--	55	ns
t_{BA}	t_{BA} (1)	Data Byte Control Access Time ($\overline{LB}$,$\overline{UB}$)	--	--	35	--	--	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	35	--	--	30	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z (CE2,$\overline{CE1}$)	10	--	--	10	--	--	ns
t_{BE}	t_{BE}	Data Byte Control to Output Low Z ($\overline{LB}$,$\overline{UB}$)	5	--	--	5	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	--	--	5	--	--	ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z (CE2,$\overline{CE1}$)	--	--	35	--	--	30	ns
t_{BDO}	t_{BDO}	Data Byte Control to Output High Z ($\overline{LB}$,$\overline{UB}$)	--	--	35	--	--	30	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	30	--	--	25	ns
t_{AXOX}	t_{OH}	Data Hold from Address Change	10	--	--	10	--	--	ns

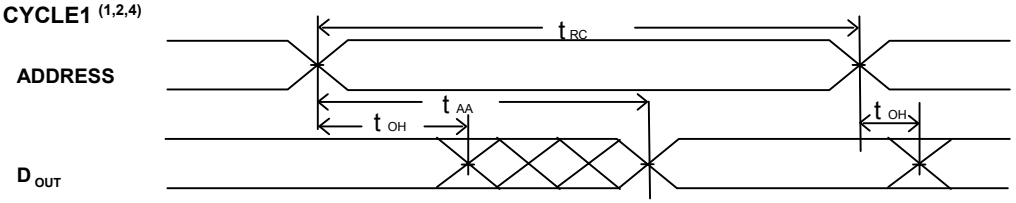
NOTE :

1. t_{BA} is 35ns/30ns (@speed=70ns/55ns) with address toggle .

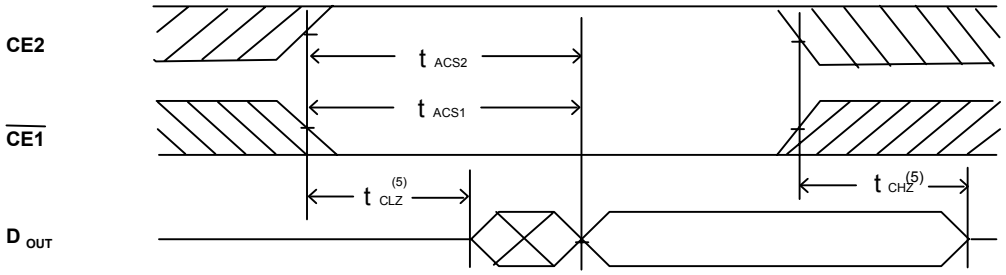
   t_{BA} is 70ns/55ns (@speed=70ns/55ns) without address toggle .

■ SWITCHING WAVEFORMS (READ CYCLE)

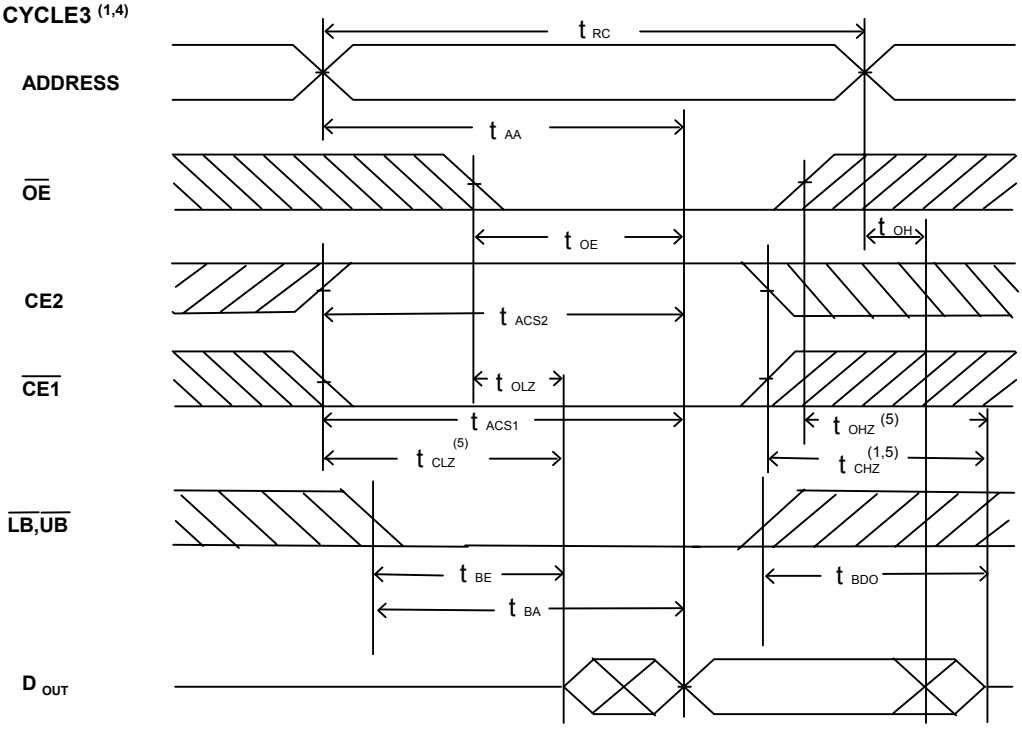
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:
1. $\overline{WE}$ is high in read Cycle.
2. Device is continuously selected when $\overline{CE1}$ = V_{IL} and CE2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and CE2 transition high.
4. $\overline{OE}$ = V_{IL} .
5. The parameter is guaranteed but not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS (TA = -40°C to +85°C)

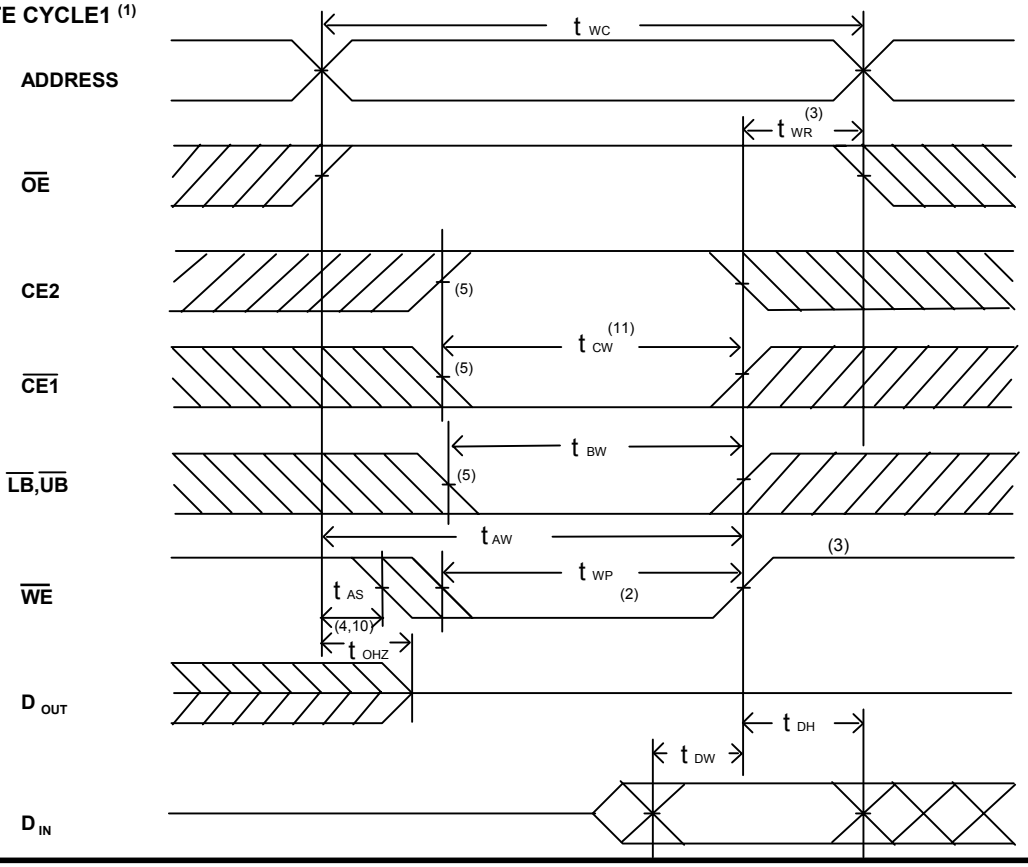
WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 70ns Vcc = 2.7~3.6V MIN.	TYP.	MAX.	CYCLE TIME : 55ns Vcc = 3.0~3.6V MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	70	--	--	55	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	70	--	--	55	--	--	ns
t_{AVWL}	t_{AS}	Address Setup Time	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	70	--	--	55	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	35	--	--	30	--	--	ns
t_{WHAX}	t_{WR}	Write recovery Time (CE2,$\overline{CE1}$,$\overline{WE}$)	0	--	--	0	--	--	ns
t_{BW}	t_{BW} (1)	Date Byte Control to End of Write ($\overline{LB}$,$\overline{UB}$)	30	--	--	25	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	--	--	30	--	--	25	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	30	--	--	25	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	30	--	--	25	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5	--	--	5	--	--	ns

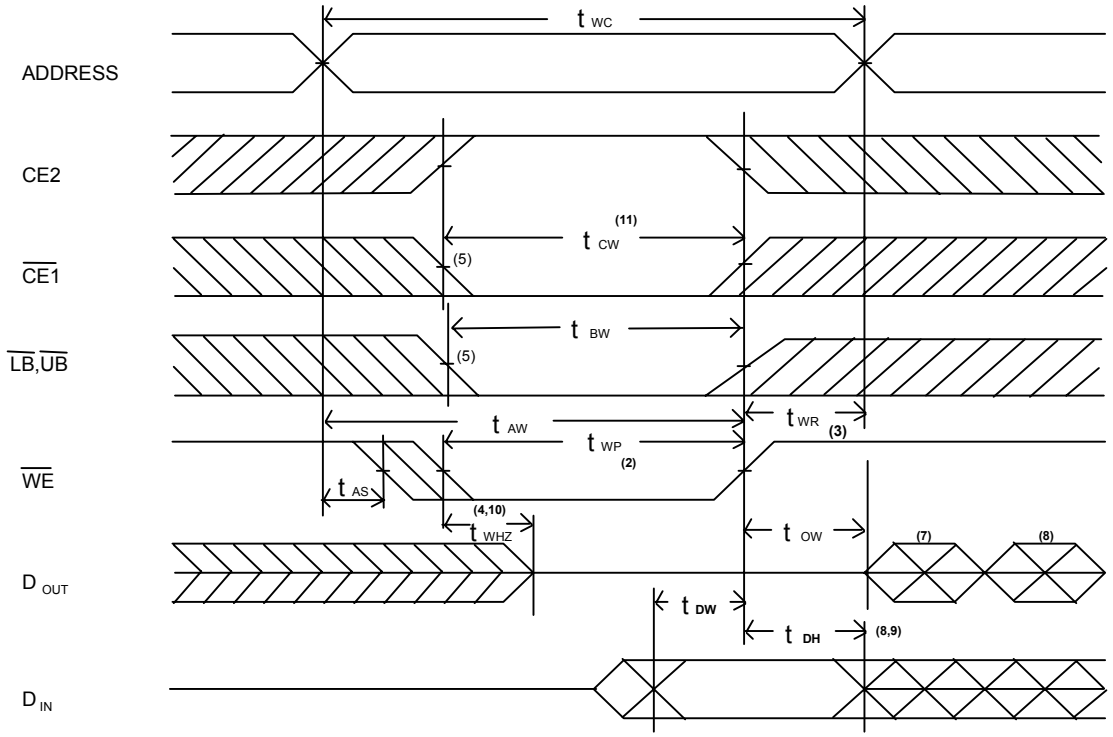
NOTE :
1. t_{BW} is 30ns/25ns (@speed=70ns/55ns) with address toggle. ; t_{BW} is 70ns/55ns (@speed=70ns/55ns) without address toggle.

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (1)



WRITE CYCLE2 (1,6)



NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE2, $\overline{CE1}$ and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of CE2 going low, or $\overline{CE1}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE2 high transition or CE1 low transition or $\overline{LB}$,$\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CE2 is high or $\overline{CE1}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of CE2 going high or $\overline{CE1}$ going low to the end of write.

■ ORDERING INFORMATION

BS616LV1623 X X Z Y Y

SPEED
55: 55ns
70: 70ns

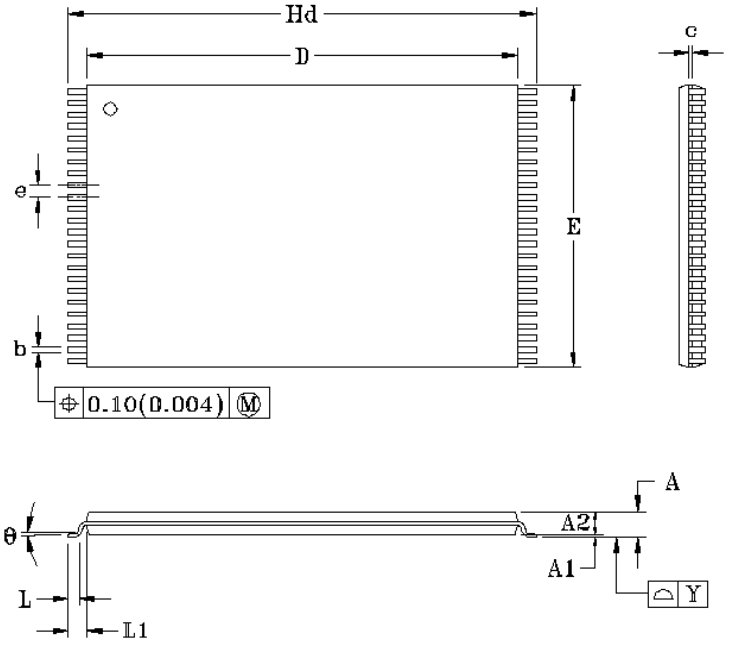
PKG MATERIAL
-: Normal
G: Green
P: Pb free

GRADE
C: +0°C ~ +70°C
I: -40°C ~ +85°C

PACKAGE
T : TSOP1-48(12mmx20mm)

Note:
BSI (Brilliance Semiconductor Inc.) assumes no responsibility for the application or use of any product or circuit described herein. BSI does not authorize its products for use as critical components in any application in which the failure of the BSI product may be expected to result in significant injury or death, including life-support systems and critical medical instruments.

■ PACKAGE DIMENSIONS



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.10	0.125	0.16	0.004	0.005	0.006
D	18.30	18.40	18.50	0.720	0.724	0.728
E	11.90	12.00	12.10	0.468	0.472	0.476
Hd	19.80	20.00	20.20	0.780	0.787	0.795
e		0.50			0.020	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.80			0.031	
Y	0.00		0.10	0.000		0.004
θ	1°	3°	5°	1°	3°	5°

TSOP1-48 (12mm x 20mm)